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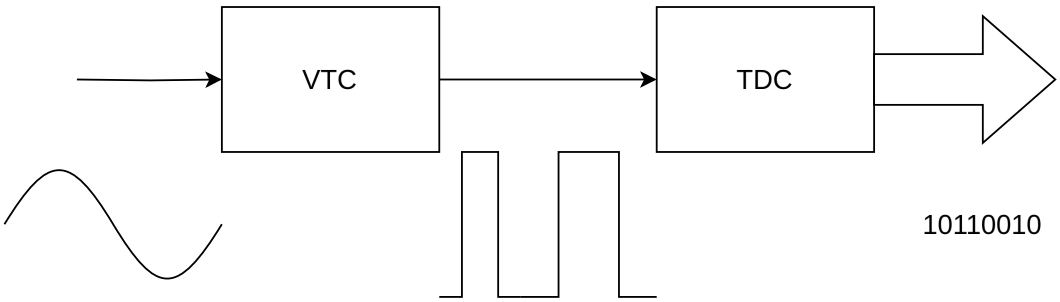

Very High Speed, Time Domain, Analog-to-Digital Converter

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Eletrical and Computer Engineering

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Declaration

I declare that this document is an original work of my own authorship and that it fulfills all the requirements of the Code of Conduct and Good Practices of the Universidade de Lisboa.

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I want to express my sincere gratitude to the many people who have contributed to the completion of this thesis.

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Resumo

Motivado por avanços tecnológicos e comunicações de alta velocidade, os serializadores e deserializadores, que requerem conversores analógico-Digitais nos recetores, operam com frequências superiores a $100\ GSa/s$. Frequências tão elevadas só podem ser alcançadas intercalando no tempo vários conversores, cada um a trabalhar com frequências mais baixas, impactando a área e o consumo energético. Aliado ao facto dos nós tecnológicos mais recentes afetarem negativamente as características e design dos circuitos analógicos, em favor da velocidade e consumo energético dos circuitos digitais, existe um crescente interesse em circuitos de processamento de sinal no domínio do tempo, impulsionando a substituição de blocos analógicos por alternativas digitais. Conversores tensão-tempo codificam a informação contida na amplitude do sinal num intervalo de tempo entre eventos. Conversores tempo-digital traduzem esta informação de tempo em bits. Estas arquiteturas não só beneficiam das tecnologias mais recentes, como também mostram resultados promissores, comparáveis ou até superiores aos alcançados no domínio da tensão, quer em frequência ou consumo energético.

O presente trabalho estuda arquiteturas no domínio do tempo e propõe num conversor analógico-digital de 7 bit com uma frequência de 5 GHz. Um conversor tensão-tempo, gerador de rampa dupla de modo comum com apenas uma fonte de corrente, seguido por um conversor tempo-digital SAR com células de atraso seletivas, conclui num ENOB = 6.5 bit, TDH = -46.38 dB, consumindo $12,54$ mW e com uma figura de mérito de Walden $FOM_W = 27.71$ fJ/conv. São também apresentados alguns dos problemas esperados com possíveis soluções e melhorias.

Palavras Chave

Conversor analógico-digital, Processamento de sinal no domínio do tempo, Conversor tensão-tempo, Conversor tempo-digital, Elevado ritmo de transmissão, Célula de atraso selectivo.

Abstract

Motivated by the advances in technology and high-speed communications, Serializers-Deserializers (SerDes), which require Analog-to-Digital Converters (ADCs) in the receiver, operate with frequencies in excess of 100 GSa/s. Such high frequencies can only be achieved by time interleaving multiple ADCs, each operating at a lower nominal rate, which impacts area and power overhead related to signal and clock distribution. Recent advancements in semiconductor technology favor digital over analog circuits, particularly in terms of speed and power efficiency. To address this trend, Time-Mode Signal Processing (TMSP) circuits have emerged as a promising solution to replace analog blocks with digital alternatives. Voltage-to-time converters (VTC) encode voltage amplitude signal information as a time interval between events. Time-to-digital converters (TDC) can then translate the time information into bits. These architectures not only take advantage of the most recent nodes' benefits but also show very promising results in terms of frequency and power consumption, comparable to and even exceeding the voltage domain achievements.

The present work studies Time Domain (TD) architectures and concludes on a proposed ADC of 7 bits, operating at 5 GHz. A common mode ramp generator VTC followed by a Successive Approximation Register (SAR) TDC using Selective Delay Tuning (SDT) Cells achieves a 6.5 bit ENOB with a TDH = -46.38 dB consuming 12.54 mW, concluding a Walden Figure of Merit (FOM_W) of 27.71 fJ/conv. Expected problems, possible solutions, and circuit improvements are also stated.

Keywords

Analog-to-digital converter (ADC), Time mode signal processing (TMSP), Voltage-to-time converter (VTC), Time-to-digital converter (TDC), High-speed, Selective delay tuning (SDT).

Contents

List of Tables

List of Figures

Acronyms

ADC	Analog-to-Digital Converter
CM	Common Mode
CS	Constant Slope
DAC	Digital-to-Analog Converter
ENOB	Effective-Number-of-Bits
FOM	Figure of Merit
FS	Full-Scale
INL	Integral Nonlinearity
LSB	Least Significant Bit
MSB	Most Significant Bit
MUX	Multiplexer
PVT	Process, Voltage and Temperature
RMS	Root Mean Square
SAR	Successive Approximation Register
SerDes	Serializers-Deserializers
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SDT	Selective Delay Tuning
TA	Time Amplifier
TC	Time Comparator
TD	Time Domain
TDC	Time-to-Digital Converter

THD	Total-Harmonic-Distortion
TI	Time Interleaver
TMSP	Time-Mode Signal Processing
ULVT	Ultra Low Voltage Threshold
VCDU	Voltage Controlled Delay Unit
VCO	Voltage-Controlled Oscillator
VS	Variable Slope
VTC	Voltage-to-Time Converter

1

Introduction

Contents

1.1 Motivation

Today's technologies are evolving to require very high bandwidth and speed. In such a world, where the demand is driven by cutting-edge technologies such as artificial intelligence, the Internet of things, virtual reality, or high-speed communication; the networking systems need to be capable of handling heavy processing tasks.

High-speed Serializers-Deserializers (SerDes) have a key role in such circuits and allow the communication between both the system and its exterior (inter-chip) and different components of the same chip (intra-die). Emergent SerDes implementations, which require Analog-to-Digital Converters (ADCs) in the receivers, feature sampling frequencies in excess of 100 GSa/s. Such high frequency can only be achieved by time-interleaving many unitary ADCs, each operating at a lower sampling frequency. To minimize area, and the power overhead related to signal and clock distribution, it is important to reduce the number of unitary ADCs, which implies increasing their individual operating speed, leading to degraded power efficiency.

Addressing this challenge, an alternative approach that has been gaining traction involves the use of Time Domain (TD) ADCs. Such circuits enable attaining high speeds while maintaining good power efficiency.

These ADCs are usually composed of a Voltage-to-Time Converter (VTC) followed by a Time-to-Digital Converter (TDC), having the input signal in the voltage domain, translating it to a time difference between events and ultimately converting it to a usefully binary representation. Such circuits leverage predominantly digital building blocks, thus capitalizing on the benefits of advanced CMOS technologies, such as amplified speed and reduced power consumption, not being impacted by the analog's diminished capacities.

Some state-of-the-art work is directed at exploring these types of architectures, reaching optimistic results comparable to and even exceeding the voltage domain achievements.

1.2 Objectives

The objective of this work is to explore the use of TD conversion techniques. Multiple TD ADCs architectures are to be explored, comparing them and leading to a conclusion on the benefits, drawbacks, and main challenges of each implementation.

Ultimately a very high-speed, low-resolution, full working ADC is to be proposed. Concluding on a circuit that will be studied in detail and simulated, deciding on its viability for further work and eventually its silicon implementation. Such a device will work individually as a single module; nonetheless, it will be able to incorporate a time-interleaving system, with similar modules, where the operation at much higher frequencies is possible.

To conclude on numbers for the end goal of such a circuit, allow the following parameters to be taken into consideration:

Table 1.1: Objective parameters.

Sampling Frequency (f_s)	Number of bits (N_b)	Power
5 GSa/s	7 bit	$\lessapprox 20$ mW

A differential 400mV peak-to-peak input is to be considered. Each single-ended signal will have an appropriate Common Mode (CM) voltage, varying 100mV in each direction. Regarding the technology node on which these circuits will be based, a 16nm FinFET node is used.

This thesis was conducted in the context of an internship at Synopsys (SNPS Portugal), making use of Synopsys tools in all the steps of circuit creation and simulation.

1.3 Document Organisation

This document is organized as follows:

In chapter 2 there is an introduction to analog-to-digital conversion, outlining the concepts involved. It is followed by some of the most common voltage domain architectures, with their benefits and drawbacks. The time domain concept in signal conversion is presented, explaining the key concepts and main blocks. There is a conclusion on the state of the art and the position of these TD converters in such an environment.

In chapter 3 multiple voltage-to-time conversion implementations are explored, presenting circuits and their respective simulation results. A circuit is proposed to perform this conversion for the present specifications.

Having the signal encoded in the time domain, time-to-digital conversion implementations are presented in chapter 4. A proposed circuit is concluded to achieve the necessary signal translation.

To conclude, in chapter 5, the chosen VTC and TDC are put together to constitute the full ADC, reaching a voltage-to-digital complete system. The results are shown, outlining some problems, possible solutions, and future work to develop.

2

Analog-to-Digital Converters' Fundamentals and Time Domain Conversion

Contents

2.1 Fundamentals of Analog-to-Digital Conversion

In the physical world, signals tend to have analog characteristics, meaning they are time-continuous with an amplitude comprised within a range that, even if limited to a certain interval, has infinite possible values. The signals resultant from the observation of the physical world, a transducer's outputs, also tend to be analog, following the same characteristics as the measured signal, just as some other quantity.

Even if true that analog processing of signals can be done, and some simple operations related to signal conditioning and filtering are performed in this domain, digital processing has many advantages, and conversion of the analog signal to the digital domain, where the necessary operations are performed, is beneficial. Some advantages worth mentioning are the less complex circuits, which result in a more power-efficient and economical option to produce, along with benefits in the storage, access, transmission, and display of digital signals, as well as a better immunity to noise and external factors. The drawbacks of this conversion are related to loss of information and accuracy, as a digital signal is time discrete and amplitude quantized, limited to a finite number of values within a limited interval, dependent on the operation frequency and the used number of bits.

To perform this conversion, between the analog and digital realms, ADCs and Digital-to-Analog Converters (DACs) are used. Even if DACs are of extreme importance, as some ADCs use DACs in their architectures, they are outside the scope of this work and will not be detailed.

2.2 Concepts and Metrics

There are many concepts and metrics used to describe and understand the universe of ADCs, some of which will be used throughout this work. Because of that, some of these concepts are worth explaining and detailing, summarizing their meaning and application while helping to define and understand ADCs working principles [7–9].

SerDes: Technology that involves the conversion of parallel data to serial data and vice versa, enabling efficient data transmission over high-speed serial links. It is crucial for high-speed data transmission and communication between different electronic components. It incorporates clock data recovery functionality to ensure that the transmitted data is synchronized and accurately recovered on the receiving end as well as impedance matching circuitry to minimize signal distortion and ensure optimal signal integrity during data transmission. Such technology is a foundational component in various modern technologies, including high-speed networking, telecommunications, and data centers, playing a crucial role in facilitating rapid and reliable data transfer, that nowadays requires frequencies in the hundreds of Giga Hertz. To achieve higher transmission rates, recent architectures use pulse amplitude modulation with four codes, therefore ADCs are required to decode the received signal.

Time Interleaver (TI): This technique involves the use of multiple identical ADCs to process sampled

data in parallel, resulting in a higher effective sampling rate and increased overall system performance, figure 2.1. Multiple problems arise with this technology use, such as calibration and clock synchronization issues, the need for very efficient sample and hold circuits, and the use of a high number of individual ADCs which incurs in area and power consumption problems. However, it is a solution to achieve higher conversion frequencies, as with recent ADC applications, very high frequencies are required.

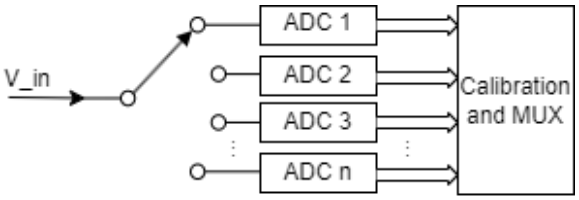


Figure 2.1: Time interleaved process exemplification with the distribution of the input signal through multiple parallel analog-to-digital converters.

Power Consumption (**P**): Amount of power consumed by the ADC during the conversion process. Measured in joules per conversion (J/conv) or in Watt (W).

Sampling Rate or **Sampling Frequency** (f_s): Rate at which the ADC samples the input signal to convert it from the continuous analog domain to a discrete digital form. It is usually measured in samples per second (S/s) or Hertz (Hz). A higher sampling rate allows the ADC to capture more details of the analog signal. As the sampling process is of extreme importance, a sample and hold may be needed to sample and hold a stable voltage for the duration of the conversion.

Related to the sampling frequency, there can be a classification of either a Nyquist rate or Oversampling ADCs. The first are defined as converters that operate at a certain frequency (f_s), sampling, and therefore converting, signals with a bandwidth of up to half of said operation frequency $\left(f_\mathsf{max} = \frac{f_\mathsf{s}}{2}\right)$, obeying the Nyquist–Shannon sampling theorem; the latest operate at much faster rates than the input bandwidth maximum frequency (f_max), usually with an oversampling ratio $= \frac{f_\mathsf{s}}{2f_\mathsf{max}}$ of 10 to 512, enabling the use of techniques such as noise-shaping or modulations.

Resolution: Number of bits ($N_\mathbf{b}$) used to represent the analog signal. It determines the ADC's ability to distinguish between small changes in the input voltage. Higher resolution generally leads to more precise digital representations of the analog signal. The higher the N_b, the lower the value of the Least Significant Bit (LSB), and therefore a lower **quantization step** (Δ_V) between consequent words is present,

$$\Delta_V = \frac{V_\mathsf{max} - V_\mathsf{min}}{2^{N_\mathsf{b}} - 1}. \tag{2.1}$$

Regarding this topic, an ADC may be, subjectively, classified as being of high-resolution ($N_\mathsf{b} \gtrapprox 14$ bit), medium-resolution ($N_\mathsf{b} \in [8; 14]$ bit), or low-resolution ($N_\mathsf{b} \lessapprox 8$ bit).

Input Range and **Full-Scale (FS) Range**: Range of analog input voltages that the ADC can effec-

tively convert to digital values, without distortion. If a voltage is either higher or lower than the maximum (V_{max}) or minimum (V_{min}) range voltage, respectively, saturation will happen and the output value will be that of the maximum or minimum voltage supported.

Errors and Nonlinearities: When considering an ideal ADC, the aspects of its constitution are assumed to be linear and not suffer from any error. Such is not achievable once errors are always present. Offset and gain errors introduce deviations in the transfer characteristic as a whole, while differential nonlinearity and Integral Nonlinearity (INL) affect the uniformity of the quantization steps. Missed codes can occur due to these errors or other factors, leading to further inaccuracies, which can significantly impact the accuracy of analog-to-digital conversions.

Noise: On every signal, apart from the useful information carried, there is always the presence of unwanted fluctuations that disrupt the integrity of the signal. There are multiple noise sources, including the quantization error, other internal influences such as the sample switch or clocks feed-through, non-linearities in the system that may create signal harmonics, thermal noise, or interference from external sources. To quantify the noise present in a signal and in its conversion, there are multiple quantities.

- **Signal-to-Noise Ratio (SNR)**: Ratio of the power of the signal (P_{signal}) to the power of the noise (P_{noise}). A higher SNR indicates less impact of the noise on the signal leading to a more accurate conversion,

$$\text{SNR} = 10\log\left(\frac{P_{\text{signal}}}{P_{\text{noise}}}\right)\ \text{dB}\,. \tag{2.2}$$

  If only the quantization noise is considered, and the input signal is a perfect sinusoid, without harmonics or distortions, then a direct relation to N_b can be derived in equation 2.3,

$$\text{SNR} = 10\log\left(\frac{S_{\text{RMS}}}{e_{\text{RMS}}}\right)^2 = 10\log\left(\frac{\frac{V_{\text{max}}-V_{\text{min}}}{2\sqrt{2}}}{\frac{\Delta_V}{\sqrt{12}}}\right)^2 \approx 6.02N_{\text{b}} + 1.76\ \text{dB}\,. \tag{2.3}$$

- **Spurious-Free Dynamic Range (SFDR)**: Measure of the ability of signal detection and harmonic rejection. It represents the ratio of the power of the fundamental signal to the power of the strongest spurious tone or harmonic. It can be seen in the frequency domain and is typically expressed in dB. With S as the signal's amplitude and S_{h_max} is the maximum amplitude harmonic, equation 2.4 S is concluded,

$$\text{SFDR} = 20\log\left(\frac{S}{S_{h\_max}}\right)\ \text{dB}. \tag{2.4}$$

- **Total-Harmonic-Distortion (THD)**: Measures the level of distortion caused by harmonics in a signal, indicating the extent to which the output deviates from the ideal sinusoidal waveform. THD is calculated as the ratio of the sum of the powers of all harmonic components (V_{RMS_n}, the Root

Mean Square (RMS) value of the n^{th} harmonic voltage), to the power of the fundamental frequency (V_{RMS_1}),

$$\text{THD} = 20\log\left(\frac{\sqrt{V_{\text{RMS}_2}^2 + V_{\text{RMS}_3}^2 + V_{\text{RMS}_4}^2 + \dots}}{V_{\text{RMS}_1}}\right) \text{ dB.} \tag{2.5}$$

- **Signal-to-Noise-and-Distortion Ratio (SNDR)**: Takes into consideration the previous quantities, accounting for both noise and distortion and representing the quality of the signal, quantifying how much the signal's amplitude exceeds the combined noise and distortion levels,

$$\text{SNDR} = 10\log\left(\frac{P_{\text{signal}}}{P_{\text{noise}} + P_{\text{distortion}}}\right) \text{ dB .} \tag{2.6}$$

- **Effective-Number-of-Bits (ENOB)**: Represents the number of bits an ideal ADC would have for the same SNR as the actual ADC under consideration. The equation can be derived from equation 2.3,

$$\text{ENOB} = \frac{\text{SNDR[dB]} - 1.76}{6.02} \text{ .} \tag{2.7}$$

Digital Output Code: Even if a trivial concept, different output code formats may be used in different ADCs' conversion steps. The most usual output code is the binary one, with a possible difference with either the use of an unsigned or a signed (2'complement) code. However, other options may be used: a thermometer encoding used, for example, in flash ADCs; or a Gray-code, used to reduce the errors and noise sensitivity associated with bit state transitions. It is worth noting that, once in the digital domain, the translation from one code to another is the result of a digital logic circuit.

Figure of Merit (FOM): A numerical quantity based on one or more characteristics of a system or device that represents a measure of efficiency or effectiveness [1]. Numerous metrics can be used to quantify the performance of an ADC, however, the three most useful ones to include in a FOM are resolution, conversion rate, and power consumption. A FOM should not be used as the only indicator of an ADC performance but rather as an additional value to better understand its behavior. Furthermore, when comparing two ADCs there should be an awareness regarding a disparity in two metrics that could lead to a similar FOM value but represent two completely different types of operation. The following FOM can be considered the most used:

- Walden FOM: Takes into consideration the referred three metrics, the trade-off between power consumption, sampling rate, and resolution, with lower values typically indicating better performance. Considering the process variations as the main contributing factor for power growth with resolution increase, this FOM considers that power grows by a factor of 2 per bit added. Its value

is expressed in energy per conversion step.

$$\text{FOM}_\text{W} = \frac{P}{f_\text{s} 2^{\text{ENOB}}}. \tag{2.8}$$

- Schreier FOM: As in the previous FOM, this quantity measures a trade-off between the same properties. However, with a higher FOM_s value typically indicating better performance, it is more suitable for ADCs where the power consumption per bit added is limited by thermal noise, considering a $4\times$ power growth per bit. For an SNDR greater than ≈ 60dB, this FOM became the most appropriate quantity to use.

$$\text{FOM}_\text{S} = \text{SNDR} + 10\log\left(\frac{\frac{f_\text{s}}{2}}{P}\right). \tag{2.9}$$

There are multiple architectures possible for an ADC. Characteristics such as accuracy (resolution), sampling frequency, size, power consumption, power supply voltage, and complexity, among many others, are needed to bear in mind when choosing what circuit to use or build for the application in hands [10]. Therefore it is important to understand the existing architectures and the limitations they have [11, 12].

Known as the fastest architecture to convert a signal, there is the **flash or parallel ADC**. By comparing the input voltage with multiple reference voltages, simultaneously, a thermometer bit scale is created. These are rather simple circuits that can support large input bandwidth, as the conversion is only dependent on the comparator's characteristics and the speed of the logic circuit that follows. However, flash ADCs are usually limited to a resolution of around 7 bit, as for every increased bit in the resolution, the number of comparators and voltage references needs to be doubled. This fact implies an increase in the power consumption, area of the circuit, and the need for high voltage reference accuracy with lower voltage steps.

Arguably the most used type of ADC are the **Successive Approximation Register (SAR)** as they employ a good balance between conversion speed, resolution, and power consumption. The name derives from the binary search algorithm used to perform the conversion process, as the digital approximation output is adjusted until it converges to the analog input's value. In every clock period, one bit of the binary word is tested, creating a voltage in the DAC and comparing it to the input voltage; if the input voltage is higher than the generated DAC voltage, the tested bit will remain at '1' while the remaining bits are to be tested; if the input voltage is lower than the generated DAC voltage, the tested bit will be corrected to a '0' for the rest of the comparisons. For the increase of a single bit, there is only the need to increase the conversion time by a single period, but a better DAC and comparator are needed.

The **Sigma-Delta ADCs ($\Sigma\Delta$)** are known for having very high resolutions as they use noise-shaping techniques to generate a stream of digital bits at a frequency much higher than the input. After a process of filtering and decimation, the output binary word is arrived at with a high SNR [13]. However, to reach

such remarkable resolutions, a high complexity circuit, clock frequency, and synchronization problems are encountered, limiting the output frequency.

Pipeline ADC divide the conversion process into multiple steps, separating the determination of certain bits through different stages and therefore allowing for higher resolution with an increase in operating frequency. These architectures allow for very high speed and high resolution, limited by the DAC and operation circuits performance, at the cost of a complex system incurring a high power consumption.

There are many more types of architectures, slight variations from the ones mentioned or combinations of two or more. However, all these ADCs are voltage domain ADCs as in they directly convert voltage into a digital word. They are, in fact, the most common architectures in use. Nonetheless, technologies that take advantage of less analog-dependent circuits by using digitally friendly blocks, are starting to be explored and present benefits with comparable or even improved results. Some architectures may use voltage-to-frequency converters such as Voltage-Controlled Oscillators (VCOs), while others convert and process signals in the TD. These will be the aim for the rest of this thesis.

2.3 State of the Art Time Domain Analog-to-Digital Converters

The advances in technology, with the scaling down of transistor features, aim to increase the system's performance and reduce manufacturing costs. Such reduced-size devices are fully taken advantage of by digital blocks as they occupy a smaller area, consume less power, and are able to operate under increased switching speeds and lower voltage supply, increasing the packing density and reaching higher levels of integration.

However, when referring to analog blocks, which rely on the actual shape of the entire voltage characteristic and not only on the fast transition between a couple of discrete states, there is a clear degradation of performance. Due to drop in transistor intrinsic gain, increase in device variations, and decrease in signal-to-noise ratio caused by the shrinking of supply voltage, analog design becomes increasingly more complex, with a poor bias point operation, large gate leakage, reduced input voltage swing and linearity problems.

In such a reality, replacing analog blocks with digitally friendly and digitally intensive alternatives has many advantages. Therefore, efforts should be put in place to pursue digital alternatives to analog components [14, 15].

In the case of voltage ADCs, because these devices are based on the translation of an analog quantity, they operate with signals using, in most cases, analog blocks. In order for there to be a substitution with digital blocks the signal information needs to be encoded in a quantity that can be used in a digital domain, such as time, where the information is encoded in the waveform transitions instead of its amplitude. The encoding of signals in time and their further digitization is not new and

has been adopted in early designs of ADCs going back to 1942 [16]. There are many applications where such devices are already used to measure time intervals: particle and nuclear physics, all-digital phase-locked-loops, positron emission tomography scans, light detection and ranging (LiDAR), digital oscilloscopes, biomedical imaging scanners or on-chip sensors [16].

Even if not to a full extent, the use of digital blocks in place of analog circuits may enable digital syntheses and digital test methods, improving certain steps of the design flow. Furthermore, some architectures, or parts of architectures, may be reproduced in FPGAs, taking advantage of these circuits for tests and simplification of the production process.

Academic work in this realm is still scarce, with a recent growing interest illustrated by the number of papers in recent conferences [4, 17–33], already some Ph.D. theses [34–36], along with more complex publications as systematic reviews [2, 16, 37, 38] and even dedicated books [6, 39].

2.3.1 Key Concepts and Working Principles of Time Domain Converters

The main idea of a TD ADC is to first convert the voltage to time-encoded impulses, with a time interval between events proportional to the amplitude of the input voltage. This can be done using a VTC. Once in the TD, a circuit that detects the time difference between said events can be used to generate a digital word, proportional to the time duration, a TDC. The block diagram of said idea can be seen in figure 2.2.

The respective opposite circuits are also possible and indeed exist, a time-to-voltage converter and a digital-to-time converter. One of the first ideas to measure time intervals was to use a time-to-voltage converter and then apply the resulting voltage to a voltage ADC [6]. Even if of some importance, these types of circuits will not be further detailed in the present work.

All these circuits can be grouped into a more general classification of circuits called Time-Mode Signal Processing (TMSP) circuits, which share the same principle of time encoding information to detect, store, and manipulate sampled analog signals [39].

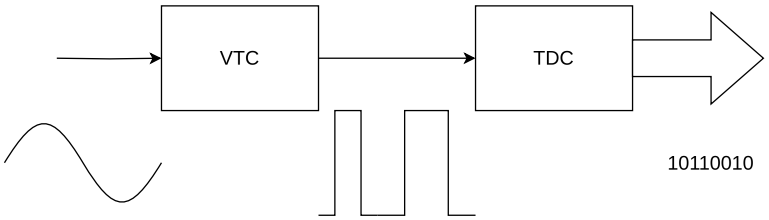
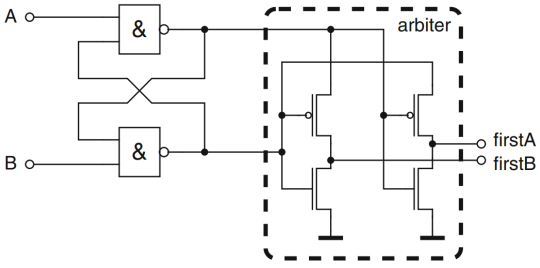


Figure 2.2: Block diagram of a voltage-to-time converter followed by a time-to-digital converter.

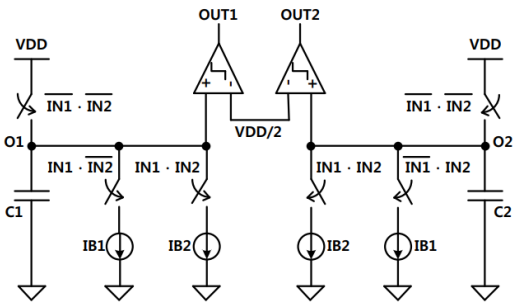
Regarding the VTC, even though there are multiple types of circuit solutions, the most common principle is to charge and/or discharge a capacitor from an initial voltage and subsequently detect the time at which the capacitor voltage crosses a threshold [2]. These circuits will be detailed in the following chapter 3.

With the signal information encoded in the TD, a TDC can be used to obtain a binary representation of the signal. There are multiple architectures, some of which are based on the voltage ADCs seen above, while others are new concepts. These circuits will be discussed in chapter 4.

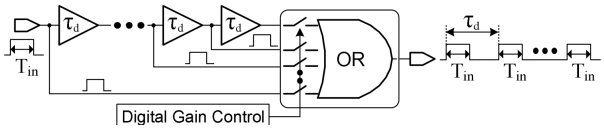
Another TMSP block worth mentioning is a Time Amplifier (TA). Similarly to the voltage amplifiers used in a pipeline ADCs, in between conversion steps, if a pipeline or hybrid architecture is used, such a circuit may be needed, but in the TD. The idea is to amplify the time difference of the two relevant input events by increasing, proportionally to the input time, the time distance of the output events. The first architectures were based on SR latches [40], with the circuit presented in figure 2.3(a), where a gain between 3 and 10 can be achieved. This circuit has, however, limitations on the input time interval, only working for events with time spacing in the order of a few pico-seconds, defined by the discharging time of the NAND output. Further developments were made and architectures such as the Pulse-Train TA, presented in [41], with the circuit represented in figure 2.3(c), showing a programmable gain but a different approach to the amplification process as a time repetition of the signal, instead of a time stretch of the signal duration; or the high-gain wide-input-range with an open-loop and a gain equal to the current bias ratio presented in [42], an interesting design presented in figure 2.3(b). These circuits are still far from perfection and a lot needs to be done in the area to reach good and useful solutions.



(a) NAND latch (from [6]).



(b) high-gain wide-input-range with an open-loop and a gain equal to the current bias ratio (from [42]).



(c) Pulse Train TA (from [41]).

Figure 2.3: Time amplifier Circuits.

2.3.2 State of the Art

To consult the state of the art and have access to a high number of published ADCs' information, the Boris Murmann's ADC Performance Survey is one of the best collections of data [1]. This Survey collects information from the International Solid-State Circuits Conference (**ISSCC**) and the Institute of Electrical and Electronics Engineers (**IEEE**) SYMPOSIUM on Very Large Scale Integration TECHNOLOGY and CIRCUITS (**VLSI**) since 1997 up until the present day, with regular updates.

In order to better understand and compare similar purpose ADCs, filtering is needed to reduce the many different options to a comprehensible number. Recalling the objectives of the present work, of a low resolution ($N_b \approx 7$ bit), very high speed ($f_s > 1$GHz) and lower power consumption and area, the following filters were applied: Area < 1 mm^2, SNDR > 40 dB, $f_s > 1$ GHz, P < 1 W, OSR $= 1$ focusing only on Nyquist rate ADCs. With a further, more subjective, selection to eliminate older architectures/technologies, the tables 2.1 and 2.2 represent the state-of-the-art ADCs that fulfill the mentioned specifications.

ADC	Year	Type	Technology	Area [mm^2]	SNDR [dB]	P [W]	f_s [GHz]	FOM$_W$ [fJ/conv]
[43]	2023	SAR, TI	7n	0.9	46.5	7.50E-1	24	181.0
[44]	2024	Pipe, TI	28n	0.24	54.1	1.80E-1	12	36.2
[45]	2017	SAR, TI	28n	0.184	49.0	3.00E-1	8	162.9
[46]	2015	Pipe, SAR, TI	28n	0.45	46.1	1.50E-1	5	181.9
[47]	2019	VCO, TI	28n	0.023	45.2	2.27E-2	5	30.5
[48]	2024	SAR, TI	28n	0.015	44.3	7.70E-3	4.8	12.0
[49]	2016	Pipe, TI	16n	0.24	56.0	3.00E-1	4	145.5
[50]	2023	Pipe, TI	7n	0.0243	60.2	7.75E-3	1.8	5.0
[51]	2016	SAR, TI	65n	0.9	65.0	3.77E-2	1.6	16.2

Table 2.1: State of the art voltage analog-to-digital converters (from [1]).

ADC	Year	Type	Technology	Area [mm^2]	SNDR [dB]	P [W]	f_s [GHz]	FOM_W [fJ/conv]
[31]	2020	TI, TD	65n	0.095	40.1	5.08E-2	10	61.5
[4]	2022	Pipe, SAR, TD	14n	0.00143	40.80	7.40E-3	5	16.5
[32]	2023	Pipe, TD	28n	0.0056	51.4	1.39E-2	2.6	17.6
[33]	2023	Pipe, TD	28n	0.03375	60.4	2.7E-2	2	15.8
[26]	2023	Pipe, SAR, TI, TD	28n	0.016	62.50	6.9E-3	1	6.3
[23]	2023	SAR, TD	28n	0.009	36.40	3.17E-2	1	48.2
[27]	2022	TD	28n	0.074	50.10	3.15E-2	2.5	58.7
[28]	2022	Pipe, TD	28n	0.083	58.20	1.49E-2	1	22.4

Table 2.2: State of the art time domain converters.

In the first table, table 2.1, there is the state-of-the-art voltage ADCs. There are two facts worth mentioning, and that goes per the mentioned above. All the presented ADCs use TI modules, meaning that the frequency reached is due to the existence of at least two independent modules put together to work temporally in alternation. Secondly, most architectures are either SAR, pipeline or a combination of both, proving that for a high frequency of operation, with low to medium resolution, a SAR ADC is

the most suitable option, with pipeline architectures improving in complexity while maintaining and/or increasing speed and converted bits.

Table 2.2 presents TD architectures, some already present in Murmann's ADC Performance Survey, others taken from other sources and papers. By comparison, a conclusion that TD architectures, even if only very recently explored, present clear good results that compete with the considered state of the art in the voltage domain and even go beyond, reaching higher frequencies without TI, not degrading the resolution performance.

So far it was shown the realm of ADCs as something of considerable size and complexity with multiple options and considering details. When referring to TMSP circuits and their benefits, TD ADCs, even if a fairly recent technology, show a promising path to be explored. These circuits allow very high speeds, reduced power consumption, and low to medium resolution, ideal to the present work specifications. The following chapters will detail the referred VTC and TDC blocks, stating possible architectures, their strengths, and weaknesses.

3

Voltage-to-Time Conversion

Contents

As stated in subsection 2.3.1, the goal of a TMSP circuit such as a VTC is to proportionally map a time-varying voltage-domain signal to a time variable. This circuit, being the frontier between the two used signal domains is a fundamental building block in any TD ADC.

In the following sections, the operation of various VTCs, detailing both Variable Slope (VS) and Constant Slope (CS) architectures, will be examined. There will be some design considerations, performance, and simulation results for each architecture, looking for a suitable circuit, useful for the set requirements. A final circuit is proposed, capable of converting the differential input into TD signals.

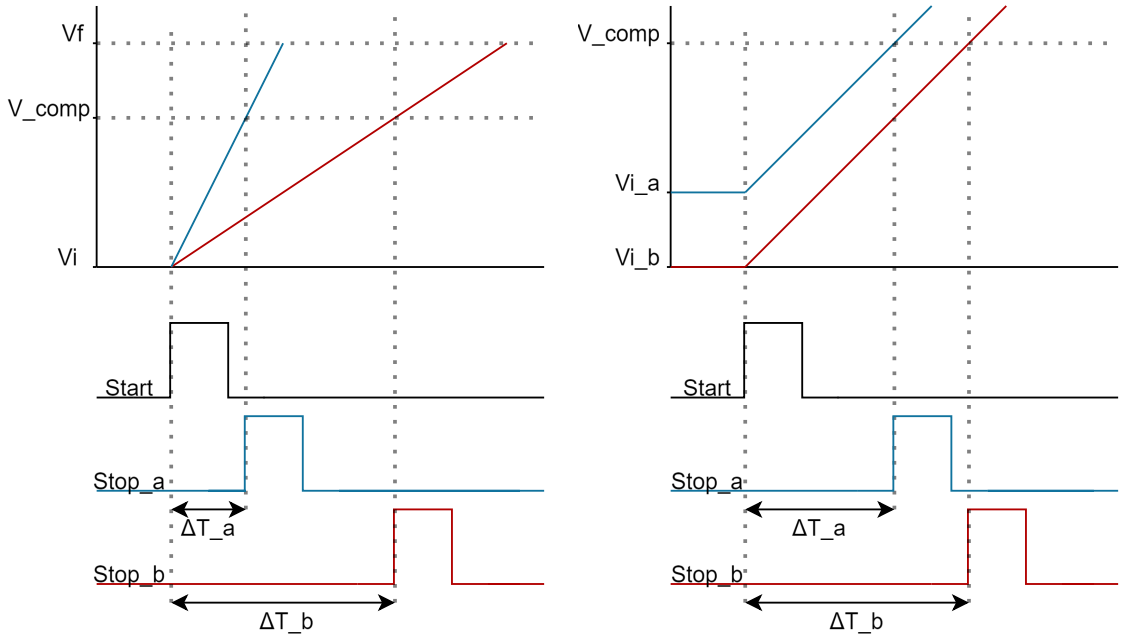
3.1 Voltage-to-Time Converters Working Mode

When a time variable is mentioned, it is, most often, defined as a time difference between events, a start event indicating the beginning of the time interval, and a stop event declaring its conclusion. Examples of such events may be the rising/falling edge of two signals, either in series (in the same line) or in parallel (different wires). Alternatively, the events may be present as part of the same signal, as in a pulse width modulation, with the rising and falling edges of the same wave. Even though, most commonly, TDCs tend to make use of the first example, there are situations where the second one is needed, such as in the Pulse Shrinking TDC (described in section 4.2).

There are many forms in which this conversion may take place, however, in a very simplified way, these circuits will control the charging and/or discharging of a capacitance, comparing it to known voltages. Depending on the characteristics of the charging/discharging current, VTCs can be loosely classified as either VS VTCs or CS VTCs. In a VS VTC the initial and final voltages (V_i and V_f) are known and well-defined, the input voltage will determine the slope and, therefore, the time needed to change from one voltage to the other. On a CS VTC the capacitor's voltage rate of change will be the same, so the input voltage will only affect the initial capacitor's voltage or the sensing comparator's reference voltage (V_comp). In figure 3.1 there is a simple comparison of these methods.

Generally speaking, it can be stated that VS VTCs are simpler, therefore consuming less power and working at higher possible frequencies, while also having a higher gain. However, they are inherently non-linear, strongly affecting the resolution. On the other hand, CS VTC are more complex, consume more power, and have lower gain, but present higher linearity [38].

This separation will be taken into consideration and the following sections will describe some possible architectures of each of these VTCs.



(a) VS VTC **(b)** CS VTC

Figure 3.1: Variable slope voltage-to-time converter and constant slope voltage-to-time converter mode of operation comparison.

3.2 Variable Slope Architectures

In figure 3.2 is presented a Voltage Controlled Delay Unit (VCDU). This is a very simple example of a VS VTC. With ϕ_{in} as a clock, controlling either the charge or discharge of C_{Fixed}, V_{in} controls the current that passes through $M3$, serving as a control to the capacitor discharge time. The inverter at the end serves as a sensing comparator to change the state of ϕ_{out} once the C_{Fixed} voltage passes the inverter threshold. $M4$ guarantees that the capacitance will always discharge within the used time window, even if $V_{\text{in}} = 0$V.

Such a circuit generates an output with a duration, between the rise of ϕ_{in} and the rise of ϕ_{out}, inversely proportional, to V_{in}. Furthermore, it can then be used as a building block to construct more complex circuits, such as in [52] where higher linearity, lower power consumption, and higher tolerance to Process, Voltage and Temperature (PVT) variations are achieved by applying V_{in} to two VCDUs. Further work is being done in this area, and new architectures are being explored for an increase in speed, time resolution, and linearity, and a decrease in power consumption [22].

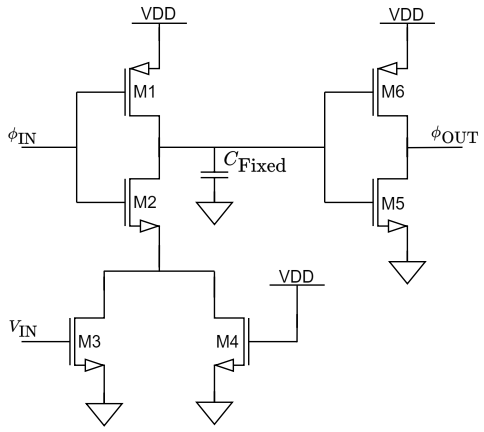


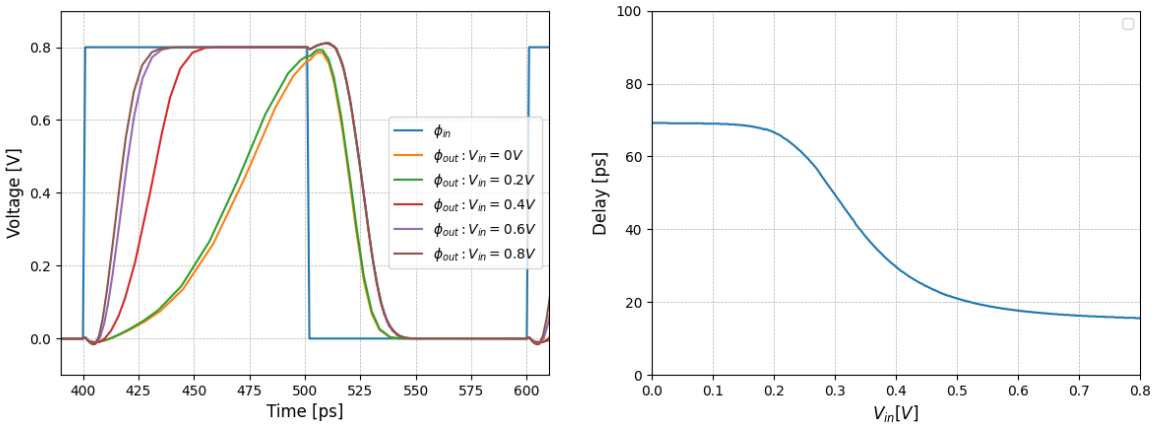
Figure 3.2: Voltage controlled delay unit with V_{in} controlling the capacitance discharging, CMOS schematic [2].

The first design step is to define the circuit's output capacitance. With such a value the sensing comparator size and therefore its input capacitance, which will add to C_{Fixed}, can be concluded. While $\phi_{\mathrm{in}} = 0$, $M1$ has to fully charge this capacitance, therefore this transistor size is determined. Having as an objective to achieve a time resolution as high as possible, the half period in which the conversion takes place must be fully taken advantage of. To do so, when discharging this node, and if $V_{\mathrm{in}} = \mathrm{V_{DD}}$, ϕ_{out} must commute as early as possible, $M2$, and by the same conclusion $M3$, need to have a large size. If $V_{\mathrm{in}} = 0\mathrm{V}$, ϕ_{out} must commute as late as possible while still within the time in which $\phi_{\mathrm{in}} = \mathrm{V_{DD}}$, this concludes on the size for $M4$.

In [38] are presented some architectural changes that may take place, such as the inclusion of degeneration resistances or the application of the clock to different parts of the circuit. However, the main idea is the same and the results show small differences among them.

As for the size of C_{Fixed}, it was concluded that an explicit capacitor is not needed for the technology and frequency in use. The capacitance of the involved transistors, mainly the gate capacitance of the sensing comparator, along with all the other parasitic, are enough.

Conducting a voltage sweep for V_{in} results in figure 3.3(a). While $\phi_{\mathrm{in}} = 0$, C_{Fixed} charges and ϕ_{out} goes to 0. When $\phi_{\mathrm{in}} = \mathrm{V_{DD}}$, depending on the value of V_{in}, ϕ_{out} will take more or less time to rise. The slope of ϕ_{out} may be corrected and normalized by adding buffers between this stage and further circuits. Figure 3.3(b) is the delay achieved as a function of V_{in}, measured from 50% of ϕ_{in} to 50% of ϕ_{out} .



(a) Transient analyses.

(b) Input voltage sweep.

Figure 3.3: Voltage controlled delay unit with V_{in} controlling the capacitance discharging.

A possible change is to control not the discharging, but the charging of the capacitance, by mirroring the circuit, figure 3.4. Its behavior is the same, only working on the complementary clock half period, presenting a direct proportionality between V_{in} and the delay from the rise of ϕ_{in} to the fall of ϕ_{out}. The results can be seen in 3.5.

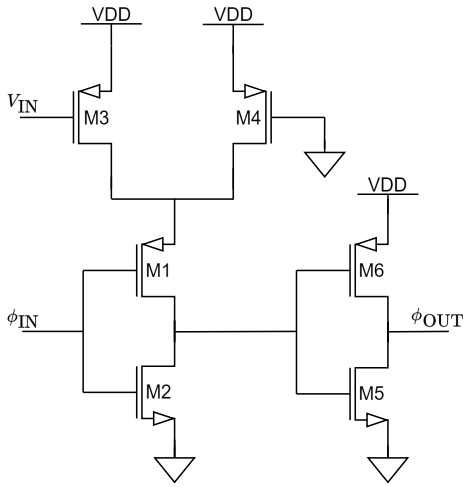
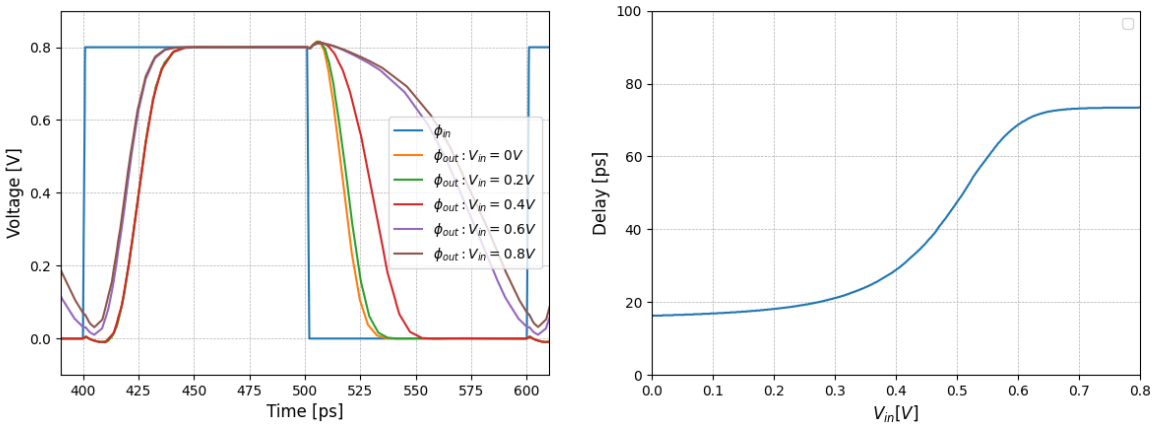


Figure 3.4: Voltage controlled delay unit with V_{in} controlling the capacitance charging, CMOS schematic [2].



(a) Transient analyses.

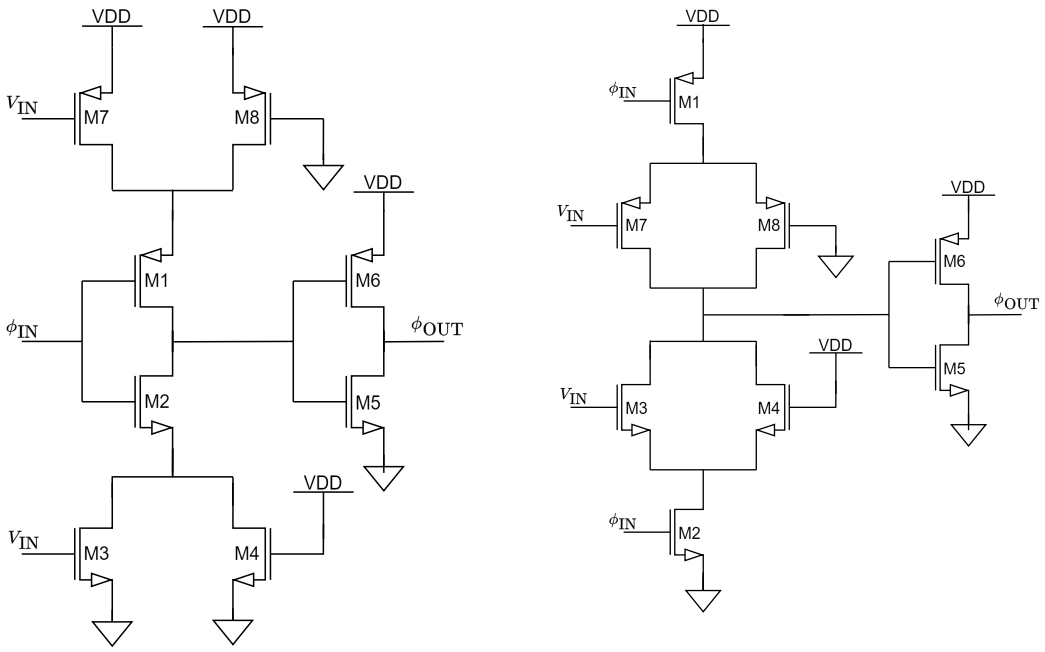
(b) Input voltage sweep.

Figure 3.5: Voltage controlled delay unit with V_{in} controlling the capacitance charging.

With the presented in figures 3.6 and 3.5 there are already some visible problems. There is a very strong non-linearity present for the full V_{in} sweep which can be attenuated by the smaller FS needed, adjusting the CM voltage to the preferable range. Additionally, this circuit is single-ended, and not directly compatible with the required differential input. This can be solved by applying two parallel circuits, each receiving the differential inputs. It is worth mentioning that the different proportionality between the delay of ϕ_{in} to ϕ_{out} in relation to V_{in}, among the two tested circuits is irrelevant when using a differential input. The result will be the difference between the two ϕ_{out}, not using ϕ_{in} as a reference in the final calculations.

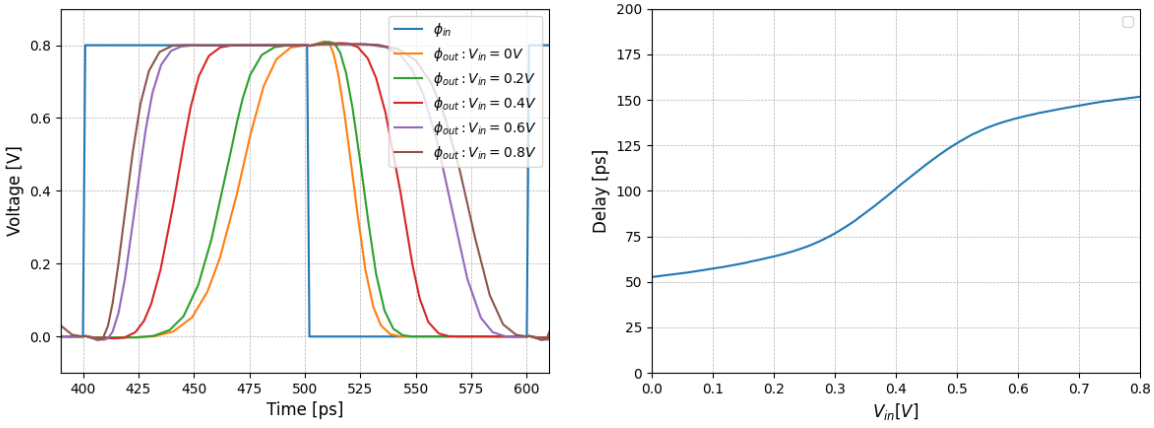
Taking inspiration from the ideas presented in [52] of controlling both the charging and the discharging of the capacitance's, circuits such as the ones in figure 3.6 may be used. 3.6(a) presents better linearity as the clocked transistors serve as degeneration resistance for the input voltage transistors, improving the characteristic. The transient and voltage sweep for this circuit, figure 3.6(b), are presented in figure 3.7.

It is important to note that this circuit is not differential input compatible. There may be possible changes to turn this idea into a differential circuit, such as applying one input for the charging and the other for the discharging of the same capacitance however, as the created time events are the rising and falling edge of the same signal, not using ϕ_{in} as a direct reference, the differential use is not possible as in the previous VTCs. Nonetheless, the existence of the two time events in the same signal means it can be used directly in architectures as the pulse shrinking TDCs. Furthermore, it is interesting to note the use of almost the full period to encode the signal, and not only half of the period, as in the other implementations.



(a) **(b)**

Figure 3.6: Voltage controlled delay unit with V_{in} controlling capacitance both charging and discharging, CMOS schematic.



(a) Transient analyses.

(b) Input voltage sweep.

Figure 3.7: Voltage controlled delay unit with V_{in} controlling capacitance both charging and discharging.

Lastly, the architectures explored in [3] show a very interesting option of using the bulk biasing of the starving transistors, not the gate, as an input to V_{in}, figure 3.8. As presented in the paper, it shows a better linearity at the cost of a smaller gain, figures 3.9. However, using FinFET technology, the body

effect is almost negligible, lowering the gain to unusable values. Furthermore, porting such a circuit to newer technologies, using gate-all-around transistors, would reduce even more the body biasing effect, to very much null values.

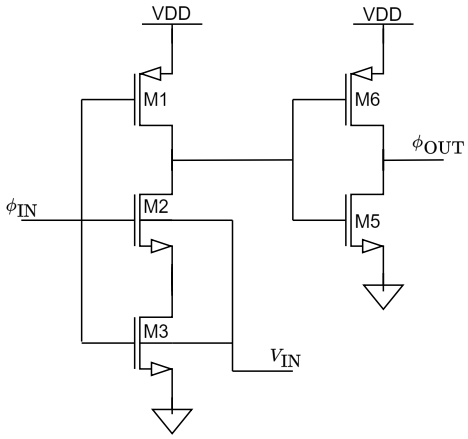
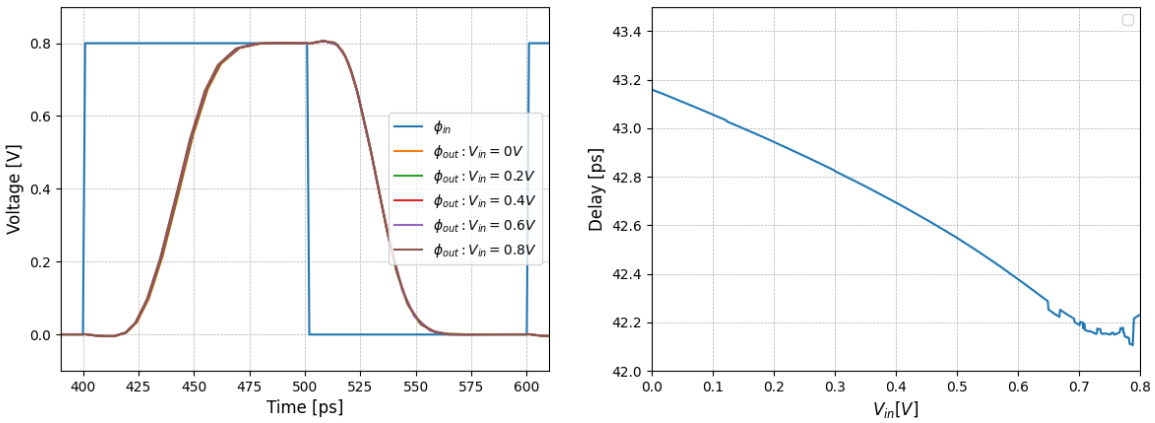


Figure 3.8: Voltage controlled delay unit with body biasing control, CMOS schematic [3].



(a) Transient analyses.

(b) Input voltage sweep.

Figure 3.9: Voltage controlled delay unit with body biasing control.

Analyzing all the presented VTCs, a conclusion should be drawn regarding their possible use for the current project. To do so, the differential input described in section 1.2 of two single-ended opposite phase signals varying $100mV$ from the CM voltage is used.

Disregarding the circuits where both charging and discharging are used, figure 3.6, and the body biasing approach, figure 3.8, because of the aforementioned limitations, only the charging or the discharg-

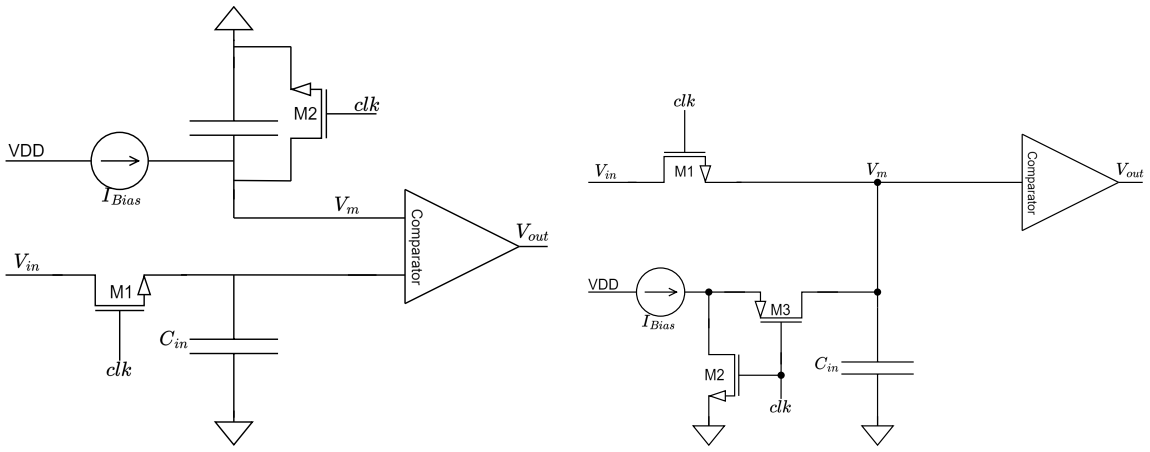
ing circuit are tested. For a differential input, two equal, parallel, circuits, each receiving a single-ended input, are used. VerilogA, ideal, sensing comparators detect the crossing of ϕ_{out} for both circuits and calculate the delay between the two output events.

The best achieved results are a THD $= -33.97$ dB, SNDR $= 31.99$ dB, ENOB $= 5$ bit, reached in the discharging circuit for a CM voltage of 0.4V and a comparator voltage threshold of 0.45V. There may be possible changes to improve the circuit, however, even without considering the sensing comparators, or possible corner and mismatch variations, the reached results are already below the required, showing the impossibility of using these circuits for the needed specifications.

3.3 Constant Slope Architectures

As stated in this chapter's introduction, CS VTCs can have two types of operation. Either both initial and final voltages are known, with the input voltage being used as the comparator's voltage reference; or the comparison threshold is always the same with the input voltage being sampled and used as the initial voltage to integrate. Example circuits using these modes of operation are depicted in figure 3.10.

The sensing comparator will be detailed in subsection 3.4. However, it can be advanced that because of speed constraints, the differential pair comparator most likely needed for the first approach, present in figure 3.10(a), is not an optimal choice for the operation frequency established in this work. Even if showing worse possible linearity, as the integration will not be constant through different inputs, only architectures based on the second implementation, figure 3.10(b), will be further explored. This is also the exemplification mode of operation depicted in the previously presented figure 3.1(b).



(a) CS VTC with V_{in} as the comparator's reference voltage **(b)** CS VTC with V_{in} as the initial integrating voltage

Figure 3.10: Constant slope voltage-to-time converter modes of operation example circuits.

Important factors to consider are the employed current steering techniques. As illustrated in figures

3.10 and in all subsequent schematics from now on, rather than blocking the current flow with a switching transistor, there is a short-circuit path to the ground. This approach diverts the current from the node, preventing abrupt changes in the current source. While this may increase power consumption, it offers several advantages as minimizing switching transients, such as voltage or current spikes, reduces noise and distortion. Moreover, keeping the current flow as continuous as possible improves the integration linearity and stability.

The idea present in 3.10(b) was constructed and tested to comprehend this circuit behavior. As with the seen VS VTCs this architecture is also intrinsically single-ended, with a possible differential implementation by employing two parallel circuits. There is also the possibility of creating either a rising or a falling ramp after sampling the signal voltage, therefore also achieving a charging or a discharging circuit. In practice, there are no benefits to using one architecture over the other, as the results are similar.

Independent of the chosen architecture, there are some limitations regarding the voltage range in use. If an NMOS transistor is used to sample the signal, as represented in figure 3.10(b), V_{in} is limited to the interval $[0; 0.5]$V. This is due to the fact that, with clk enabled with $V_{DD} = 0.8$V, V_{m} will only go up to around $V_{DD} - V_{\text{t}} \approx 0.8 - 0.3 = 0.5$V, before transistor $M1$ cuts off by not having a $V_{GS} \geq V_{\text{t}}$. On the symmetric circuit, and if a PMOS is used, the same logic can be applied, limiting V_{in} to $[0.3; 0.8]$V. In practice, these intervals are smaller than the stated, with a lower $V_{DS} = V_{\text{m}} - V_{\text{in}}$ on the sampling transistor, the resistance and therefore the time needed for the charging/discharging to happen can be greater than the existing period in use. Such facts reduce the input voltage range to $[0; 0.3]$V or $[0.5; 0.8]$V respectively for the mentioned situations. A CMOS passing gate can be used, enabling the FS voltage to be correctly sampled, however, the second issue regarding the sensing comparator threshold (V_{comp}) comes into play. Even if a sensing threshold of either V_{DD} or 0 could be realized, there would have to be a safe margin so that the comparator wouldn't trigger before the integration process starts. This limits the input to some voltage on an interval smaller than the FS. Realistically, the comparator threshold will be at least V_{t} away from V_{DD} or 0, so the use of a passing gate, even if still an interesting solution, little would improve to the overall question. There is also a similar, less impactful, issue with the current source. For the current mirror to work, its transistor needs to be in saturation, which also limits the value of V_{m}.

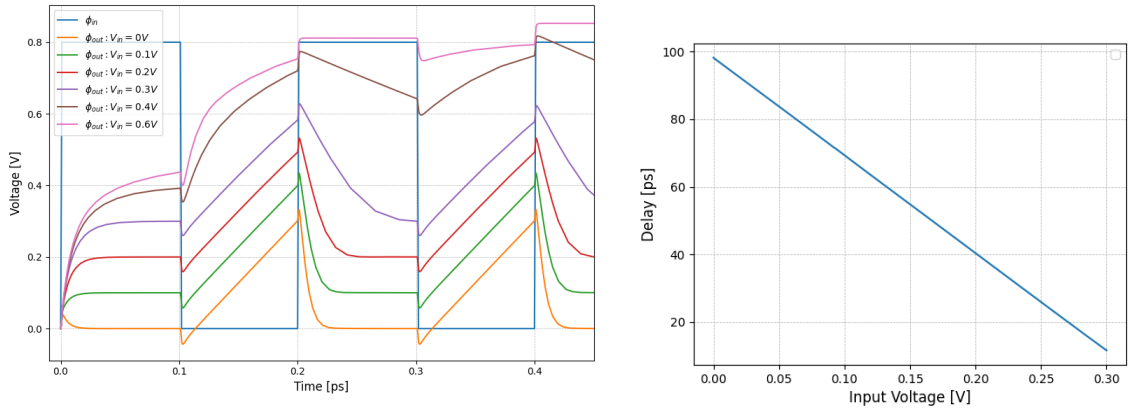
Still regarding the current source, the value for the current should be chosen so that the time interval generated is as large as possible, increasing the time resolution achieved. Considering the node charging architecture, and for the lowest input voltage situation ($V_{\text{in}} = V_{\text{in\_min}}$), the final V_{m} value should be equal to V_{comp}. Additionally, V_{comp} should also be as close as possible to the highest input voltage. In this other extreme situation ($V_{\text{in}} = V_{\text{in\_max}}$), as soon as the integration process starts, the comparator will trigger, allowing for the full integration window to be used to encode the input range. Equation 3.1 can

be used to determine the necessary current,

$$I_{\text{Bias}} = C_{\text{m}} \frac{dV}{dt} \approx C_{\text{m}} \frac{V_{\text{comp}} - V_{\text{in\_min}}}{\frac{T_{\text{S}}}{2}} \tag{3.1}$$

considering a clock duty cycle of 50% and therefore the integration process taking $\frac{T_{\text{S}}}{2}$.

As an example, the circuit presented in figure 3.10(b), a single-ended rising ramp architecture, was simulated. Figure 3.11(a) shows the transient of V_{m} for the FS voltage interval, proving the input limitations and showing the working mode of such a circuit. Figure 3.11(b) shows the DC characteristic for an input voltage sweep of V_{in} to $[0; 0.3]$V, using ideal VerilogA sensing comparator with $V_{\text{comp}} = 0.3$V. The visual result is already clearly much more linear than the previous solutions.



(a) Transient analyses.

(b) Input voltage sweep.

Figure 3.11: Constant slope, charging current source, ramp generator.

By using two parallel circuits and defining each single-ended signal to oscillate 100mV around a CM voltage of 100mV, the experimental optimal point, the differential approach was tested for the current project requirements. The results reached were of THD $= -40.24$ dB, SNDR $= 40.23$ dB, ENOB $= 6.39$ bit. These numbers, even if improved from the VS VTC, are still below the requirements, noting that the main circuit limitations are related to the current source and its linearity. It should also be noted that the sensing comparators are ideal, and do not introduce here any distortion or noise, something that will worsen the final results. Even if some possible improvements, able to elevate the reached results to values that are already above the specifications, may allow this architecture to be seen as a possibility for the current project, some further issues should be considered. For this differential architecture, there are two different current sources. A small variation in one of these current sources will unbalance the entire conversion process by creating two different slopes for each of the signals, introducing a systematic error. Also, differences in the $M2$s characteristics, or simply a clock mismatch between these current

steering transistors, will lead to the integration process starting with a relative delay between signals, introducing errors that can become significant as a result of a rather small variation. All the stated is compelling enough to look into alternative solutions, which increase even more the obtained linearity.

Following the same principle as the one detailed, there are some other interesting architectures. As an example, in [53] there is the use of a charge sharing circuit enabling very high frequencies. In [23] charge sharing is also used but with a single current source. This idea helps in solving the problems mentioned in the current source mismatch. A similar idea is also used in [4] where its understanding and direct application is easier to comprehend and replicate.

The CM ramp generator, presented in figure 3.12, uses different capacitors to sample the input voltage and to integrate the current. Furthermore, such a circuit is also directly differential.

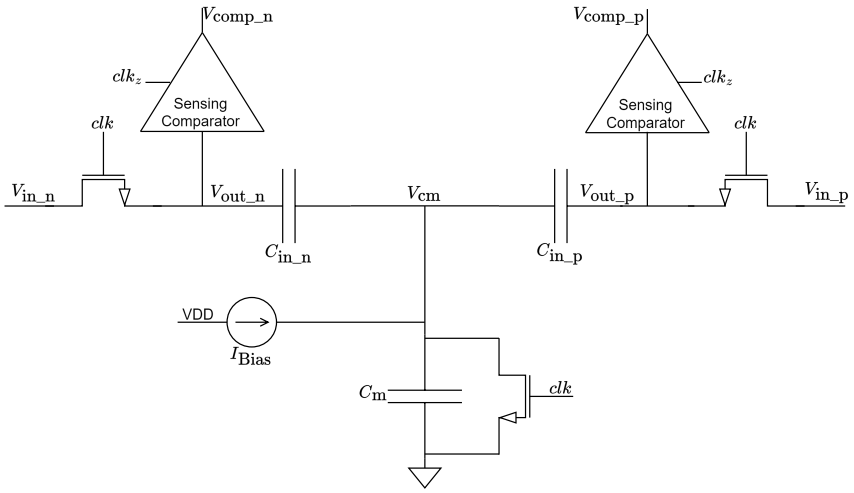


Figure 3.12: Common mode ramp generator voltage-to-time converter [4].

On the reset window, while the clock is high, the input signals V_{in_n} and V_{in_p} are sampled to C_{in_n} and C_{in_p}, respectively, while V_{cm} is shorted to ground, discharging C_m. There should also exist a non-overlapping of the clock that indexes both input transistors and the transistor that shorts V_{cm}. By discharging the common node before sampling the input voltages, distortion originated by charge injections is minimized. On the other clock half period, a constant I_{Bias} will charge C_m, whose voltage will rise with a constant slope. Because both V_{out_n} and V_{out_p}, with the input sampled voltages, are floating, the voltage difference through the capacitors will be near zero. Equation 3.2 shows the correct relation between V_{cm} and both V_{out},

$$V_{out} = \frac{C_{in}}{C_{in} + C_p} V_m \tag{3.2}$$

with C_p the parasitic capacitance on the V_{out} nodes, already considering the comparators input capacitance. This means that V_{out_n} and V_{out_p} will rise with, almost, the same slope as V_{cm} but with different

initial values, reaching the sensing comparator voltage at different times. The voltage difference is therefore encoded into a proportional time interval. Equation 3.3 shows the equivalent capacitance seen by the current source,

$$C_{\text{eq}} = C_{\text{m}} + 2\frac{C_{\text{in}}C_{\text{p}}}{C_{\text{in}} + C_{\text{p}}}. \tag{3.3}$$

It can be used in equation 3.1 to conclude on the needed current.

Once again, the inverse circuit, discharging the V_{cm} with a current source after the input signals sampling, is also viable and in practice shows no disadvantages when compared to the shown schematic. Only for a matter of simplification and to use a lower CM input voltage, the presented circuit was chosen in favor of this alternative.

This circuit has many advantages compared to the differential dual current source architecture tested, figure 3.10(b). The mentioned problems related to the current source mismatch are diminished, and the current charging both V_{out} nodes will be the same, only differing by possible capacitance size variations or comparator input non-linearities.

There is a possible argument for an increment in power consumption as the capacitors will increase, both in number and size. Therefore the current, which is also steered to ground on the reset time window, will have to be higher. Higher driving capacitors and higher currents tend to mean bigger transistors, so there is also an argument for circuit size increase. Nonetheless, this circuit was tested and the results were positive, leading this architecture to be further explored as the proposed VTC to use. The sizing and results for this circuit are detailed in section 3.5.

Apart from the aforementioned architectures, there are some other possible ideas for CS VTCs, not present in mainstream documentation. Two newer concepts are here presented as possible ideas to further explore.

One option is to use a latch. At the first moment, the latch is disconnected from both power rails, and the inverters are charged with the sampled input voltages. Once the latch is reconnected to power because the outputs already have different values, they will evolve to the respective opposite sides: the one with a higher voltage will evolve to V_{DD}, whereas the lower voltage will go to the ground. The difference in the latch's initial voltages will appear in the time it takes the outputs to reach either V_{DD} or ground. Such an architecture is extremely simple and power efficient. However, the results show a low gain and a logarithmic input to the delay function, figure 3.13. Even if not linear the slope characteristic is still constant, fitting the given definition.

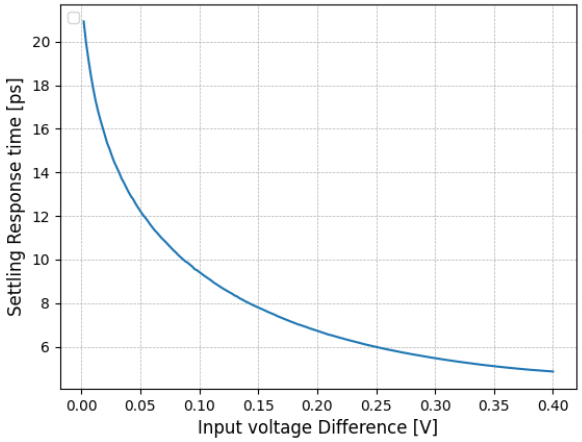


Figure 3.13: Latch logarithmic input to delay characteristic.

Another idea is to use a fully differential approach. On the studied VTCs, after the sampling process, the voltage nodes are both either charged or discharged. With a fully differential architecture, it should be expected that one of the signals is charged and the opposite is discharged, balancing out the charge/discharge characteristics. This idea is represented in figure 3.14.

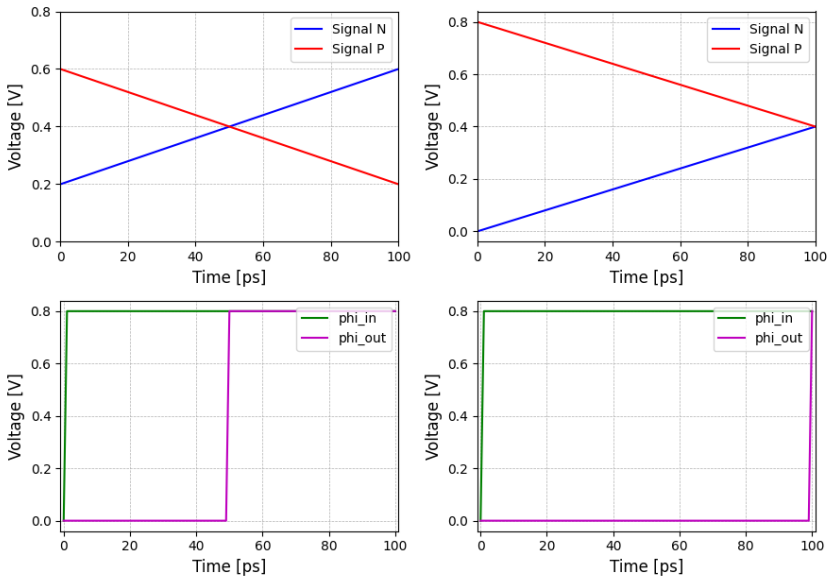


Figure 3.14: Fully differential concept.

The higher value node is discharged at a constant linear slope, while the lowest value is charged at an opposite, equal, slope. Detecting when both output nodes cross each other, at the middle voltage value, triggers the sensing comparator. This is a very promising idea, leading to a deeply linear circuit. Nonetheless, there are some issues that complicate such a concept. Firstly it needs to be determined

which is the highest and the lowest input voltages, comparing both inputs. There can be complications comparing very close values, due to small variations or mismatches, which would result in wrong decisions, possibly leading to the charge of the highest signal and the discharge of the lowest signal, not achieving a signal output crossing and therefore no sensing comparator triggering. Both output nodes also have to be capable of either charging or discharging with the same slope, which increases complexity and error sources. The signal crossing detection has to be done by a differential, continuous, comparator, which was seen to be slow. All these needed signal processing are very time-consuming and result in disregarding such a circuit for the presented specification situation.

3.4 Sensing Comparator

A very important circuit in all the presented VTCs is the comparator used to detect when the capacitor's charge has crossed the necessary threshold. This circuit is also responsible for emitting the output pulse representing this event. Most of the papers omit this circuit explanation or take its architecture as something trivia. Apart from [38] which presents the circuit in figure 3.15(a), most papers only present simple inverters without mentioning them or present nothing at all. However, the experience when developing the proposed VTC is compelling to give a general overview of the encountered problems.

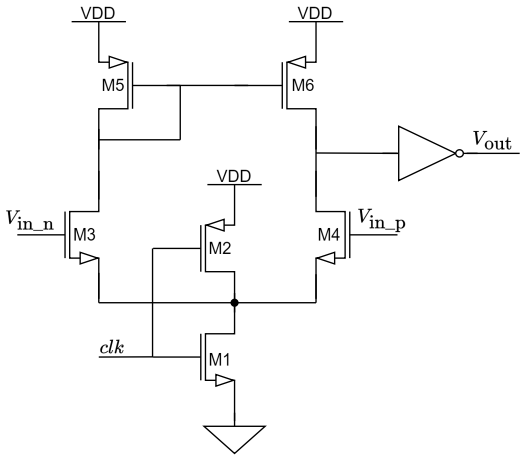
3.4.1 Differential Pair

A common implementation for a comparator is the differential pair circuit, figure 3.15). This circuit takes two input voltages and, if they differ, imbalances the current distribution between the input transistors. If one of the inputs is the sensing comparison voltage, once the second input equals or overtakes the stated threshold, the comparator output changes, indicating this event.

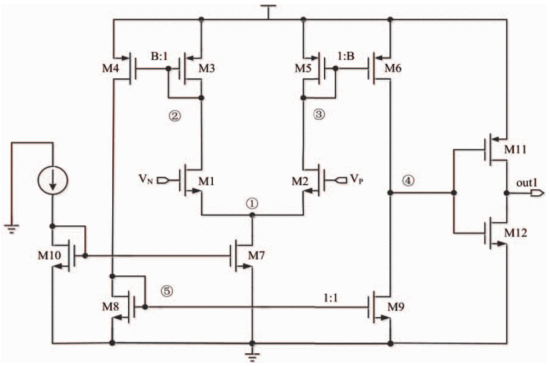
Differential pair comparators are very reliable and multiple architectures may be considered to construct the necessary circuit. Dynamic comparators are good high-speed options, and such a circuit will be revisited for the Time Comparator (TC) in subsection 4.6.1. However, for this application, a continuous analog comparator is needed, where the input signals exist with nonbinary values, and a small change upon voltage crossing is to be detected.

The circuits such as the ones presented in [54], figures 3.15, were tested and even though these are good comparators and meet most requirements, they all lack in speed. The fastest achieved conversion timing is around 100 ps, incapacitating the use of such circuits at the present needed frequency.

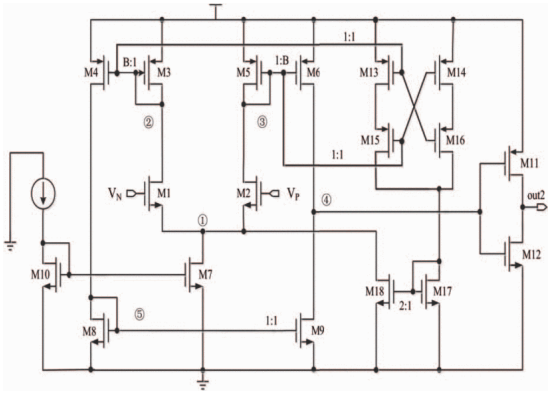
Simplifications may be done knowing that the threshold voltage is fixed or that the output transition will always have the same polarity (the comparing voltage will always start below the threshold voltage, for example). However, none of these changes showed enough of a speed up, for the comparator to have usable timings.



(a) Differential Comparator used in [38]



(b) Conventional differential comparator (from [54])



(c) Proposed differential comparator in [54]

Figure 3.15: Differential comparator architectures.

3.4.2 Inverter

Just as used in all the presented VS VTCs, inverters may serve as comparators. This is, arguably, the simplest and fastest form of threshold-crossing detection. It is a good option for VS VTCs as the inter voltage between the initial and final voltages is always swept. As long as the inverter threshold is in between said voltages the result will be the same with minimal impact upon threshold change. However, problems may arise if a CS VTC is used, as the initial voltage may change and conflict with the inverter's threshold.

Using a simple inverter, whose commuting threshold is $\frac{V_{DD}}{2}$, the input range will be limited to an even lower value, already considering possible problems due to PVT variation or devices' mismatch. It is possible to control the threshold voltage of the inverter, increasing the possible input range, to either higher or lower values, by adjusting the NMOS and PMOS sizes. One way to perceive the threshold

input voltage is to state that the current in both the PMOS and the NMOS has to be the same upon state transition, for the wanted voltage. With this though, equation 3.4 may be reached with some simplifications, considering that $\mu_{n} \approx \mu_{p}$, $C_{ox\_n} \approx C_{ox\_p}$ and $V_{t\_n} \approx V_{t\_p} = V_{t}$. There remains a limitation for the inverter threshold, given by the threshold voltage of the transistors (around 300mV) and, while Ultra Low Voltage Threshold (ULVT) transistors may be used, it comes with an even bigger possible device variation and possible power consumption. This also means that equation 3.4 will become ineffective for values close to the inverter threshold limit.

$$\begin{aligned} I_{n} = I_{p} \Leftrightarrow \frac{1}{2}\mu_{n}C_{ox\_n}\frac{W_{n}}{L_{n}}\left(V_{in} - V_{t\_n}\right)^{2} = \frac{1}{2}\mu_{p}C_{ox\_p}\frac{W_{p}}{L_{p}}\left(V_{DD} - V_{in} - V_{t\_p}\right)^{2} <\approx> \\ <\approx> \frac{W_{n}}{L_{n}}\left(V_{in} - V_{t}\right)^{2} = \frac{W_{p}}{L_{p}}\left(V_{DD} - V_{in} - V_{t}\right)^{2} \end{aligned} \tag{3.4}$$

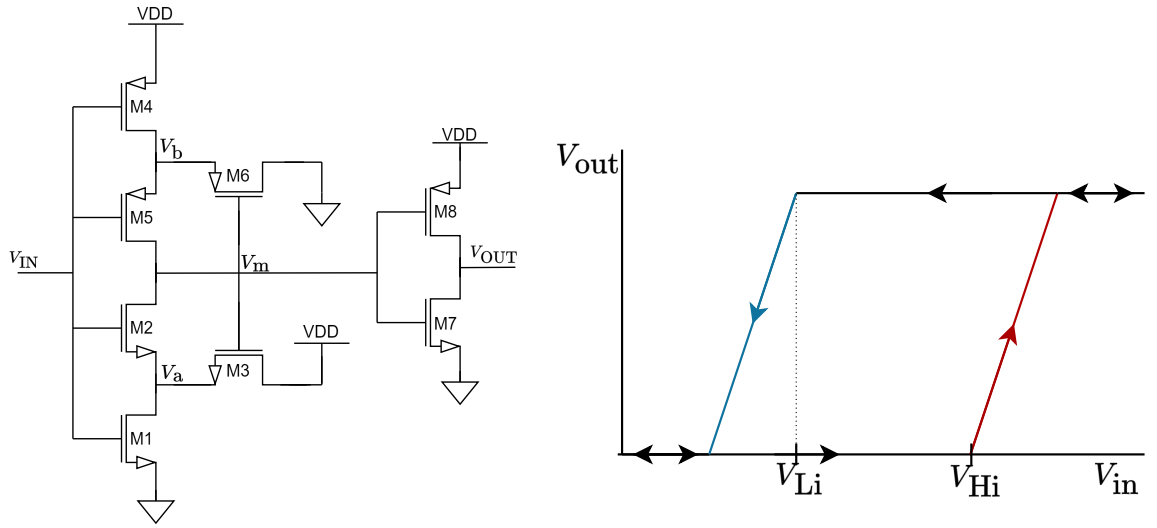
Furthermore, an inverter also shows a high non-linearity in its input capacitance. Because of the change in the transistor's inversion state through the voltage sweep, both the NMOS and PMOS will contribute with different capacitance values for every input voltage. Moreover, if a greater size difference between NMOS and PMOS transistors is used for an inverter threshold change, the capacitance will suffer an even higher difference.

3.4.3 Schmitt Trigger

Based on the inverter, and to better control the threshold defining voltage and its dependency with PVT variations, an interesting circuit is the Schmitt trigger. There are a few versions of this circuit, some using differential comparators, nonetheless, a simpler version using CMOS technology is presented in figure 3.16(a) [55]. It is essentially a comparator with hysteresis, meaning its output depends not only on the present input voltage but also on its previous state. This hysteresis is achieved by positive feedback of the output, reinforcing the output state and reducing the direct influence of the input. This also means that contrary to the single input voltage threshold of the inverter, there will be a threshold for the output to transition from 0 to 1 (V_{Hi}) and a different voltage threshold for the output transition from 1 to 0 (V_{Li}). The DC characteristic is presented in figure 3.16(b).

There are some advantages of using a Schmitt trigger when compared to a simple inverter. First, there is a better immunity to noise and spurious signals. Because of the feedback, there is also an improvement in the switching speed and a better control of the thresholds. Some disadvantages are the more complex circuit with an increase in input capacitance and power consumption, and in extreme cases and bad sizing, the possibility of oscillation.

The equations 3.5 size the transistor to achieve a certain low and high transition threshold (V_{Li} and V_{Hi} respectively) [55]. For simplification consider $K_{x} = \frac{1}{2}\mu C_{ox}\frac{W_{x}}{L_{x}}$, with μ and C_{ox} constant and equal for both the PMOS and NMOS transistors,



(a) Schematic [55].

(b) DC characteristic.

Figure 3.16: CMOS Schmitt trigger.

$$\begin{cases} \dfrac{K_1}{K_3} &= \left(\dfrac{V_{DD} - V_{Hi}}{V_{Hi} - V_t}\right)^2; \\ \dfrac{K_4}{K_6} &= \left(\dfrac{V_{Li}}{V_{DD} - V_{Li} - V_t}\right)^2. \end{cases} \tag{3.5}$$

To better understand the working principle of this circuit consider the following situation. Allow the output $V_{out} = 0$V, the voltage on $V_m = V_{DD}$ and $V_{in} = 0$V. In such an initial condition $M1$ will be in cut-off, while $M3$ puts $V_{DD} - V_t$ in V_a. As V_{in} rises, $M1$ may start conducting, but it will compete with $M3$ to discharge V_a. Only when V_{in} is high enough that the current passing through $M1$ is higher than the one passing through $M3$, will V_a discharge, allowing $M2$ to start conducting to discharge V_m, cutting-off $M3$. V_{Hi}, the value for V_{in} to which this happens, depends only on the sizes relation between $M1$ and $M3$, equation 3.5. For this situation, it is beneficial if $M2$ is as big as possible to discharge V_m as soon as $V_{in} > V_{Hi}$ and $M5$ and $M6$ are as small as possible to reduce the capacitance and therefore the charge in node V_m. Once this transition happens, to revert the output state, V_{in} must now go below V_{Li}, following the same operating logic.

As in the inverter, for this circuit, there is also the same input capacitance non-linearity, aggravated by the doubling of input gates and therefore a higher absolute capacitance. There are also limitations to the threshold voltages, related to the threshold voltage of the transistors, limiting the possible values for V_{Li} and V_{Hi}, and therefore making equations 3.5 improper for input voltages outside this interval. ULVT transistors may also be used, increasing the possible V_{Li} and V_{Hi} range, by worsening the possible variation and power consumption. However, because V_{Li} and V_{Hi} depend only on the same type transistors,

such variance will be less impacted by PVT variations.

3.5 Proposed Voltage-to-Time Converter

Having discussed and tested some possible architectures for the VTC to use, the presented circuit in section 3.3, of a directly differential, single current source, ramp generator, figure 3.12, is the most promising. For convenience, the already present schematic is here reintroduced.

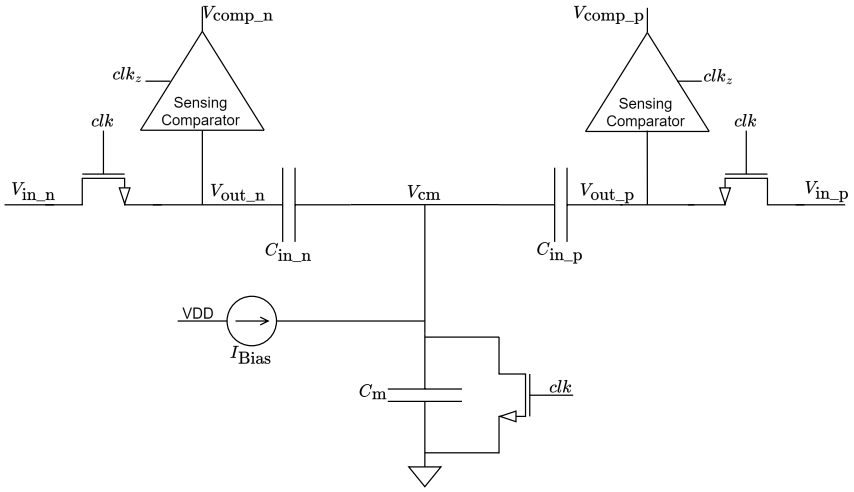


Figure 3.17: Common mode ramp generator voltage-to-time converter [4].

There are a few points that need to be kept in mind when sizing such a circuit, namely the CM voltage for the input signal; the sensing comparators architecture, detecting voltage threshold with its input capacitance; the current source; and the sizes of the capacitors and transistors.

The learned logic for the tested ramp generator VTC, figure 3.10(b), contributed to a good initial understanding of this circuit. As already stated, for the achieved time resolution to be as high as possible, for the situation where V_{in_min} is considered, the final value for V_{out} (V_{out_min}) should be as close as possible to V_{comp}, while still higher to guarantee the comparator's triggering. The value chosen for V_{comp} should also be as close as possible to V_{in_max}, while also higher to prevent the comparator's triggering before the integration process starts. This conclusion can also be mathematically reached by equation 3.6,

$$\begin{cases} V_a = slope \times t_a + V_{a\_i} \\ V_b = slope \times t_b + V_{b\_i} \end{cases} = \begin{cases} t_a(V_a = V_{comp}) = \dfrac{V_{comp} - V_{a\_i}}{slope} \\ t_b(V_b = V_{comp}) = \dfrac{V_{comp} - V_{b\_i}}{slope} \end{cases} \Leftrightarrow$$
$$\Leftrightarrow \Delta_t = \frac{V_{comp} - V_{a\_i}}{slope} - \frac{V_{comp} - V_{b\_i}}{slope} = \frac{(V_{b\_i} - V_{a\_i})\frac{T_s}{2}}{V_{a\_f} - V_{a\_i}} \tag{3.6}$$

where the $slope$ is defined in equation 3.7,

$$slope = \frac{V_{\text{a\_f}} - V_{\text{a\_i}}}{\frac{T_\text{s}}{2}} = \frac{V_{\text{b\_f}} - V_{\text{b\_i}}}{\frac{T_\text{s}}{2}}, \tag{3.7}$$

and Δ_t in equation 3.8,

$$\Delta_t = t_\text{a}(V_\text{a} = V_\text{comp}) - t_\text{b}(V_\text{b} = V_\text{comp}), \tag{3.8}$$

as long as the value for V_comp is in between the range $[V_{\text{in\_max}}; V_{\text{out\_min}}]$. Consider $V_{\text{a\_i}}$ and $V_{\text{b\_i}}$ any pair of input voltages for the chosen range with $V_{\text{a\_f}}$ and $V_{\text{b\_f}}$ their final integrated value. To maximize Δ_t, $V_{\text{a\_i}} = V_{\text{in\_min}}$ and $V_{\text{b\_i}} = V_{\text{in\_max}}$ with the minimum slope resulting in the lowest $V_{\text{a\_f}}$ possible, which should be equal to $V_\text{comp} = V_{\text{in\_max}}$. In this optimal situation a $\Delta_t = \frac{T_\text{s}}{2} = 100$ ps maximum resolution is possible. Realistically, and to provide some error margin, allow $V_\text{comp} = V_{\text{in_max}} + 100$mV and $V_{\text{a\_f}} = V_\text{comp} + 100\text{mV} = V_{\text{in\_max}} + 200\text{mV}$. This situation will result in a maximum $\Delta_t = \frac{T_\text{s}}{4} = 50$ ps.

Regarding the optimal input range, considering the input limitations from the same tested ramp generator VTC circuit, and because a simple NMOS transistor is used for the sampling, the voltages should be as low as possible. Therefore a CM voltage of 100mV is to be considered, having the input range be $[0; 200]$mV for either single-ended signal.

The size of these input sampling transistors is so that the RC filter it constitutes with the input capacitance, will have a frequency pole where the error to a unitary step response is lower than $\frac{1}{4}$ LSB $= \frac{1}{4}\frac{1}{2^n} = \frac{1}{2^{n+2}}$, the chosen error acceptable for this sampling circuit step. Equation 3.9 can be followed to determine the resistance needed for such a device,

$$w_\text{p} = \frac{1}{R \times C} = \frac{\ln\left(2^{n+2}\right)}{\frac{T_\text{s}}{2}} \Leftrightarrow R = \frac{1\frac{T_\text{s}}{2}}{C \times \ln\left(2^{n+2}\right)} \tag{3.9}$$

from which the transistor size is derived.

To size the capacitors, equations 3.2 and 3.3 should be revisited. The situation where $C_\text{p} = 0$F, or at least where its value is small and the variance almost non-existent, would be ideal. However, from the conclusion on the sensing comparator's section (3.4), such is extremely difficult to achieve. Depending on the chosen architecture for the comparator, C_p's value and its non-linearity will strongly affect both the $\frac{V_\text{out}}{V_\text{m}}$ relation and C_eq, impacting the integration process. While minimizing C_p should still be a main objective, the constraints it causes should be kept in mind for the sizing of C_m and C_in.

Because C_m is only present in equation 3.3, a larger value is beneficial. It does not prevent C_p from impacting the current source's perceived capacitance (C_eq), but shortens its relative value variation by making its absolute value larger. A larger C_eq will also translate to a higher current, and therefore a larger power consumption, meaning a C_m increase is still limited.

Regarding the sizing of C_in, because this variable is present in both stated equations, there are two

situations to consider. From equation 3.2, for V_{out} to reach V_{comp} before V_{cm} lead the current mirror out of saturation, $\frac{C_{\text{in}}}{C_{\text{in}}+C_{\text{p}}}$ should be as close to one as possible. For this situation a large C_{in} is beneficial. On the other hand, and from equation 3.3, any variance from C_{p}, due to its non-linearities, will be minimized if a smaller C_{in} is used, due to the series of these capacitors. This concludes on a needed balance between these two effects to reach the optimal value for C_{in}, once C_{p} and its variation are defined.

In section 3.4, comparator architectures were studied, concluding on the difficulty of achieving both a fast comparison timing and a small, linear, input capacitance. Inspired by the Schmitt trigger concept, subsection 3.4.3, the idea presented in figure 3.18 was reached for a fast, low input capacitance option, suitable for the current situation.

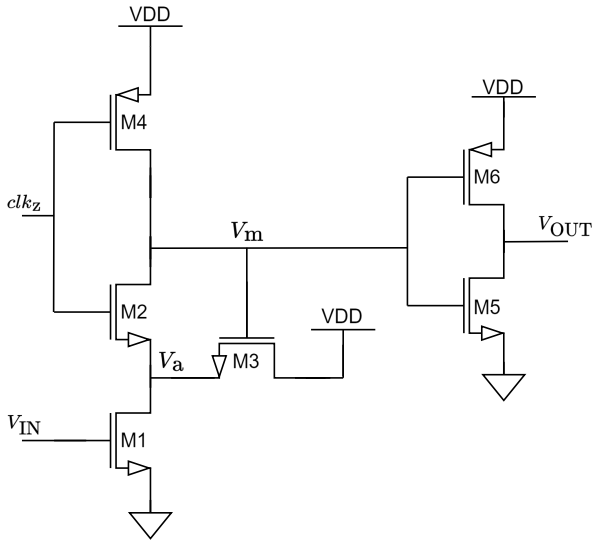


Figure 3.18: Simplified version of a Schmitt trigger CMOS schematic for the proposed sensing comparator.

In a first architectural change, starting from the presented in figure 3.16(a), the clock was introduced. As only $M1$ and $M4$ are relevant for the threshold definition, along with $M3$ and $M6$, $M2$ and $M5$ can be indexed by the clock to synchronize the output. Furthermore, for the chosen VTC architecture, V_{out} will always start below V_{comp}, and only the rising detection is required. Therefore, only the V_{Hi}, defined by $M1$ and $M3$, is needed. The PMOS part can be removed and the clock can reset the circuit without V_{in}. Because V_{comp} was set to 0.3V, there is the need to use ULVT transistors for $M1$ and $M3$ ($\text{V}_{\text{t}} \approx 0.15$V), and relation of $K1/k3 = 11.11$ from equation 3.5. In reality, the necessary relation is $K1/k3 \approx 16$ because such sensing value is close to the limit value of the equation veracity. This circuit not only allows a fast comparison, with a delay between input threshold crossing and output 50% rising of around $23ps$, as well as, because V_{in} only connects to one transistor, a small and low varying input capacitance, with its value in the range $[1; 1.5]$fF.

With a value interval for C_{p} it is possible to arrive at values for C_{m} and C_{in}. After simulation results, and already considering corners, the values of $C_{\text{m}} = C_{\text{in}} = 40$fF were concluded. These presented the

best results, not reaching incomprehensible capacitor sizes.

With all the capacitor sizes, the equivalent capacitance can be calculated, and equation 3.1 can be used to achieve the necessary current, allowing for the sizing of the current mirror and the current steering transistor. With equation 3.9 the input transistors can be determined.

All these theoretical values were slightly adjusted, following the results achieved by the simulations. The main changes were a higher needed $V_{\text{out\_min}}$ to allow the necessary time for the comparator to trigger and drive the following buffer to transition, propagating the generated signal. This also meant a slight increase in the current.

Figure 3.19 presents the time evolution of some signals throughout six periods, allowing the full comprehension of the circuit working mode. The results reached are presented in table 3.1. The comparators output signal ($V_{\text{comp\_n}}$ and $V_{\text{comp\_p}}$) appear in the time interval of 67 ± 18.2 ps after the falling edge of clk, resulting in an achieved time resolution of 36.4 ps, lower than the 50 ps theoretical maximum calculated.

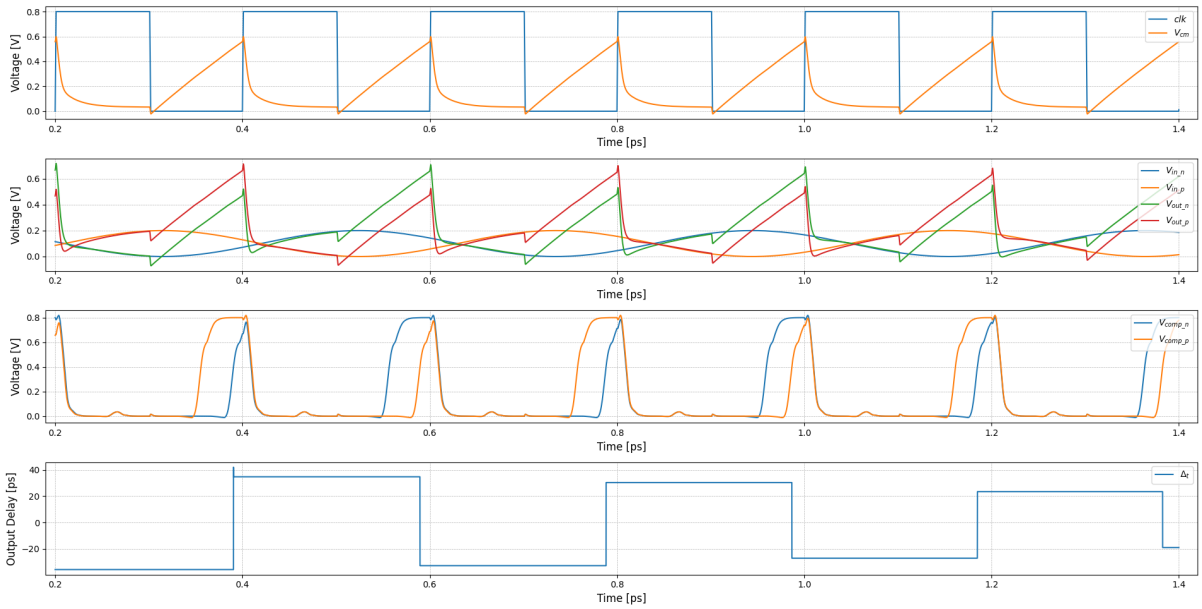


Figure 3.19: Transient analyses of the proposed voltage-to-time converter throughout six periods.

$t(V_{\text{in\_max}})$	$t(V_{\text{in\_min}})$	Δ_{t_max}	SFDR	SNR	SNDR	THD	ENOB	P
48.8 ps	85.5 ps	36.4 ps	50.71 dB	64.36 dB	50.17 dB	-50.34 dB	8.04 bit	606 μW

Table 3.1: Final results for the proposed voltage-to-time converter.

Simulating the circuit in corners, a maximum worsening variation of 11.5% to a THD $= -44.8$dB for the lower temperature, higher voltage, faster PMOS, and slower NMOS. On the other hand, some corners improved the circuit results, reaching a 24.9% increase to a THD $= -63.2$dB in the opposite situation. The average expected THD is $\mu_{\text{THD}} = 50.3$dB with a variation of $\sigma_{\text{THD}} = 3.6$dB.

The resultant time resolution also suffered and benefited in some corners, ranging in values $[33.8; 37.7]$ ps with $\mu_{\Delta\_t} = 35.96$ ps and a variation of $\sigma_{\Delta\_t} = 1.18$ ps. The worst results are present for the corner in the same characteristics as the worst THD corner only with higher temperature.

Running Montecarlo simulation, with 330 runs using sigma amplification, a smaller THD variation is seen, when compared to the presented corners results, with $\mu_{\text{THD}} = -49.96$ dB and $\sigma_{\text{THD}} = 0.65$ dB being reached. As for the time resolution, the variation is steeper, with $\mu_{\Delta\_t} = 36.17$ ps and $\sigma_{\Delta\_t} = 2.06$ ps.

In this chapter, multiple VTCs architectures were studied. Some VS designs were presented with their main problems being related to linearity. The CS options show an improvement in this regard and the proposed architecture, in figure 3.12, is the schematic reached. The sensing comparators were discussed as a crucial circuit, and, based on the Schmitt trigger CMOS circuit, the schematic presented in figure 3.18 is the proposed sensing comparator to use. With a low input capacitance and fast decision times, it suits the application. The reached circuit's simulation results are presented in table 3.1. Such a circuit also shows a small variance and robust operation when corner and Montecarlo simulations are considered.

4

Time-to-Digital Conversion

Contents

As introduced in chapter 2, subsection 2.3.1, and as shown in figure 2.2, once the information is encoded into the time domain, a circuit able to translate it to a binary word representation is the following step in an TD ADC. Like in the voltage domain, where the binary word may be reached by different algorithms and circuit architectures, in the TD multiple time-to-digital conversion techniques may be considered. Some of these techniques are inspired by voltage domain ADCs while others are new architectures and ideas.

The following sections will provide an overview of some TDC architectures, explaining their working modes, advantages, and disadvantages. The goal is to arrive at a possible architecture to use for the present work, given the result and seen limitations from the proposed VTC.

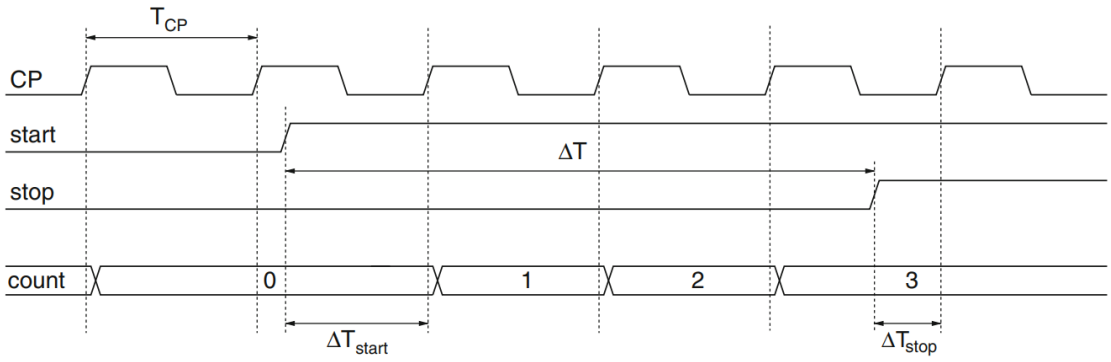
4.1 Counter Type Time-to-Digital Converter

Arguably the simplest form to measure time is to use a counter. By using a clock to increment a count, for the duration of the time interval between events, a binary representation of said time distance is achieved. With this concept, an increase in resolution comes at the cost of adding extra bits to the counter; with a possible increase in the frequency of the used clock, if the maximum conversion time window is kept the same. Furthermore, the frequency of said clock also defines the quantization error (time quantization), as a faster clock will allow for a finer quantization. The idea for the working principle of such circuits can be seen in figure 4.1(a).

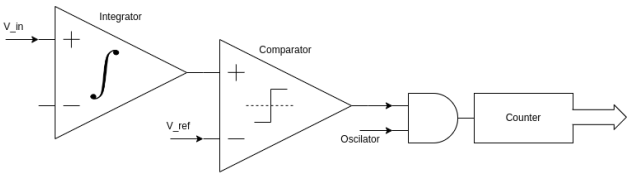
One of the first architectures to use this concept is explored in [56], with the single slope ADC [34]. This circuit is presented in figure 4.1(b). As the first step, the integration of the input voltage is performed, with its value being compared with the reference voltage. This is, in fact, a VTC circuit that controls a counter. While the integration value is lower than the reference voltage, the count increases. The lower the input voltage, the slower the integration will take, resulting in a higher count. A logic circuit may be added to invert the used representation to a more logical counting style that increases proportionally to voltage. Alternatively, a ramp ADC can be used, where the integration signal to integrate is the reference voltage, which in turn is compared to the input voltage. This change will increase the input swing, even to negative values, but worsen the noise tolerance with the non-integration of the input signal.

An improvement to these architectures is to use a double slope ADC, figure 4.1(c). The integration of the input voltage is done for a fixed time and then a reference voltage is used to discharge the capacitor and bring the voltage to 0 at a fixed rate. The time taken to reach the ground value is dependent on the voltage reached during integration, which is in turn proportional to the input voltage. The discharging period is used to increment the count. This makes the operation duration more time constrict and allows for a better noise tolerance. The extra possible circuit to invert the count logic is no longer needed.

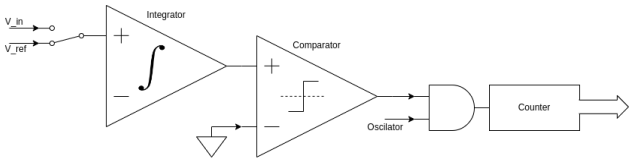
Such architectures are used in high-resolution, low-frequency situations, where there is time to count



(a) Principle of a counter-based TDC (from [6]).



(b) Single slopeADC block diagram.



(c) Double slopeADC block diagram.

Figure 4.1: Counter type time-to-digital converter.

to high values without the need for very strict constraints on the clock frequency, resulting in a good noise tolerance, due to the integration process. However, once the time needed to be measured is at the pico-second level, there is a more complex operation and loss of efficiency. Examining the goal of 7 bit at 5 GHz, a clock of 640 GHz ($2^7 \times 5 \times 10^9 = 6.4 \times 10^{11}$) would have to be used to index the counter, which is an impossible value to use. For such situations, other architectures ought to be explored.

4.2 Flash Type Time-to-Digital Converter

A way to increase the measurement resolution beyond the maximum feasible clock frequency means that each clock cycle has to be sub-divided asynchronously to generate more than 1 bit. Inspired by the voltage flash ADCs, with their conversion speed and simplicity, the flash time domain converters are an option for the implementation of a TDC, that performs exactly that. The time domain flash ADC

presented in [5] presents an interesting view, as one of the first ideas for this concept of time usage in flash ADCs. It uses reference voltages to index multiple VCDUs, and compare the time delay of each one of those with the delay from the input voltage VCDU. The working principle is the same as the voltage flash ADC, only using VCDUs and TCs instead of voltage comparators, 4.2.

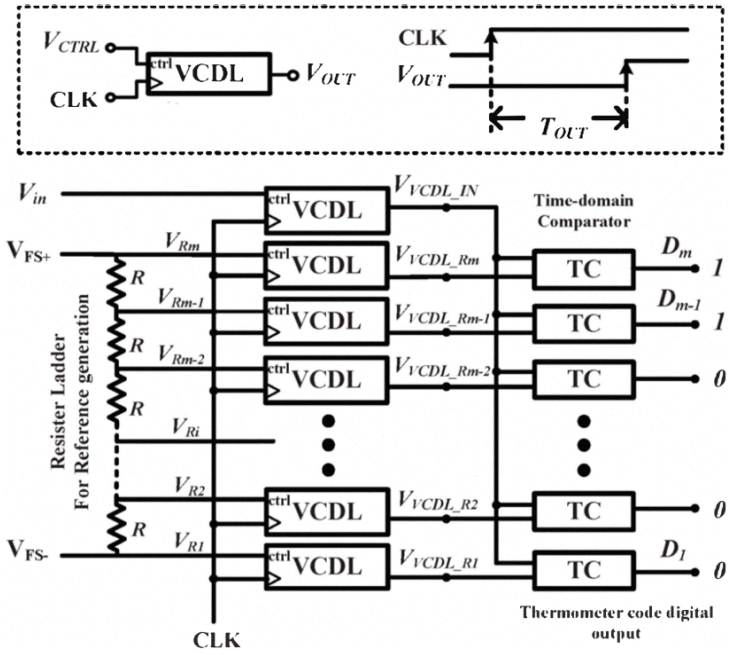


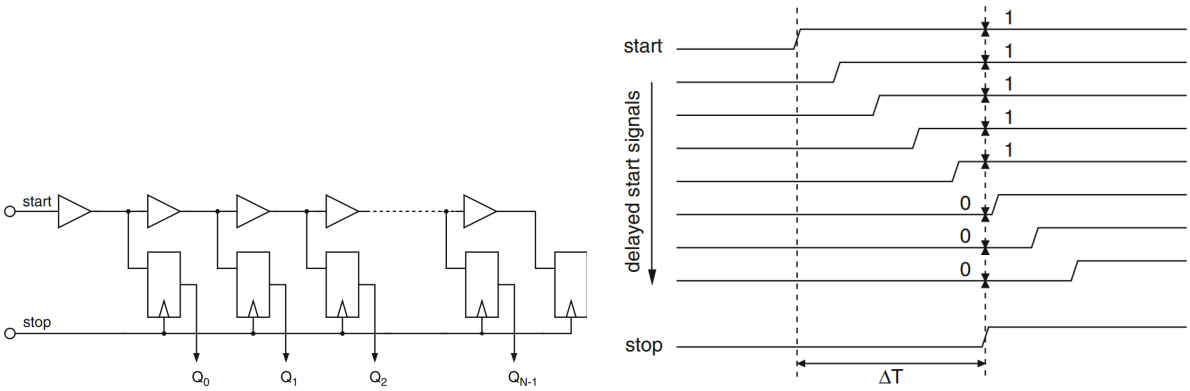
Figure 4.2: Simplified architecture of the time-domain Flash analog-to-digital converter (from [5]).

Later on, the idea evolved into other architectures, such as the simple, fully digital, delay line, figure 4.3(a). This circuit receives the start event as an impulse that will propagate through a delay line of buffers, serving as the input to logic gates such as flip-flops. The end event will act simultaneously on every logic gate, sampling the input value present at the time. The working principle can be seen in figure 4.3(b). This circuit will generate a thermometer code where more active flip-flops reflect a greater time interval between the start and end events. Recent architectures take advantage of this concept to achieve state-of-the-art performance, as in [20] by using oversampling and noise shaping techniques, or as in [21] using interpolation techniques.

The first limitation encountered in this architecture is the delay of each buffer, as a better resolution requires more flip flops and, for the same conversion time, a smaller delay unit in each step. To help this problem an inverter can be used in place of the buffers, reducing the delay in half by detecting not when a flip-flop passes from '1' to '0' (1111|0000) but when the sequence is inverted (1010|0101).

For long delay lines, problems related to the clock skew can start to appear, needing the inclusion of a buffered clock tree to minimize the clock mismatch between flip flops.

To overcome the gate delay limits in resolution, different architectures were explored. A Vernier line, figure 4.4(a), is similar to the simple delay line architecture, but there are delays applied to both the



(a) Block Diagram. **(b)** Working principle.

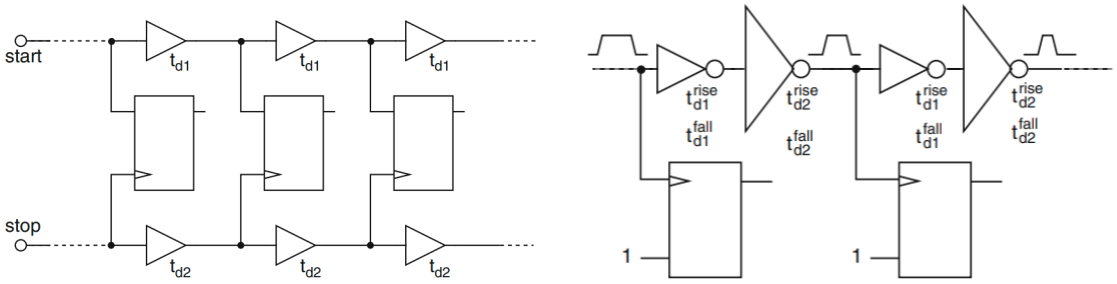
Figure 4.3: Delay Line time-to-digital converter (from [6]).

start and stop event signals. The stop event does not act simultaneously in the flip-flops, instead, it will propagate through a delay line, with a smaller step delay, chasing after the start event signal. With the stop event not implying an immediate ceasing to the conversion process, the signals continue to propagate through the delay lines for the time needed for the stop event to catch the start event. This architecture tends to need more time and, generally, longer lines. However, the time resolution achieved is proportional to the step delay difference between the start and end events delay lines, reaching sub-gate delay timing resolution [57].

Another alternative is the pulse-shrinking TDC, figure 4.4(b), which consists of creating (or already using from the VTC) a square wave active during the start and end event. The duration of the pulse will be decreased by a certain, fixed, amount in every step until it vanishes completely. Detecting the disappearance of the pulse leads to the comprehension of the period of the pulse and, therefore, a binary word can be generated in accordance [58]. The decreasing time, applied to the pulse may be a subdivision of a gate delay, allowing for very precise sub-gate delay resolutions. However, even if this architecture is defined, generally, as a flash type TDC, most of the time it also makes use of counters to keep track of how long the pulse takes to disappear [59], leading to the limitation of frequency previously experienced.

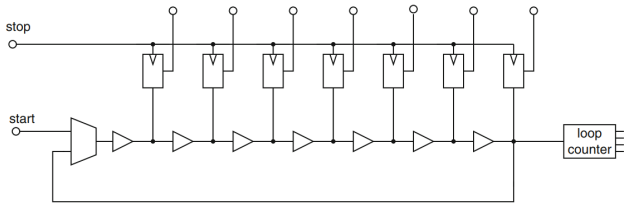
There remain problems, similar to the ones suffered by the voltage flash ADCs, of an exponential increase in size, and power consumption, with an increase in bit resolution. Time folding techniques can help reduce the system size by increasing the circuit complexity, figure 4.4(c). These techniques consist of a looped architecture, where the input of the delay line is controlled by a Multiplexer (MUX) that either selects the start event signal or the feedback of the delay signal from the end of the line to its beginning. An extra counter keeps track of how many times the signal has restarted and serves as a coarse value,

with the normal flip-flop thermometer code as a fine value for the quantization. There also needs to exist the inclusion of a control circuit to clean the delay line and to index the MUX. Nonetheless, a trade-off between conversion frequency and resolution makes these architectures limited in one of these realms, not being very efficient in a general increase in performance. Furthermore, the voltage flash ADCs' problems of sparkle codes and metastability are still possibilities and also constrain the operation of flash TDCs.



(a) Vernier TDC.

(b) Pulse-Shrinking TDC.



(c) Principle of looped TDC architecture.

Figure 4.4: Advanced flash time-to-digital converter architectures (from [6]).

4.3 Successive Approximation Register Time-to-Digital Converter

A SAR TDC working mode, just as the voltage domain SAR ADCs, referred in 2.2, are based on a binary search, testing bit by bit until the value of the two used signals converges. On the voltage domain SAR ADCs, one of the signals is the input voltage, and the other is the result of the DAC to the present output binary word. These two signals are then compared and voltage subtraction is performed until the two voltages are as similar as possible for the resolution in use. When considering the time domain, the storage and manipulation of the signals is impossible, therefore such an algorithm must be performed by adjusting and comparing delays as the signals propagate through the TDC line. The main SAR TDCs conversion algorithm consists of applying two different delays to each of the start and end signals, comparing the time relation between them, and scaling those delay differences along the conversion

process [16].

There are slight differences in the algorithms used in different architectures. As an example, delays may always be applied to both start and end signals [4, 23] or just to the first signal to arrive at the comparator [60]. Nonetheless, the principle is always similar.

In figure 4.5 there is a looped unrolled version of a SAR TDCs. The two input signals will propagate through two different delay lines, each. These signals are also time compared to detect which arrived first. To the signal that appeared first, the comparator will index the respective MUX so that the delayed signal to propagate will be the one coming from the more delayed line. On the other hand, the signal that the comparator understood to have reached last will have its MUX indexed so that the propagated signal has a smaller delay. By doing so, the two signals' time difference will be subtracted by the delay lines' delay difference. In the following stage, the same will happen, only with a smaller delay difference between lines, ideally half of the delay used in the previous stage. And so will be done N_b times using the time comparators' decisions as the result output bits.

Figure 4.6 is a time diagram exemplifying the circuit's algorithm. In the first stage, the signal 'P' arrives first when compared to the signal 'N', which arrives $D1$ units of time later. The comparator in the first stage will index the delay line's delay selection to be higher ($t1_0 = 2t_{inv} + 2^{N-1}t_{LSB}$) for the first arriving signal 'P', while the second signal 'N' will suffer a smaller delay ($t1_1 = 2t_{inv}$). Comparing with the circuit in figure 4.6, the 'P' signal that will propagate through the first MUX will be the one from the lower delay line, the one with the capacitance in the middle node and therefore with a higher delay. On the other hand, the 'N' signal that passes through the upper delay line will be the selected by the MUX. One of these decisions, in this case, the decision on the 'N' side, will be interpreted as the comparator result, propagating to the output binary word. The delay difference between the signal's delay line will result in a time spacing between 'P' and 'N', when entering the second stage, of $D2$ units of time, having approximated the two signals by a time interval of $\Delta_1 = D1 - D2 = t1_0 - t1_1$. In the second stage, the same logic applies: the comparator outputs a '1' representing the control bit for the 'N' signal, which still arrived later and therefore is less delayed than the 'P'; and the two signals are approximated by $\Delta_2 = D2 - D3 = t2_0 - t2_1$. However, because $\Delta_2 > D2$, the signals will swap their relative time position, resulting in the third stage's comparator deciding symmetrically, outputting '0', and therefore delaying the 'N' signal more than the 'P'.

As it happens on the vernier delay line, this architecture allows for a sub-gate delay by not being dependent on the cell's minimum delay, but rather on the delay difference between lines.

Another alternative, used to reduce the number of delay buffers is the one presented in [4]. Here Selective Delay Tuning (SDT)Cells are used to implement a different delay based on the comparators result. So instead of the comparator indexing a MUX that chooses which line to propagate, there is only one delay line for each signal and a cell whose delay is tuned to differ depending on the value of the

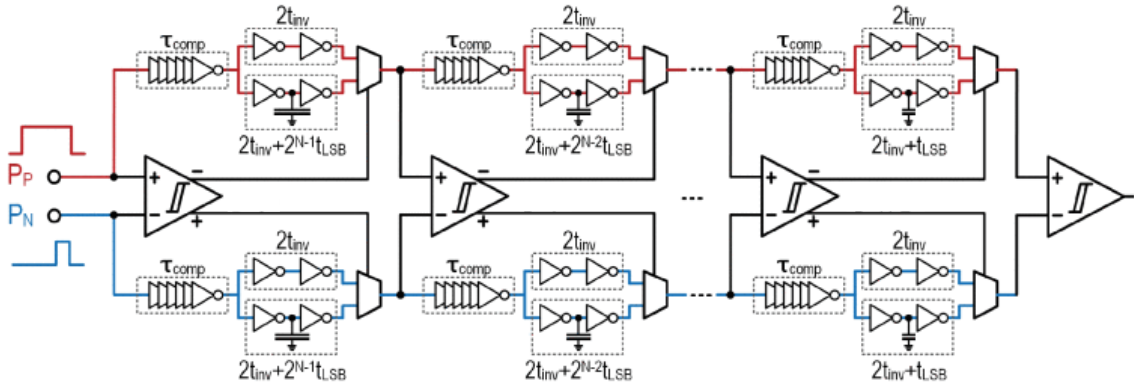


Figure 4.5: Loop unrolled successive approximation register time-to-digital converter (from [4]).

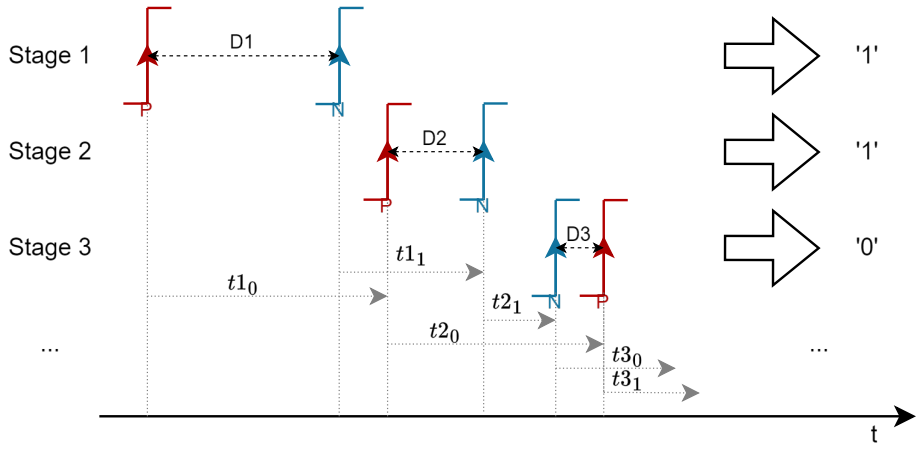


Figure 4.6: Time diagram exemplifying the successive approximation register time-to-digital converter algorithm.

control signal given by the comparator.

4.4 Ring Oscilator Time-to-Digital Converter

A ring oscillator is a simple digital circuit composed of inverters looped around a chain, figure 4.7. The chain may contain a combination of inverters, non-inverting buffers, differential or non-differential amplifiers, feedthrough cancellation circuits, or even some control logic circuits. As long as the number of inverters is odd, a constant oscillation through the line is present. Using such a circuit enables the use of techniques where the phase of the propagated signal through the line contains and translates into a binary word representing the delay between events. Multiple paths [19], or multiple injections of the start signal into the line, in either one or more places at once, are alternatives that can be explored to achieve measurements that translate into bits, representing the delay between the start and end events.

These TDCs architectures can be seen as an evolution from the delay line using inverters, taking

advantage of time folding techniques [17]. It also enables the use of oversampling by sampling the propagation phase of the inverters multiple times and performing either interpolation and/or decimation to obtain a more realistic and true measurement, increasing the SNR and decreasing the time resolution obtained to sub-gate delay values.

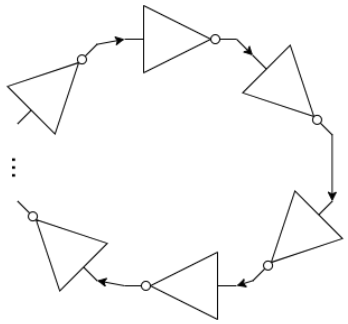


Figure 4.7: Simple Ring oscillator.

This is a very promising architecture with state-of-the-art results reaching medium resolution with reduced power consumption, limited by the frequency of operation and circuit complexity [18].

4.5 Hybrid Architectures

As previously mentioned in subsection 2.2, the conversion process can be divided into multiple steps to reduce the complexity of each individual step, increasing the resolution and the operation frequency. When referring to TD converters the same idea can be applied, having a combination of one or more architectures used in different conversion steps. These TDCs are called hybrid and can be divided into two categories: Voltage ADCs followed by TD ADCs or ”Pure” Time Domain ADCs.

The concept remains the same in both scenarios: a first step called a coarse ADC, generates the most significant bits. The residue is then used to generate a signal that can be utilized by the following step, a fine value ADC, to achieve more, less significant, bits. The bits generated in each step can be disjoint, where a simple concatenation of bits is enough to come up with the final word; otherwise, if the bits overlap, an additional circuit, to correct and align the bits, must be used.

In case a Voltage ADC followed by Time Domain ADC is in the study, the first step of the conversion is still done in the voltage domain, the residues can be determined and translated into the time domain by, for example, detecting the comparators' commutation delay or by use of a VTC with the, possibly amplified, residue voltage [30]

If a ”pure” TDC is in use, each step may be separated by a TA, not needing any analog block or a VTC in between steps.

These systems are the most recent advances in analog-to-digital converters and present state-of-

the-art power consumption and operation frequency, with still up to medium resolution [37]. Hybrid architectures can convert signal in the GS/s frequency range, such as the presented in [4, 23, 26–28], consuming power below the μW line [24, 25], while still generating above 11 bit [29, 30] for lower frequencies.

4.6 Proposed Time-to-Digital Converter

Considering all the stated architectures, the SAR alternative seems to be the most suitable for the present project, achieving a reasonable complexity, frequency, and resolution, ideal for the project in hands. Pipeline techniques will also be applied to achieve the necessary throughput, but no TA or time residue generator are to be projected.

Following the presented in [4], the use of a single delay line for each of the signals, by employment of SDTCells, is to pursue looking for the stated reduction of size, power consumption and delay mismatch in corners and Montecarlo. However, contrary to the presented in the refereed paper, instead of a 3-bit coarse flash TDC followed by a 5-bit SAR TDC, only a SAR TDC, with 7 stages, will be tested.

As detailed in section 4.3, the algorithm used may have its operations divided into 4 main circuits. There needs to exist a TC, to assess the input signals arrival order, subsection 4.6.1. While the time comparison takes place, the signals will pass through a delay line. These delayed signals will then enter the SDTCells, already with the comparator output, the control bit, available, approximating the two signals in time, subsection 4.6.2. Once the stage decision is made and the signal propagates to the following stage, the following signal may enter that same stage, allowing pipelining. Therefore a control circuit, to generate the clocks for each stage is needed, subsection 4.6.3. Finally, registers to sample and hold the comparator decisions are required, grouping and synchronizing all the stage-generated bits, subsection 4.6.3. All these blocks will be explained in detail in the following subsections, explaining the encountered problems and found solutions.

Figure 4.8 can be considered as the proposed architecture, with figure 4.9 a simple initial version of each stage.

The architecture is custom-designed for the achieved proposed VTC, following its output Δ_{t_max} and delay between clock and output signals. Therefore, table 4.1 explains the delay lines' time difference each stage introduces between the signals. Each stage will delay half of its maximum delay input, halving the maximum delay of the following stage. The sixth stage delay is the lowest introduced delay, being considered as the LSB delay value. The seventh and last stage does not introduce delays, only compares the received signals to generate an output bit, the LSB.

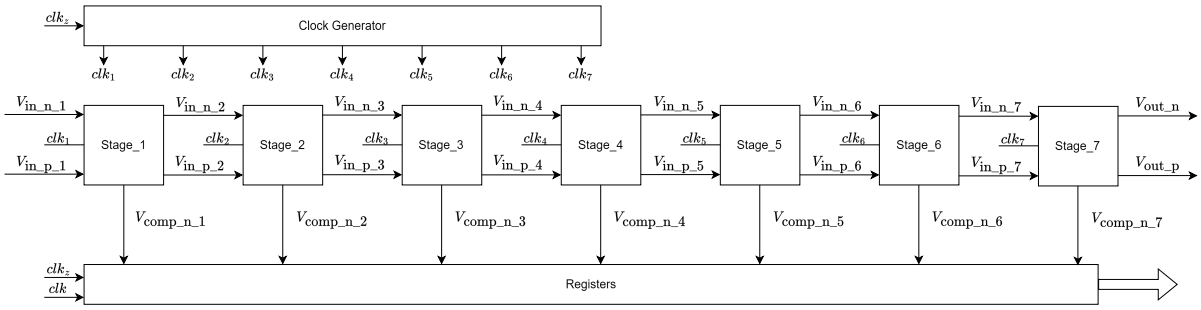


Figure 4.8: Block diagram of the proposed successive approximation register time-to-digital converter architecture's top view.

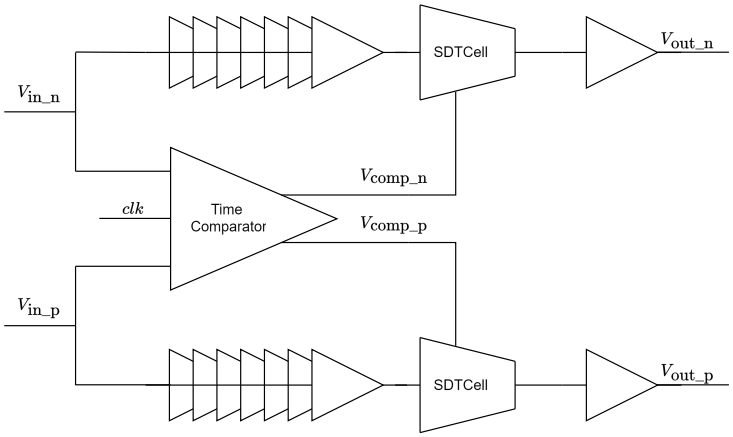


Figure 4.9: Initial block diagram of each stage.

4.6.1 Time Comparator

To decide the signals' relative time appearance, concluding on which signal should be more or less delayed, a TC is needed. As stated in section 3.4, and because the necessary characteristics for the present comparator do not require it to be continuous, a dynamic comparator may be considered, improving its possible speed. Figure 4.10(a) shows the comparator architecture used. It is a simple, and therefore fast, circuit, achieving the result characteristic presented in figure 4.10(b). Because of the circuit symmetry, only half of the characteristic is shown, measuring the time the respective output goes to the ground, the most time-consuming scenario.

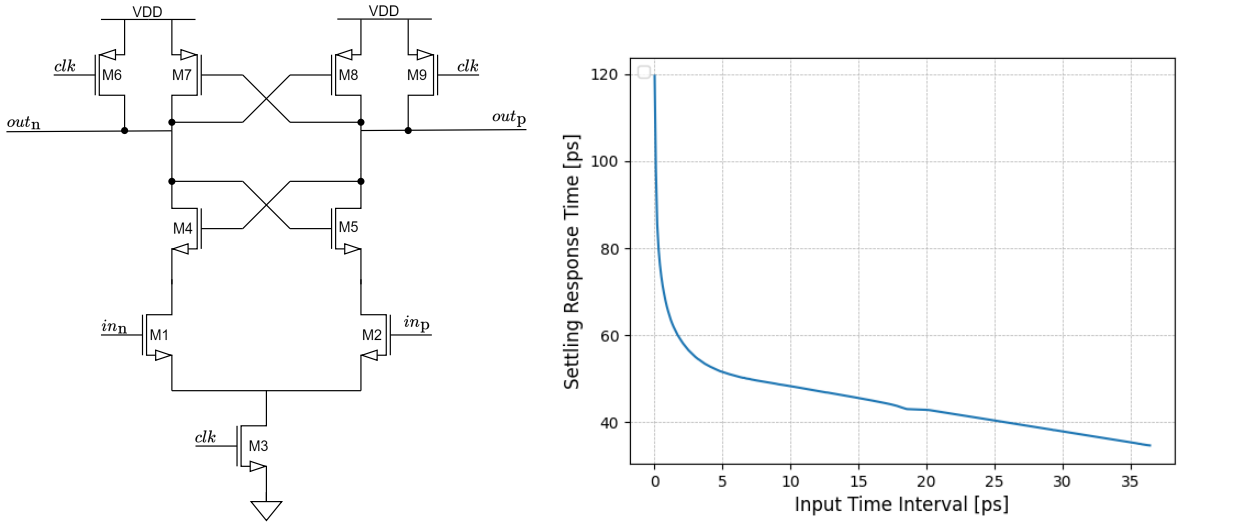
Initially, the comparator is reset with the clock, disconnecting the input transistors ($M1$ and $M2$) from the ground and charging the output nodes (out_{n} and out_{p}) to V_{DD}. Once the clock goes to 1, the circuit is left in an unstable situation. The first input signal to enter the comparator will start discharging its respective output node. The feedback loop cuts off the opposite node from discharging while also connecting it to V_{DD}.

A minimum delay between input signals of $100fs$ is here deemed as acceptable, generating a correct output value to an interval below $\frac{1}{5}$LSB, in less than $80\%\frac{f_{\mathbf{S}}}{2}$.

Stage	1	2	3	4	5	6	7
Δ_{t_n}	± 18.2 ps	± 9.1 ps	± 4.55 ps	± 2.28 ps	± 1.14 ps	± 568 fs	-

Table 4.1: Delay difference of the delay lines in each stage.

Awareness is needed for the arrival of the clock in relation to the appearance of the first signal. If there is more than $20\% \frac{f_s}{2}$ time difference between these events, such a small input signal time difference may not be correctly resolved by the comparator before reset, making the matching of the clock with the input signals an important operation. Alternatively, if a clock duty cycle higher than 50% is used, allowing more time for the comparator to decide its value before being reset, not only do these limitations become more relaxed but a smaller input signal delay may be acceptable and correctly resolved.



(a) CMOS Schematic.

(b) Settling time to reach 90% in function of the delay between the two input signals.

Figure 4.10: Time Comparator

Three main problems ought to be addressed. There is a non-linear delay introduced to the signals, dependent on their input delay. The second signal arriving at the comparator will encounter the input transistor gate with a different capacitance, dependent on how much time has passed since the first signal arrived. Such a fact does not directly influence the comparator decision but may alter the relative time position of the signals themselves, affecting the following stages. To solve this problem there needs to exist a buffering from the signal that enters the comparator to the signal that continues to propagate through the delay line.

The time at which the output of the comparator is stable before the clock reset is too short to index the SDTCell. This issue is solved by using an SR latch, to detect the comparator's decision. It introduces a larger comparison delay but will keep the decision stable for almost the following full period. It is true

that, if the comparator does not decide in time, because of a small input delay, the SR latch will also not be able to commute its value, keeping the previous state. However, in such a situation, the relative delay between the comparator's input signals is well below the considered acceptable minimum delay, also below the LSB value. Therefore, either decision from the comparator-latch will introduce an acceptable error for the number of bits in use, not adding to the already existing quantization error. Even though the comparator's metastability situation is not a direct problem, the SR latch could also have metastability issues, if the comparator so establishes. Nonetheless, this fact is neglected, and considered as a rare occasion. It is, however, something to improve through calibration.

Lastly, there is an error related to the time the input signals themselves are with a high value at the input of the comparator. In a situation where a small input time difference conditions the comparator to take a longer time to resolve, if the first signal to arrive becomes no longer present at the comparator's input, while the second signal continues actively discharging its node, this second signal may overcome the first one in discharging its output node, resulting in a wrong decision. This situation may happen for input delay differences as large as one LSB. Such may happen in the last stages, given different delays may have been applied to the falling of the signals by the SDTCells of previous stages, reducing the duty cycle of the propagating signals. This issue may be resolved by adding a clock-controlled buffer at the comparator's input. The rising of the comparator's input is still controlled by the signal, however, its falling will only happen with the clock. The used clock in these cells may be the same clock that will reset the comparator. This will introduce non-linearities as different capacitances are present at the input of the clock-controlled buffers, depending on the time between the clock and the signal. Nonetheless, the relative time position between signals will not change and therefore the comparator decision is kept correct. The previously added buffers between the comparator input signal and the propagating signal will also help in isolating these added, non-linear, delay effects.

There is an interesting fact, of a slight increase in the comparators output node capacitance, for the case in which the SR latch has the output of '1'. In this situation, the NAND PMOS transistor to which the comparator output node is connected will have a larger input capacitance, compared to the symmetric scenario. Such a fact introduces a memory-based offset. If a small input delay is considered, this capacitance difference is enough for the first signal to take more time to discharge its node than the second signal, leading to a wrong decision. However, the time interval needed for this to show itself is smaller than the time the comparator has to make a decision, where, even if this error occurs, either output value would be accepted.

4.6.2 Delay Cells

The idea introduced in [4] of using a SDTCell for creating different delays for each of the delay lines takes use of the circuit presented in figure 4.11(a). The idea consists of two inverters, in which the middle point

may also be charged or discharged with auxiliary transistors, depending on the control bit (V_{ctr}). As an example, if $V_{ctr} = V_{DD}$, once V_{in} rises, the node V_{mid} is discharged through both $M2$ and $M5, 6$. If the control bit $V_{ctr} = 0$V, $M6$ is cut off, and therefore V_{mid} only has $M2$ to discharge, taking more time for V_{out} to commute.

By changing the transistor sizes of the output inverters ($M3$ and $M4$), changing the capacitance of the middle node, and by tuning the size relation between $M2$ and $M5, 6$ (and $M1$ and $M7, 8$) it is possible to conclude on different delays between $t(V_{in})$ and $t(V_{out})$, depending on V_{ctr}. The exact values needed are the ones presented in table 4.1.

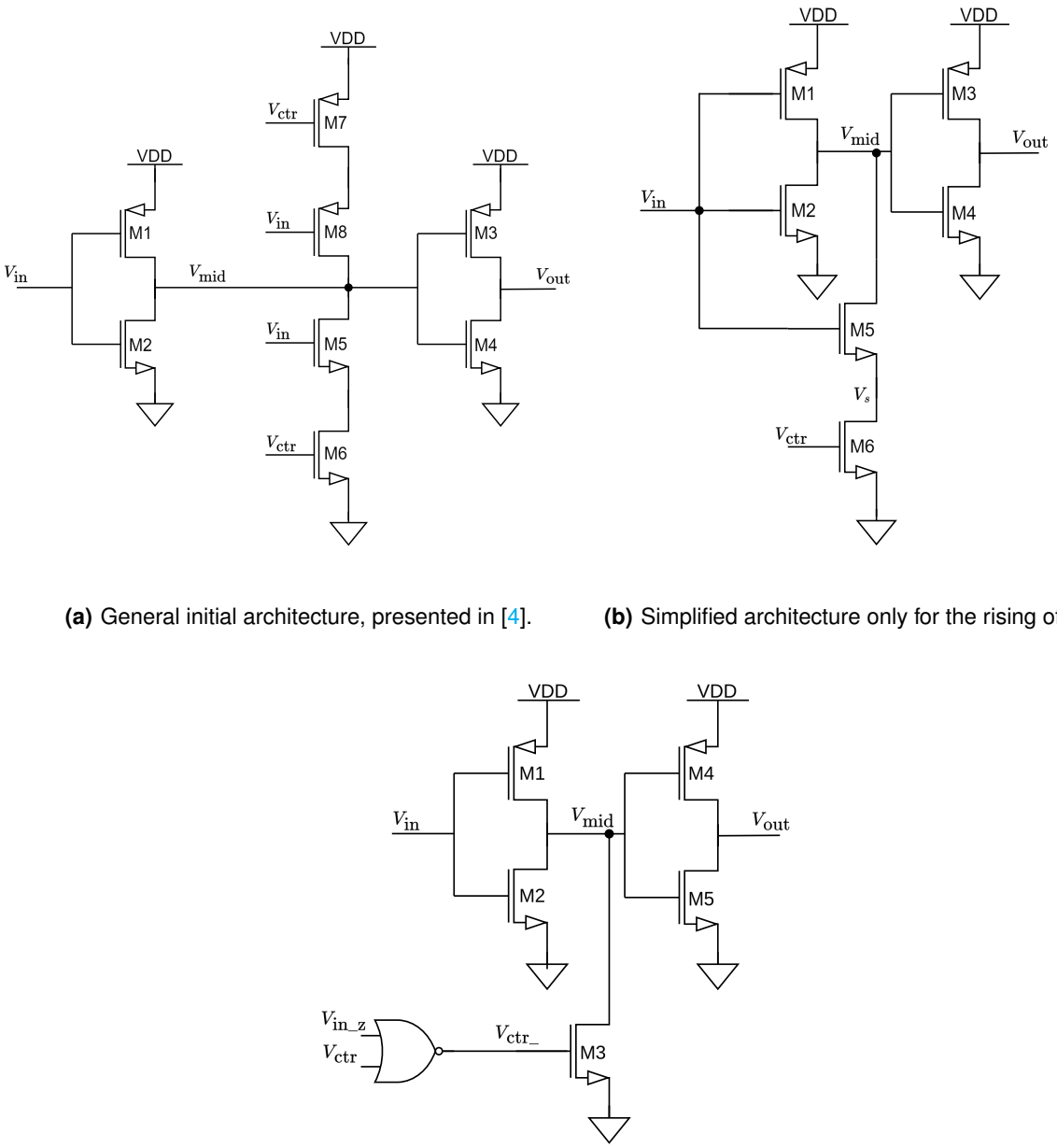
The presented circuit is a general idea, capable of delaying both the rising and falling of V_{in} differently. However, for the presented situation, the information is only encoded in the rising delay of the signals. This simplifies the circuit, eliminating $M8$ and $M7$, reaching the presented in figure 4.11(b). These changes make the circuit smaller as well as reduce the input capacitance for V_{in}.

A smaller input capacitance is beneficial for the situation of a low input voltage at the VTC. As the triggering of the sensing comparator is close in time to the reset of the circuit, the generated pulse will have a narrow time characteristic at a high voltage. If a large input capacitance is met at the input of these cells, the signal may not be propagated, limiting the size of the input transistors that can be used in these cells.

To further decrease the input capacitances, like the performed in section 3.5 for the proposed sensing comparator, the clock could input transistor $M1$, substituting V_{in}, to reset the node V_{mid} synchronously. However, by doing so, not only extra delay lines would be needed to create this signal from the stage's clock, but time dependencies between this clock and the input signals would appear, affecting the cell's delays and adding non-linearities.

Even though the reached circuit in figure 4.11(b) follows the stated logic, there exists an input non-linearity on the generated delay difference between delay lines in excess of 5ps. This is due, in part, to the node V_s, whose voltage will be slightly different depending on the time relation between $t(V_{in})$ and $t(V_{ctr})$. This changes the perceived input capacitance and influences the delay of the cell. Such a time difference, of almost 10 LSBs, is enough to make the circuit unusable, concluding that a different approach is needed.

To try and minimize this issue, the circuit presented in figure 4.11(c) was studied. As the V_{in} arrives at the SDTCell from a delay line, it is possible to use its inverted, earlier, version (V_{in_z}). Using a NOR gate, indexed by V_{ctr} and V_{in_z}, a second control bit ($V_{ctr\_}$), which will input $M3$, is created. With the rising of V_{in}, V_{in_z} has already fallen to ground. If $V_{ctr} = 0$V, $V_{ctr\_}$ will take the value of V_{DD}, allowing $M3$ to help discharge V_{mid}.



(a) General initial architecture, presented in [4].

(b) Simplified architecture only for the rising of V_{in}

(c) Proposed architecture.

Figure 4.11: Selective delay tuning cell architectures.

There may be a mismatch between the delay from $V_{\text{in\_z}}$ to V_{in} when compared to the time it takes $V_{\text{in\_z}}$ to originate $V_{\text{ctr\_}}$. The inverter may be faster than the NOR gate, leading V_{mid} to begin discharging only through $M2$, before $M3$ starts conducting to increase the discharging current. Such a fact would decrease the delay difference between the two V_{ctr} situations. However, given a different mismatch, the

resultant delay would be constant for every input.

There is still a non-linearity source, as $V_{\text{in\_z}}$ will still encounter the NOR gate with a slightly different input capacitance, dependent on $t(V_{\text{ctr}})$. Nonetheless, by taking the input signal from a previous delay line inverter, and passing both signals through buffers before reaching the SDTCell, isolating $V_{\text{in\_z}}$ from V_{in}, a great improvement can be achieved. The impact of the control bit will only be present for the case $V_{\text{ctr}} = 0$V, as only $V_{\text{in\_z}}$ may be affected. The non-linearity source still exists, but its implication is now lower than 1 LSB and only notable for situations where V_{ctr} only became stable very close in time to $t(V_{\text{in\_z}})$ (very small input signals time differences).

Considering the stated architectures for the comparator and the SDTCell, figure 4.12 reflects the concluded block diagram for each stage. Substituting the initial idea from figure 4.9, it solves some of the detected problems and improves on its linearity and metastability issues.

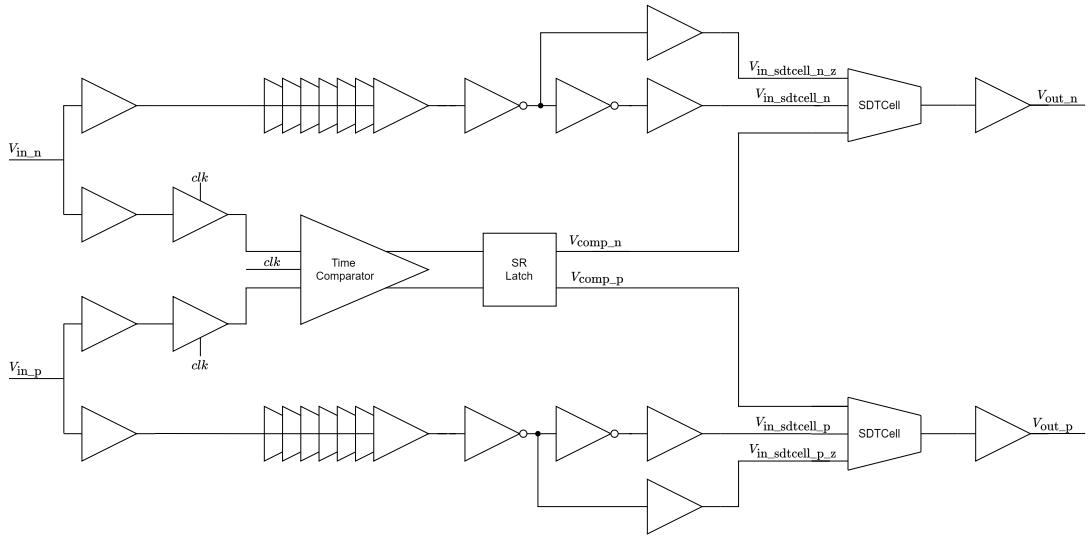


Figure 4.12: Proposed stage architecture.

Still regarding delay cells, and apart from the just mentioned SDTCells, all the buffers and inverters' purpose is to either isolate signals or delay the signals enough time for some parallel operation to take place. This last objective is the intent for the buffers that constitute the delay line from the input to the SDTCells. They need to delay the signal time enough for the comparator-latch to decide and make the control bit available, and stable, for when the signals arrive at the SDTCells. Given the comparator-latch characteristic and the SDTCells requirements, this line was determined to have around 120ps of delay.

4.6.3 Registers and clock pipeline

The last blocks to refer to, from figure 4.8, are the clock generation circuit and the registers. These are simpler, yet crucially important, systems for the used architecture.

Starting with the clock generation circuit, the mentioned awareness of the timing between the arrival of the clock to the appearance of the first signal on the TC, should be revisited. Given the use of a 50% duty cycle clock, for the TC to decide on small enough input signals, the stage's clock has to appear as close as possible to the earliest signals to arrive at the TC.

From the proposed VTC it is known that the first signal to be emitted by the sensing comparator happens 48.8ps after the falling of clk, table 3.1. As the comparator is enabled with a rising clock, the inverted version of clk (clk_{z}), should be delayed at a similar time for the matching of the clock to the signal in this first stage.

After entering a stage, each signal will be propagated through a delay line and then through the SDTCell, suffering an absolute delay dependent on its relative appearance to the other signal. Nonetheless, the timing interval at which the signals will pass from the present stage to the following one is well-defined. The clock that indexes said stage should, therefore, be delayed exactly that timing to index the following stage's comparator at the optimal moment. Objectively, and as also stated in [4], the best way to guarantee this delay, and have it be as constant through different PVT variations and mismatch, is to replicate the operation it wants to mimic as the delay line itself. This would mean using another similar full stage with its comparator-latch, all the delay buffers, and the SDTCells to mimic the delay wanted. However, such would involve the addition of unnecessary devices, consuming way more power, and area, introducing more parasitic and complexity than needed. Using delay buffers will produce a similar result, not as accurate and variation-resistant, but simpler and more effective.

Between each stage, a buffer line will exist, delaying the same stated 120ps for the comparator-latch, plus the adequate SDTCells absolute equivalent delay, to produce the following stage's clock.

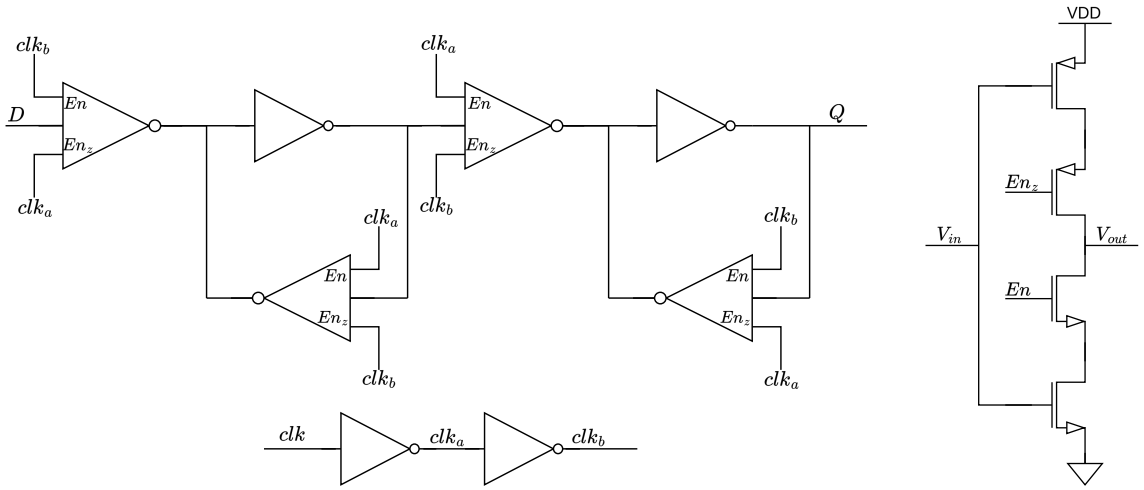
Because this delay is always lower than the period used (200ps), it is possible to pipeline the circuit without any additional components. As soon as the signals are through a stage, the following VTC converted signal may enter and be processed independently of what will happen in the following stages.

The only needed guarantee is that the comparator decision is sampled to registers to keep the decided bit stored until the remaining stages' comparisons take place, and the final binary word is formed, ready to be output synchronously.

As the clocks used in every stage are derived from the main clk, or clk_{z}, either one of these signals' edges may be used to sample the comparator output at the most optimal time.

As for the registers themselves, even with rather relaxed specifications, a fast circuit is still needed. The design presented in figure 4.13(a) was used, with the clocked inverter schematic represented in figure 4.13(b). It is a negative edge-triggered circuit with a small set-up and hold timings, ideal for this application.

Once the information is already on the flip-flops a fully digital circuit is being used. Using a chain of flip-flops to propagate the stages' decided bits until the end, every sampled bit will be synchronized



(a) Flip-flop **(b)** Clocked inverter.

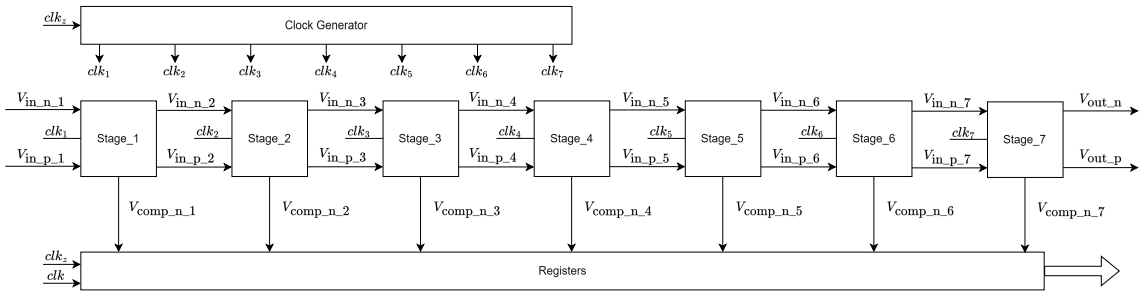
Figure 4.13: Register circuit proposed.

along the way. The final stage decided bit will be sampled and output synchronously as a 7-bit word.

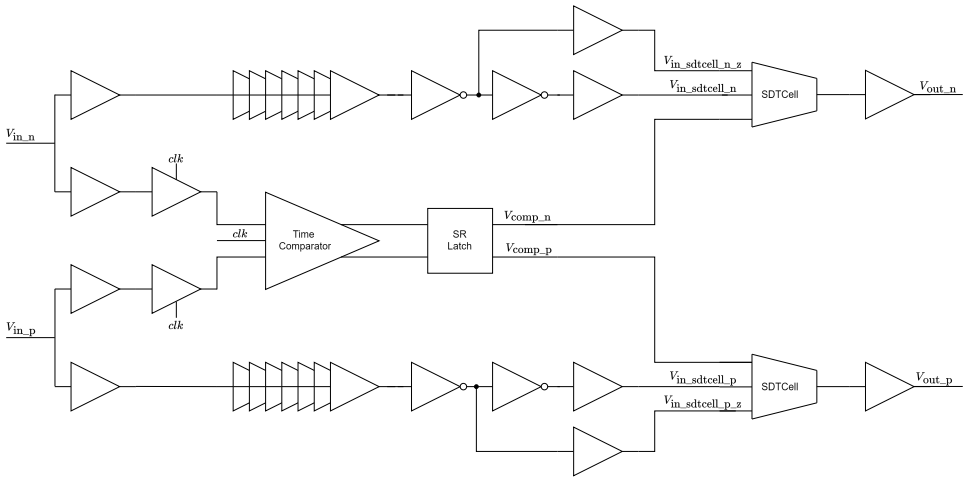
Once the proposed TDC is designed specifically for the proposed VTC the results of the achieved circuit are not here detailed individually. The full working ADC results are presented in the following chapter 5.

After exploration of multiple TDC architectures, a SAR TDC is proposed. Taking advantage of pipelining to achieve the necessary throughput, the block diagram from figure 4.8 was concluded as a top view for the proposed circuit, with the first six stages as the schematic presented in figure 4.12, and the seventh stage only as a comparator. Instead of using two delay lines for each signal, with a decision MUX, SDTCells were used to apply the different delays to each signal propagating through the line, figure 4.11(c). A suitable TC is also proposed, achieving high-speed decisions for input time intervals of 100 fs, referring to some of the circuit limitations and found solutions.

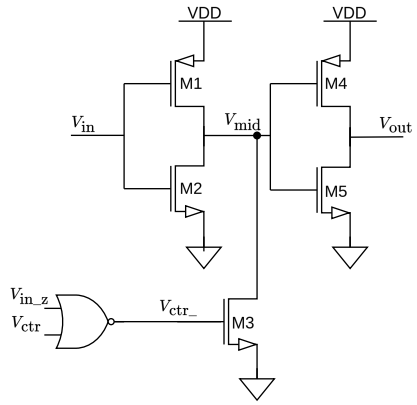
All the proposed circuits are here repeated for convenience, summarizing the reached final TDC circuit.



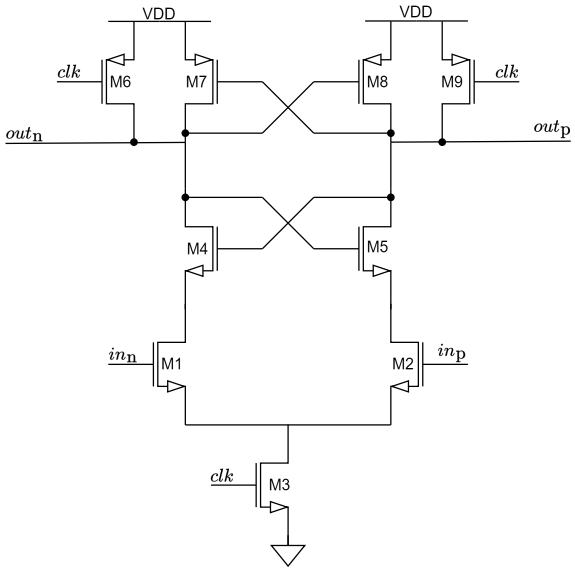
(a) Block diagram of the proposed SAR TDC architecture's top view.



(b) Proposed stage architecture.



(c) Proposed SDTCell architecture.



(d) Proposed TC CMOS Schematic.

Figure 4.14: Proposed time-to-digital converter.

5

Results and Conclusions

Contents

5.1 Full Analog-to-Digital Converter simulation results

Putting the proposed TDC in series with the proposed VTC, a full ADC is achieved. To evaluate this system, a differential 400mV signal is introduced as input. The output, of both the VTC and the TDC, are measured with ideal VerilogA blocks, outputting a voltage proportional to either the received signals delay or the equivalent normalized binary word, respectively. These VerilogA blocks do not interfere in the device-level simulations run, only allowing the information to be perceived using other quantities.

Figure 5.1 represents the achieved output words for a sinusoid close to the Nyquist frequency. For a different frequency and/or amplitude input, there are slight improvements for lower values. However, the impact suffered is always under 1% for every measurement, concluding a good rejection for these quantities variations. The fast furrier transform is shown in figure 5.2, from which the values explicit in table 5.1 are calculated, for the proposed full ADC. Figure 5.3 shows the results for a ramp input, and figure 5.4 represents the INL error for the measures codes.

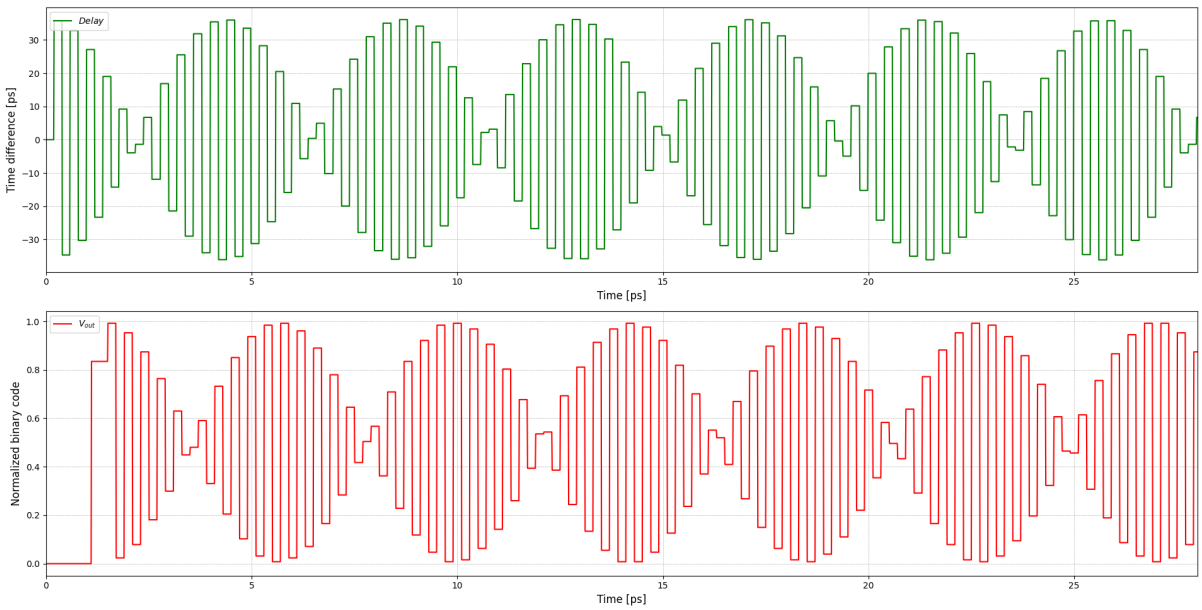


Figure 5.1: Sinusoidal Input, $f_{\text{in}} = \frac{61}{64}\frac{f_{\text{S}}}{2} = 2,382,812,500$Hz; sampled at $f_{\text{S}} = 5$GHz

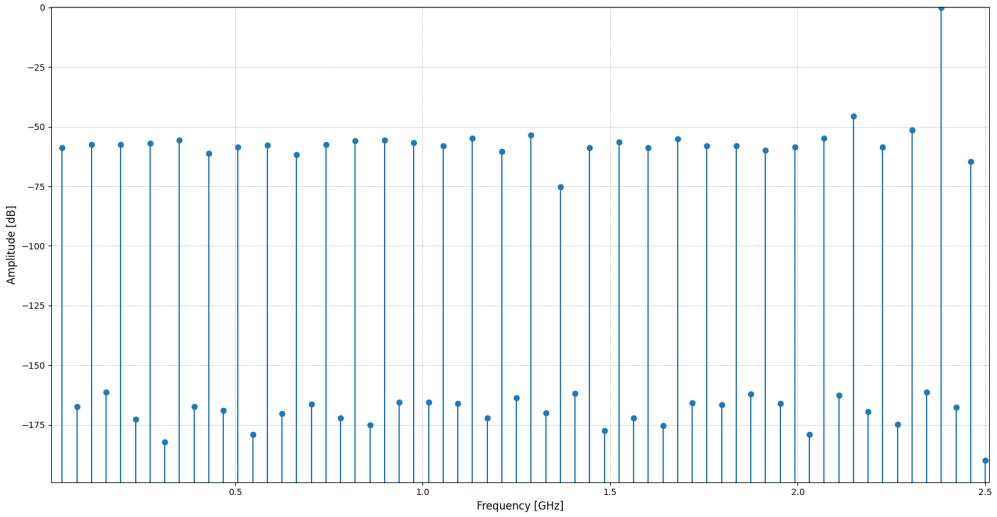


Figure 5.2: Fast furrier transform. $f_{\text{in}} = \frac{61}{64}\frac{f_{\text{S}}}{2} = 2,382,812,500\text{Hz}$; sampled at $f_{\text{S}} = 5\text{GHz}$ with 128 points.

Latency	SFDR	SNR	SNDR	THD	ENOB	P	FOM_W [fJ/conv]
1.2 ns	45.44 dB	42.29 dB	40.86 dB	−46.38 dB	6.5 bit	12.54 mW	27.71

Table 5.1: Final results for the proposed full analog-to-digital converter.

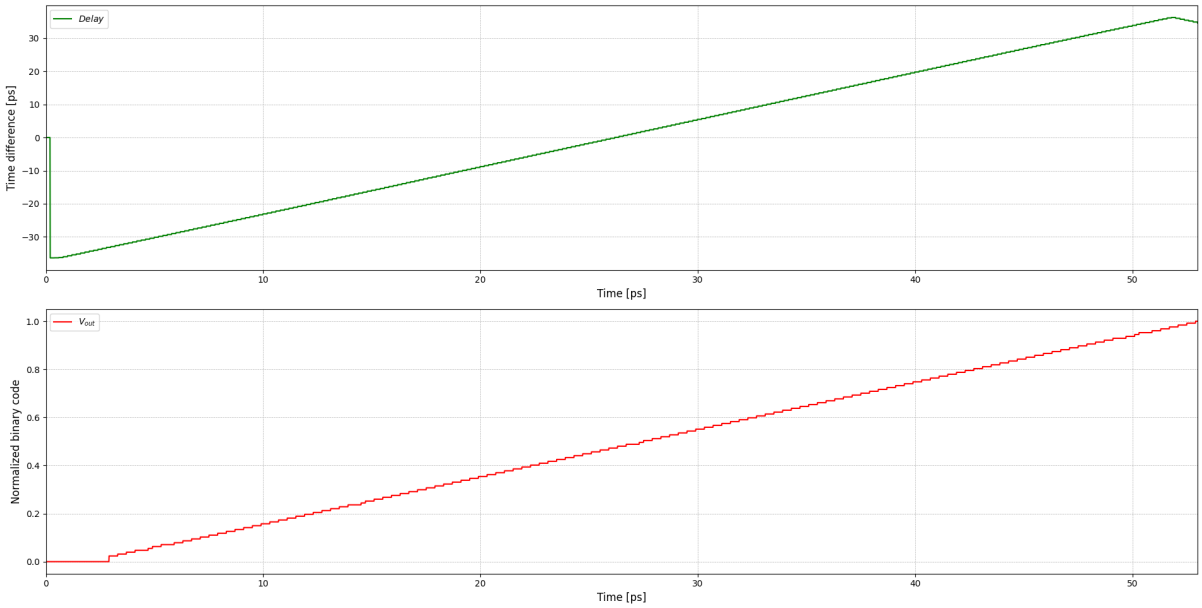


Figure 5.3: Ramp input.

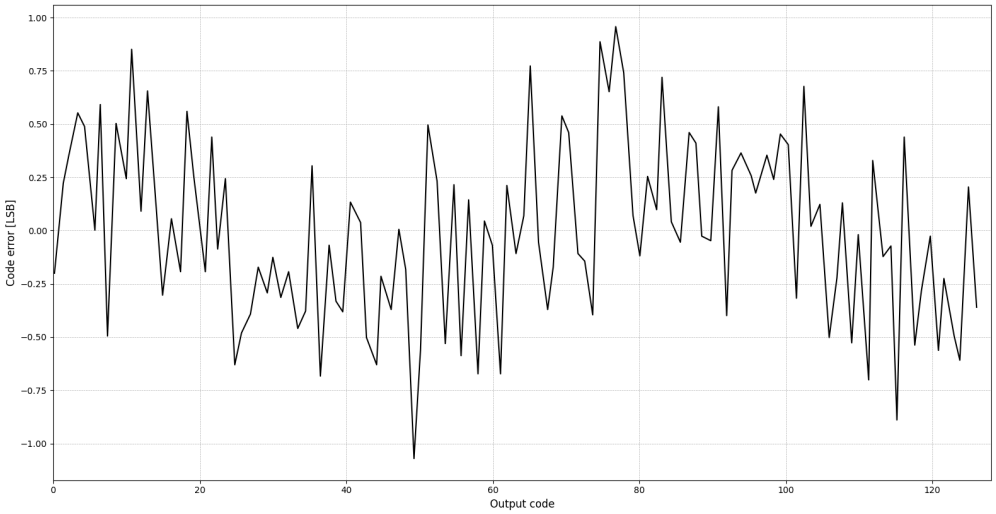


Figure 5.4: Integral non-linear error.

Even if the presented results are deemed good, some problems should be addressed. From the ramp (5.3) and the INL (5.4) figures, errors for some of the codes are visible, especially on the Most Significant Bit (MSB) transitions, which overcome more than 1 LSB in at least one case. These limitations have their main origin in the SDTCells. The different delays for each line, which should equal the values from table 4.1 are not exactly correct for every stage. Also, their variations, due to the non-linearities referred to, became impactful in distorting the output. If VerilogA blocks substitute the SDTCells for ideal operations blocks, with no variation and accurate delay differences, the ENOB increases to 6.74 bit. Furthermore, table 5.2 presents the ENOB if only some of the initial bits are considered, clarifying the smaller contribution further stages have on the overall system, due to their increased time sensitivity to errors.

Resolution	7 bit	6 bit	5 bit	4 bit
ENOB	6.49 bit	5.85 bit	4.96 bit	3.97 bit

Table 5.2: Effective number of bits if only some bits are considered.

As for the power distribution between the multiple blocks, from the 12.54 mW consumed, only 4.83% are dispended on the VTC (the previously stated 606μW, section 3.5). The remaining 95.17% are spent on the TDC. The clock generator consumes 2.45mW (19.5%), the sampling registers take 1.77mW (14.11%), the first six stages consume on average 1.23mW each ($9.82\% \times 6 = 58.91\%$), and the seventh stage, which consists only of the comparator and some buffers, consume 332μW (2.65%).

5.2 Conclusions

Overall, the objectives of this work were fulfilled. Multiple TMSP techniques were studied, and a full ADC was reached, successfully fulfilling all the set specifications.

From an exploratory point of view, multiple VTC ideas were researched to conclude the proposed circuit. The CS dual ramp generator with a single current source VTC shows a good balance between results and complexity with a proved robustness to corners and Montecarlo variations.

As for the TDC, even if issues prevail, such work is a good starting point for further improvements.

Simulation results for the full ADC are presented, reaching promising values.

The concluded circuit operates at the stated 5 GHz, without any TI techniques. It can be considered, therefore, a very high speed circuit, processing the received information at rates that equal and even overcome most of the state of the art systems.

5.3 Future work

In the present work, there is a need to make a separation between the VTC and the TDC. The VTC was tested to a deeper extent, being robust to both corner and Montecarlo simulations, section 3.5. On the other hand, for the TDC only one architecture was simulated in a typical corner and without Montecarlo simulations. Arising problems may require further ideas and circuit changes to be studied.

Regarding the VTC, the following work step would be to design the layout and extract its respective parasitics. Some design interactions may be needed to conclude a final circuit. The two major focus points, in case a higher-performance circuit is needed, should be the current source linearity and the capacitor sizes. Some options to keep in mind are the use of a cascode current mirror or the implementation of a charge-sharing architecture. There can also be a discussion for calibration of this circuit, making it more robust to PVT variations. Controlling the injected current and adjusting the sensing comparators threshold are alternatives to better this circuit.

As for the TDC, there is more to be done. There needs to exist corner and Montecarlo simulations. It is expected that these results bring up issues that need further changes to the circuit. The main problems should be related to the synchronization of the clocks in each stage and their sampling to the registers, as well as delay differences in both the SDTCells or the delay lines themselves. A small variation in either the delay lines as a whole or in the SDTCells will influence the results by unbalancing some of the code's differential nonlinearities or even causing offset or gain errors. If the issues in this realm are concluded to be of great magnitude, the delay cells architecture could have to be rethought. Other possible changes to the circuit are situations where the result of the comparator, or the signals from SDTCells, generate both the clock for the following stage and enable the registers' sampling signal. Not only could the circuit become more resistant to PVT and mismatch variations, but there could also exist some improvements

in the mentioned TC problems. Ideas such as those presented in [53] can prove to be a good option to explore. Further on, layout and parasitics extractions will also affect the circuit. The capacitances between lines and the signal's crosstalk influence between parallel paths are expected to deeply impact the working of such a system. Finally, there may also be calibration possibilities. Applying calibration to the comparators and the SDTCells may allow offset and gain corrections, as well as diminish the delay line errors and non-linearities.

Furthermore, considering the ADC as a whole, if changes in either the duty cycle, to a value higher than the used 50%, or a smaller and faster technology node are considered, then an increase in resolution or frequency can be studied.

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