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LOW POWER CONSUMPTION, HIGH PSRR AND ACCURATE BANDGAP VOLTAGE REFERENCE

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Resumo

Os circuitos que geram referências de tensão, *bandgap*, são amplamente utilizados em sistemas analógicos, digitais e *mixed-signal*, uma vez que permitem gerar, a partir de uma bateria, uma tensão de referência estável e precisa. A precisão no valor constante (dc) e a imunidade a transitórios que resultam de fluctuações da alimentação (ac) dos circuitos de referência é crítica para assegurar elevados níveis de desempenho dos blocos do Circuito Integrado que utilizam a sua tensão. Esta tese investiga a possibilidade de implementação de uma referência de tensão bandgap num ambiente caracterizado por uma tensão de alimentação com valor dc que pode sofrer pequenas fluctuações, variações de temperatura e processo de fabrico, e que, mesmo assim, é capaz de apresentar:

- elevada precisão dc apesar de variações na tensão de alimentação, temperatura e processo de fabrico, minimizando assim a influência do processo de ajuste durante o teste da *wafer* e mantendo relativamente baixa a complexidade do circuito através de compensação de temperatura de primeira ordem,
- elevada precisão dc e ac sem utilizar condensadores internos de elevada capacidade,
- elevada precisão dc e ac apesar de possíveis variações na carga, e sem introduzir mais complexidade e consumo de potência através de um *buffer* de saída adicional,
- baixo consumo de potência, que permite que o circuito seja integrado em aplicações dependentes da tensão de uma bateria e portáteis,
- uma implementação que utiliza processos de fabrico *standard* em CMOS, o que reduz os custos de produção, e
- baixa ocupação de área, o que permite menos ocupação de espaço no Circuito Integrado em que for integrado.

A referência de tensão *bandgap* proposta será integrada num *Charge Pump* e numa Unidade de Gestão de Potência constituída por conversores $DC - DC$ e reguladores de tensão *low dropout*. Implementado em tecnologia CMOS $TSMC$® 65 nm, o circuito inclui um pré-regulador, fonte de corrente e validação digital da tensão de bandgap. O consumo de corrente é menor que $5\mu A$ a $50^{o}C$, a Razão de Rejeição da Potência de Alimentação é de $-110dB@1kHz$ e

$-61.3dB@10MHz$ utilizando $27pF$ de capacidade interna, o valor típico da tensão de referência é de $1.208V$ e o coeficiente de temperatura é de $3ppm/°C$, considerando o intervalo $[-40, 125]°C$. O procedimento de ajuste do valor das resistências tem de ser feito, para se obter o valor anterior, uma vez que no pior processo de fabrico simulado, o coeficiente de temperatura é de $64ppm/°C$. A área ocupada pelo circuito de referência é de $0.04mm^2$. O desenvolvimento do circuito *bandgap* proposto vai de encontro às exigências de baixo custo, alta precisão e baixo consumo das tecnologias de vanguarda de sistemas integrados.

Palavras Chave

Circuitos integrados analógicos, baixo consumo, PSRR, tensão de referência, bandgap.

Abstract

Bandgap reference circuits are widely used in analog, digital and mixed-signal systems since they can generate a stable, accurate and standard reference voltage from a battery supply. The steady-state (dc) and transient (ac) accuracy of reference circuits is critical to ensure that the further blocks of the IC present high levels of performance. This thesis investigates the possibility of implementing a bandgap reference in an environment characterised by power supply range and fluctuations, temperature and process variations, which, even though, is able to present:

- high dc accuracy despite power supply, temperature and process variations, minimizing the influence of trimming process during wafer's test and keeping relatively low complexity with first-order temperature compensation,
- high dc and ac accuracy without using large on-chip capacitors,
- high dc and ac accuracy despite load variations, without introducing more system complexity and power consumption with an additional output buffer,
- low power consumption, which allows it to be integrated in modern and battery-operated portable applications,
- an implementation that utilises a standard CMOS process which minimizes manufacturing cost, and
- low area occupancy, to consume less IC space.

This bandgap voltage reference will be further integrated in a Charge Pump IP and in a Power Management Unit (PMU) constituted by $DC-DC$ converters and low dropout regulators. Implemented in $TSMC$® 65 nm CMOS technology, the circuit includes a pre-regulator, a master bias cell and digital validation for the bandgap voltage. The current consumption is below $5\mu A$ at $50^{o}C$, Power Supply Rejection Ratio (PSRR) of $-110dB@1kHz$ and $-61.3dB@10MHz$ using $27pF$ on-chip capacitance, reference output voltage is $1.208V$ and temperature coefficient is $3ppm/^{o}C$ considering a $[-40, 125]^{o}C$ range and the typical process. Resistor trimming procedure must be done in order to achieve the latter value, since temperature coefficient is $64ppm/^{o}C$ in the worst case process. The area occupied by the reference circuit is $0.04mm^2$. The development of the

proposed CMOS bandgap reference meets the low-cost, high-accuracy and low power demands of State-of-the-Art System-on-Chip environments.

Keywords

Analog integrated circuits, low power, PSRR, voltage references, bandgap.

Contents

List of Figures

List of Tables

List of Symbols and Abbreviations

V_{ref}	*Reference voltage*
V_{EB}	*Emitter-base voltage*
V_T	*Thermal voltage*
k	*Boltzmann's constant*
I_S	*Transistor saturation current*
q	*Electron charge*
$avdd$	*Analog* V_{dd}
$agnd$	*Analog* $ground$
CMOS	*Complementary Metal-Oxide Semiconductor*
IC	*Integrated Circuit*
SoC	*System on Chip*
BGR	*Bandgap Reference*
CTAT	*Complementary To Absolute Temperature*
PTAT	*Proportional To Absolute Temperature*
PSRR	*Power Supply Rejection Ratio*
TC	*Temperature Coefficient*
USB	*Universal Serial Bus*
DC-DC	*Direct Current-to-Direct Current*
PMU	*Power Management Unit*
IP	*Intellectual Property*
CPU	*Central Processing Unit*
dc	*steady-state*
ac	*transient*

1

Introduction

Contents

Until recently, it has been common practice to design and build analog integrated circuits separately from digital integrated circuits for several reasons. Analog circuits are often sensitive to and difficult to isolate from the noise caused by the switching of digital signals on the same integrated circuit. Also, it is often advantageous to build specific analog circuits in a different semiconductor technology (Gallium Arsenide or Bipolar Silicon, for instance) from the digital circuits associated with the design, which are usually more cost effectively implemented in a bulk CMOS process.

It is also more difficult to perform manufacturing tests of integrated circuits that contain both digital and analog circuitry. Although, today's Systems-on-Chip (SoC) need ever higher levels of integration, however. These needs, along with technology developments like BiCMOS (Bipolar and CMOS Technology on the same integrated circuit), SiGe (Silicon Germanium Technology), and even better techniques for implementing analog circuitry on bulk CMOS technology have led to more ”Mixed Signal” integrated circuits where analog functions and digital functions can be placed on the same integrated circuit.

In markets where the combination of performance, size, power consumption, weight, and thermal characteristics has particular importance (laptop computers, cell phones, and other handheld electronic devices for only some examples), the SoC became an attractive alternative to the traditional System-on-Board. To facilitate SoC design, on-chip interconnect architectures began to be developed to allow libraries of integrated circuit Intellectual Property (IP) to be mixed and matched as needed to allow application specific SoC to be developed by integrating previously designed components - design for reuse.

1.1 Motivation

Voltage and current reference circuits are fundamental building blocks of every SoC since they are often used to bias circuits or to supply a reference voltage to which other voltages are compared. Practical applications may be switching DC-DC converters, analog-to-digital and digital-to-analog converters, linear regulators, charge pumps, current sources, etc. Assuming a SoC environment, reference circuits are, commonly, found in a Power Management Unit (PMU) which is responsible for a correct and balanced distribution of energy in the IC, according to the needs of each block and operation modes. A PMU is, generally, constituted by DC-DC converters and low dropout regulators, and naturally, these circuits need a reference voltage to operate; hence, there is always a reference generation circuit which is, typically, implemented using a bandgap structure. A conceptual diagram of a SoC is presented in Figure 1.1.

Modern chips apply a considerable number of building blocks in only one chip, so it is suitable to have them consuming as less current as possible. Meanwhile, low power consumption allows SoCs to dissipate less heat and the extension of the battery's lifetime between charges, but also many other benefit factors. The supply voltage is, typically, a battery that suffers from variations

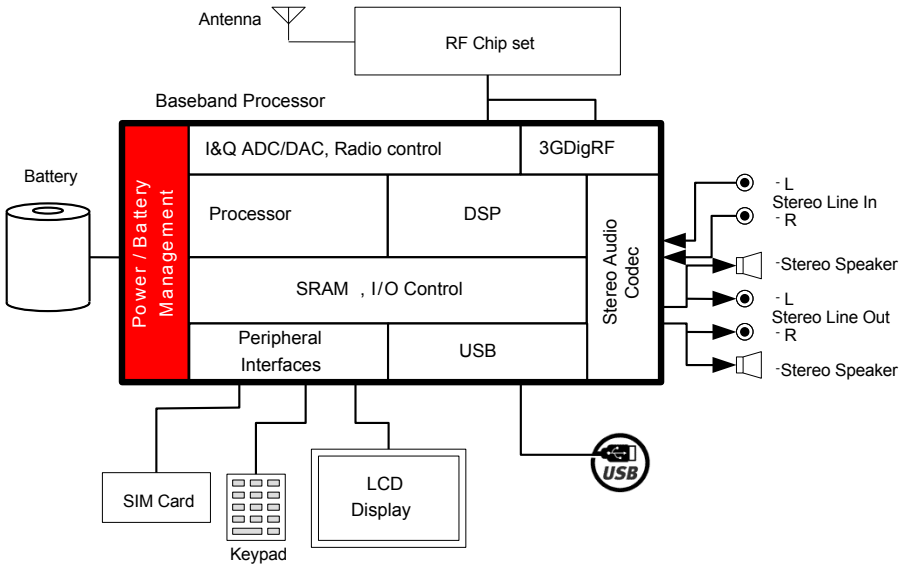


Figure 1.1: Conceptual diagram of the building blocks that constitute a modern System-on-Chip.

in its steady-state (dc) voltage and transient (ac) fluctuations which may be related to battery discharge, noise coupling and temperature dependence. In view of that, there is the need to generate a reference voltage which, ideally, would have no correlation to the battery voltage, and so it doesn't present the unwanted performance of the battery. Thus, voltage reference circuits are responsible for generating a constant dc voltage of known magnitude and are designed to be as much temperature independent as possible, along with high capability to reject supply voltage fluctuations and process variations.

Much architecture of voltage reference circuits has been studied so far and they can be organised in three topologies:

1. Using the difference in the threshold voltage between an enhancement transistor and a depletion transistor.

2. Using a zener diode that breaks down at a known voltage when reversed biased.

3. Cancelling the negative temperature dependence of a pn junction with positive temperature dependence from a proportional to absolute temperature (PTAT) circuit.

In modern circuits, the first two approaches aren't really used because depletion transistors are typically not available in CMOS foundries and zener diodes are usually larger than the power supplies, respectively. Rather, the third approach is the most popular for both bipolar and CMOS technologies and it is, commonly, called bandgap voltage reference, because the output voltage

can be expressed as a function of the silicon bandgap voltage extrapolated to the considered temperature.

1.2 Objectives

The purpose of this thesis work is to design and implement a CMOS bandgap reference circuit which shall exhibit high power supply rejection ratio (PSRR) and low power consumption, so that it represents a change magnitude in State-of-the-Art reference circuits. Particularly, different bandgap reference structures are studied, in order to obtain a simple and robust circuit that has potential to accomplish the specifications proposed.

In terms of specifications, the circuit is limited to a current consumption of $5\mu A$ and the range of the battery supply voltage is from $1.7V$ to $3.6V$. The PSRR is set to $-70dB@1kHz$ and $-40dB@10MHz$ and it is imposed that the reference voltage is capable of driving $10\mu A$. The design target for the output voltage shall be around $1.2V$. There is also a concern about the area occupied by the reference circuit, so the design is intimately related with the post implementation. Thereby, the maximum occupied area is set to $0.05mm^2$.

PSRR is important because high frequency switching often used in Systems on Chip affects the accuracy of bandgap references by coupling noise onto the supply routing channels and also introducing crosstalk effects in the reference output. These high frequency fluctuations can be minified by introducing large capacitors in the design. Thus, the area occupied by the IP is significantly increased; therefore an important matter of this thesis is to meet the specifications without introducing large capacitors, and also putting away any off-chip filter capacitor solution.

The proposed bandgap reference is designed and implemented in $TSMC$® 65 nm CMOS technology and it is intended to be integrated in a charge pump IP Core for a $10mA$ *USB* application and also in a DC-DC converter as a part of a PMU.

1.3 The Basic Bandgap Reference

A bandgap voltage reference is based on subtracting the voltage of a forward-biased diode (or base-emitter junction) having a negative temperature coefficient from a PTAT voltage. This PTAT voltage results from the amplification of the voltage difference between the base-emitter junctions. Figure 1.2 shows a symbol diagram of how a bandgap voltage reference is generated.

A forward-biased base-emitter junction of a bipolar transistor has a I-V relationship given by equation (1.1).

$$I_C = I_S \cdot e^{\frac{qV_{BE}}{kT}} \tag{1.1}$$

In equation (1.1), I_S is the transistor saturation current and is strongly proportional to temperature, q is the electron charge, k is the Boltzmann's constant and T is temperature.

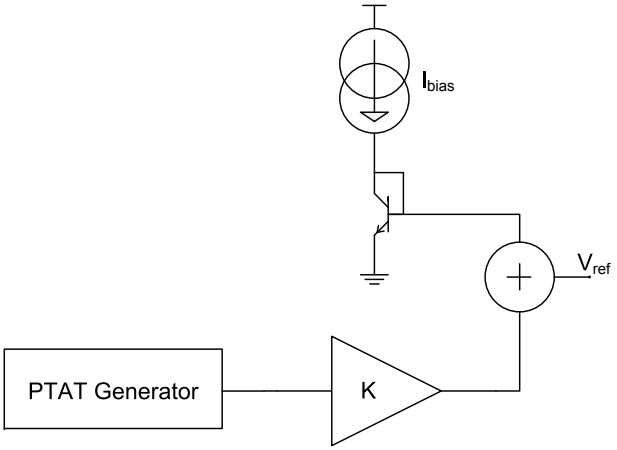


Figure 1.2: Diagram of a bandgap voltage reference.

The base-emitter voltage, as a function of collector current and temperature [1], is given by equation (1.2).

$$V_{BE}(T) = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\frac{T}{T_0} + \frac{mkT}{q}\ln\left(\frac{T_0}{T}\right) + \frac{kT}{q}\ln\left(\frac{J_C}{J_{C0}}\right) \tag{1.2}$$

V_{G0} is the silicon bandgap voltage at $0^{o}K$ (approximately $1.206V$), m is a temperature constant approximately equal to 2.3 and J_C is the collector current density. The subscript "0" designates an appropriate quantity at a reference temperature, T_0.

Assuming I_C constant, V_{BE} has a negative temperature dependence, often called the complementary to absolute temperature (CTAT) voltage, and it can be cancelled by a PTAT dependence that is generated using the amplified difference of two base-emitter junctions biased at fixed but different densities.

Supposing that there are two base-emitter junctions biased at currents J_1 and J_2 and making use of equation (1.2), the difference in their junction voltages is given by equation (1.3).

$$\Delta V_{BE} = V_2 - V_1 = \frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right) \tag{1.3}$$

The difference between the two junction voltages is, thereby, proportional to absolute temperature.

In Fig.1.3 is shown the temperature curvatures for the CTAT and PTAT voltages of a typical bandgap reference circuit.

Assuming that the junction currents are proportional to absolute temperature, even if the expected output voltage reference is temperature independent, it is possible to define the relation expressed by equation (1.4).

$$\frac{J_i}{J_{i0}} = \frac{T}{T_0} \tag{1.4}$$

J_i is the current density of the collector current of the ith bipolar transistor and J_{i0} defines the same current density but at the reference temperature.

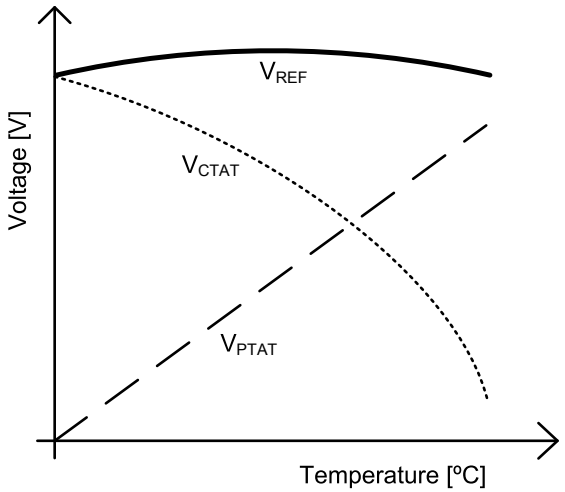


Figure 1.3: Typical temperature curvatures of CTAT, PTAT and bandgap reference voltages.

Hence, combining equations (1.2) and (1.3) along with equation (1.4), the output voltage reference is given by equation (1.5) and it represents the fundamental equation of a bandgap voltage reference as a function of temperature.

$$\begin{aligned} V_{ref} &= V_{BE2} + K \cdot \Delta V_{BE} \\ &= V_{G0} + \frac{T}{T_0}\left(V_{BE0,2} - V_{G0}\right) + (m-1)\frac{kT}{q}\ln\left(\frac{T_0}{T}\right) + K\frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right) \end{aligned} \tag{1.5}$$

In view of that, it is easy to obtain the output bandgap voltage that has a zero temperature dependence at a desired value, by making the derivate of equation (1.5) with respect to temperature such as equation (1.6).

$$\frac{\delta V_{ref}}{\delta T} = \frac{1}{T_0}\left(V_{BE0,2} - V_{G0}\right) + K\frac{k}{q}\ln\left(\frac{J_2}{J_1}\right) + (m-1)\frac{k}{q}\ln\left(\frac{T_0}{T} - 1\right) \tag{1.6}$$

Setting equation (1.6) equal to zero at $T = T_0$, the zero temperature dependence at the reference temperature is then given by equation (1.7).

$$V_{BE0,2} + K\frac{k}{q}\ln\left(\frac{J_2}{J_1}\right) = V_{G0} + (m-1)\frac{kT_0}{q} \tag{1.7}$$

From equation (1.5), the left side of equation (1.7) is equal to V_{ref} at $T = T_0$. Hence, for zero temperature dependence at $T = T_0$, the bandgap voltage reference has to be defined as in equation (1.8).

$$V_{ref} = \frac{1}{T_0}\left(V_{BE0,2} - V_{G0}\right) + K\frac{k}{q}\ln\left(\frac{J_2}{J_1}\right) + (m-1)\frac{k}{q}\ln\left(\frac{T_0}{T} - 1\right) \tag{1.8}$$

Note that V_{ref} is entirely independent of the current densities of the bipolar transistors, but if a different current density is defined, then the K factor must be trimmed and appropriately adjusted so it produces the correct reference output voltage. At the time the wafer is being tested, the

trimming process is critical because it defines the temperature curvature of the bandgap voltage reference. Hence, the temperature coefficient may be lower or higher depending on the range of trimming and it is realized by adjusting the value of the resistors that generate the reference voltage. From equation (1.7), the value of K factor is given by equation (1.9).

$$K = \frac{V_{G0} + (m-1)\frac{kT_0}{q} - V_{BE0,2}}{\frac{kT_0}{q}\ln\left(\frac{J_2}{J_1}\right)} \tag{1.9}$$

Baring in mind these concepts, the first bandgap reference [2] proposes a way of obtaining a reference voltage that is not based on zener diodes. The architecture is very simple, although it is strongly dependent of temperature and it presents weak performance in terms of PSRR. At this time, power consumption was not even a relevant concern as it is nowadays.

The Brokaw cell [3] proposes two enhancements: CTAT and PTAT voltages are generated by the same bipolar transistors and so it makes the project more reliable and easy to design; and the base currents have less influence in the overall performance of the reference, because transistors' gain is less important. The disadvantages are the requirement of an error amplifier which imposes more current consumption, the dependency of collector-emitter voltages to the supply voltage, and the voltage drop across resistors. This topology is the basis for many bipolar and CMOS bandgap references. A simplified schematic of the circuit is presented in Figure 1.4.

The current source implemented by R_1 and R_2 resistors force the same current to the bipolar transistors which have different areas ($A_1 = 8 \cdot A_2$), and, thus, different base-emitter voltages. This difference once applied to R_3, generates the PTAT current and is defined by equation (1.10).

$$I_{PTAT} \equiv I_{C1} \equiv I_{C2} = \frac{\Delta V_{BE}}{R_3} = \frac{\frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right)}{R_3} \tag{1.10}$$

So all currents are indeed PTAT. Now, adding the influence of V_{BE1} voltage to the voltage across R_4, the output voltage reference is given by equation (1.11).

$$V_{ref} = V_{BE2} + V_{R4} = V_{BE2} + 2R_4 I_{PTAT} = V_{BE2} + 2\frac{R_4}{R_3}\Delta V_{BE} \tag{1.11}$$

Note that equation (1.11) is the right form of a bandgap voltage reference as in equation (1.5). The K factor of this topology can be expressed as in equation (1.12).

$$K = \frac{2 \cdot R_4}{R_3} \tag{1.12}$$

The correct bandgap voltage with, ideally, zero temperature dependence can now be achieved by changing the K factor value, i.e., trimming the values of both R_4 and R_3 resistors during the wafer's test process.

Analysing equation (1.10), there is one possible solution in which I_{PTAT} is equal to zero, that is to say, the reference voltage is, perfectly, stable in a "'zero-current"' or *off* mode. The circuit

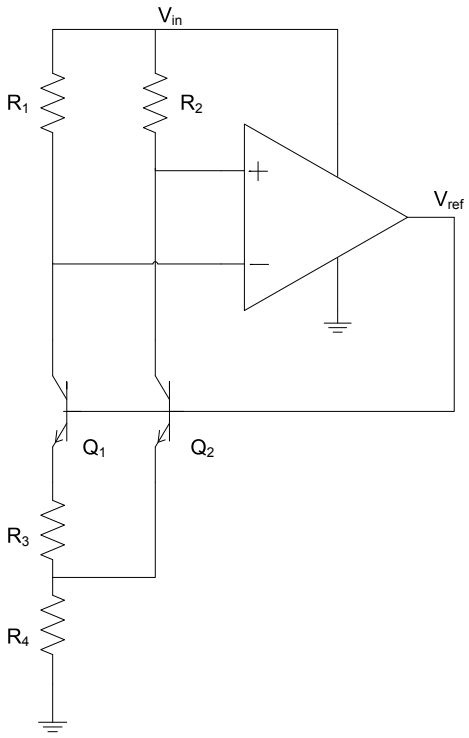


Figure 1.4: Typical bandgap voltage reference.

stays in this non-wanted stable state until a considerable amount of energy is applied, which makes the circuit to settle into the desired stable state. Therefore, reference circuits often need a start-up circuit that draws current to the collector of Q_1. In this topology, the current is drawn through Q_1 and then it is mirrored (due to R_1 and R_2) to the collector of Q_1, making the system to start converging to the stable and desired state.

1.4 Primary Specifications

A bandgap reference is an analog block which accuracy is meant to be as reliable as possible. Factors like current mirror and resistor mismatch, resistor tolerance, bipolar transistor mismatch and V_{BE} spread represent the most typical source of errors in bandgap references [4].

Current mirror errors upraises from deviations on the mirror ratio, and they may be caused by resistor and bipolar area mismatch, threshold voltage mismatch and W/L transistor mismatch. Layout techniques can be used to implement current mirrors, so that the result of Monte Carlo simulations presents very good accuracy.

Resistor mismatch is generated by weak layout techniques and it, certainly, influences the PTAT current. Typically, it is possible to obtain a $\pm 1\%$ degree of accuracy.

Resistor tolerance errors exist due to process variations and consist in different resistor values

causing the PTAT current to be different and consequently the value of V_{BE} voltage.

Bipolar mismatch errors impose a deviation in their active areas so the desired ratio is then compromised.

Finally, V_{BE} spread results in a base-emitter voltage spread, hence, it instantly influences the output voltage reference.

In view of that, layout considerations have a huge impact to reduce many of the latter errors, so no other action is taken to prevent them, but implementing the designed bandgap reference according to the technology recommendations and layout techniques.

Recently, there is a lot of focus on designing high accuracy reference circuits with low power consumption and high PSRR specifications [5], [6], [7] and [8] due to the widespread popularity of hand-held products such as cellular phones and portable multimedia players. The main goal of this thesis is to obtain a low power consumption and high PSRR bandgap voltage reference circuit, having a good performance in the remaining aspects.

PSRR is a measure of how well the bandgap reference circuit rejects small-signal ac ripples coming from the input power supply over the frequency spectrum. Every ripple in the input power supply (δV_{in}) generates a corresponding ripple in the voltage reference (δV_{ref}) that depends on frequency. Thus, the PSRR of a general circuit is presented in equation (1.13).

$$PSRR = 20 \cdot \log \frac{\delta V_{ref}}{\delta V_{in}} \, [dB] \tag{1.13}$$

Typically, it is only specified at very low frequencies ($f < 1Hz$), although, $50/60Hz$ clock frequencies and high frequency switching presented in modern SoCs may couple noise onto the supply lines, so it is primordial to study and analyse the system capability to reject these ripples. This is especially important in data conversion contexts, where high frequency power supply noise can be folded back into the signal band producing aliasing effects. The performance of the system is drastically decreased in switched-capacitor filters as already studied [9].

The temperature coefficient (TC) of a bandgap voltage reference, [10] and [11], is another major specification for bandgap reference circuits. It represents the effect of temperature deviation in the dc value of the reference voltage. It can be expressed as in equation (1.14).

$$TC = \frac{V_{ref,T_2} - V_{ref,T_1}}{T_2 - T_1} \cdot \frac{1}{V_{ref,T_0}} \, [ppm/^{\circ}C] \tag{1.14}$$

In equation (1.14), T_2 and T_1 are the upper and lower temperature extremes; V_{ref,T_2} and V_{ref,T_1} are the value of the bandgap voltage reference when temperature is T_2 and T_1, respectively; and $V_{ref,T0}$ is the reference voltage for the typical case (it can be, roughly, given by the mean value of V_{ref,T_2} and V_{ref,T_1}). The bandgap TC characterization is performed by introducing variations in PTAT and CTAT components which make the reference voltage change the dc dependence as the temperature.

Recalling equation (1.2), first order compensated bandgap references present a typical bell curve [12] where the resistor ratio of K factor is calculated so that the TC of V_{PTAT} equals appro-

ximately $+2mV/^{o}C$ to correct the linear term of the V_{CTAT} voltage. A standard value for a first order TC is $25ppm/^{o}C$. On the other hand, second order compensated bandgap references try to reduce the logarithm term of Eqn. (1.2) which is not simple to design. Theoretically, it is added to V_{ref} expression the exact opposite of the concave bell curve, i.e., a convex curve. Therefore, a corrected second order bandgap reference is generated where $V_{ref} \cong V_{G0}$; and TC is in the order of $1ppm/^{o}C$ which is a highly good performance. In this thesis, first-order compensation is chosen due to area limitations and simplicity.

1.5 Outline

This thesis is organized in 7 chapters. A brief description of each remaining chapter is presented as follows:

- **Chapter 2: High PSRR**
  This chapter provides the concepts beyond PSRR in linear systems and presents a case of study to reach high PSRR performance.
- **Chapter 3: Low power consumption**
  This chapter provides the proposed strategy and trade-offs to acquire a low power consumption bandgap reference.
- **Chapter 4: System design**
  This chapter provides an overview through the designed analog and digital blocks that constitute the proposed bandgap reference circuit.
- **Chapter 5: Simulation results**
  This chapter provides illustrations of transient, temperature sweeps, ac performance of the bandgap reference and a Monte Carlo analysis.
- **Chapter 6: Layout**
  This chapter emphasises to the layout techniques that may be used to reduce mismatch. It also contains an illustration of the final top layout of the proposed bandgap reference.
- **Chapter 7: Conclusions**
  This chapter is a summary of the contributions and major finding of the thesis and it includes a discussion on possible future work.

2

High PSRR

Contents

In modern SoC designs, radio-frequency, analog, and digital circuits reside in one common package. High frequency noise generated by digital circuits couples onto analog supply lines through crosstalk and, consequently, the ac performance of bandgap references is greatly affected. Adding large external bypass capacitors at both input and output of the bandgap circuit kindly suppresses the effects of power supply fluctuations on the reference voltage, along with separate power supply lines for analog and digital circuits. The RF and analog portions of the chip however, may still share a common supply. High frequency noise components from RF circuits can also couple onto the analog power supply. With continued scaling of supply voltages and increased integration, power supply rejection ratio (PSRR) becomes a critical design concern for reference circuits [13]. This chapter describes the State-of-the-Art techniques to obtain high PSRR and it follows a case of study which results in the design and evaluation of the proposed strategy at circuit-level.

2.1 State-of-the-Art Techniques

The first and basic solution to improve the PSRR of bandgap references is to filter power supply fluctuations before they reach the reference voltage and that can be made using an RC filter in line with the power supply as shown in Figure 2.1.

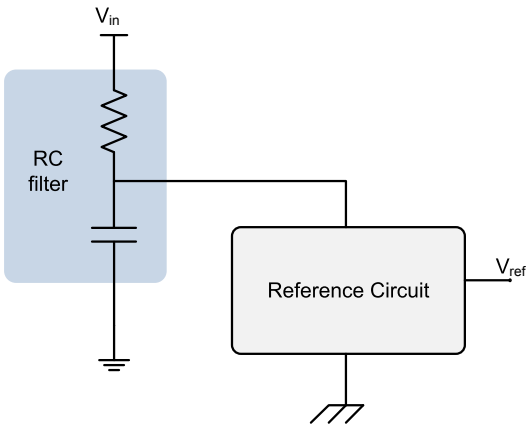


Figure 2.1: State of the Art technique to improve PSRR: use of a RC filter.

This solution adds a pole to the PSRR curve at the filters corner frequency. However, considering a low voltage SoC solution, the resistor's size would be largely limited due to the reduction in available voltage headroom caused by the dc current flowing through the resistor, and to the resultant voltage drop. As a result, the pole would be pushed to very high frequency.

Another technique is to generate a new supply voltage for the bandgap reference circuit which is already filtered from fluctuations in the power supply line. The PSRR is improved due to the increase in the resistance between the input supply and the reference's supply. One possible

architecture is to use a pre-regulator in series with the reference circuit, as shown in Figure 2.2. This is a very compact and effective method to achieve high PSRR performance, although it has the obvious disadvantage of an additional power dissipation and increased voltage headroom.

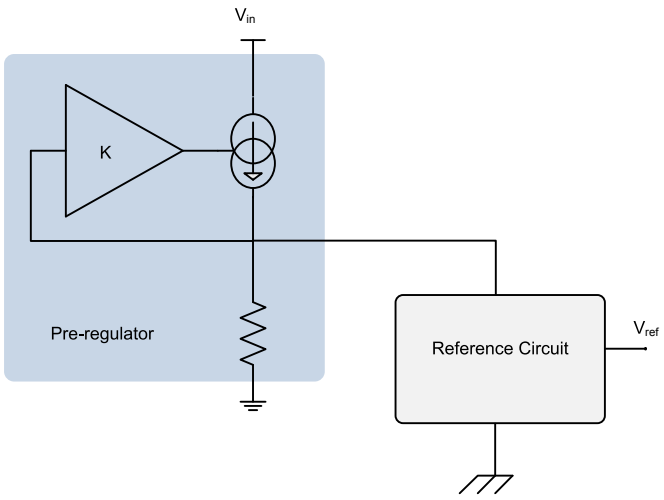
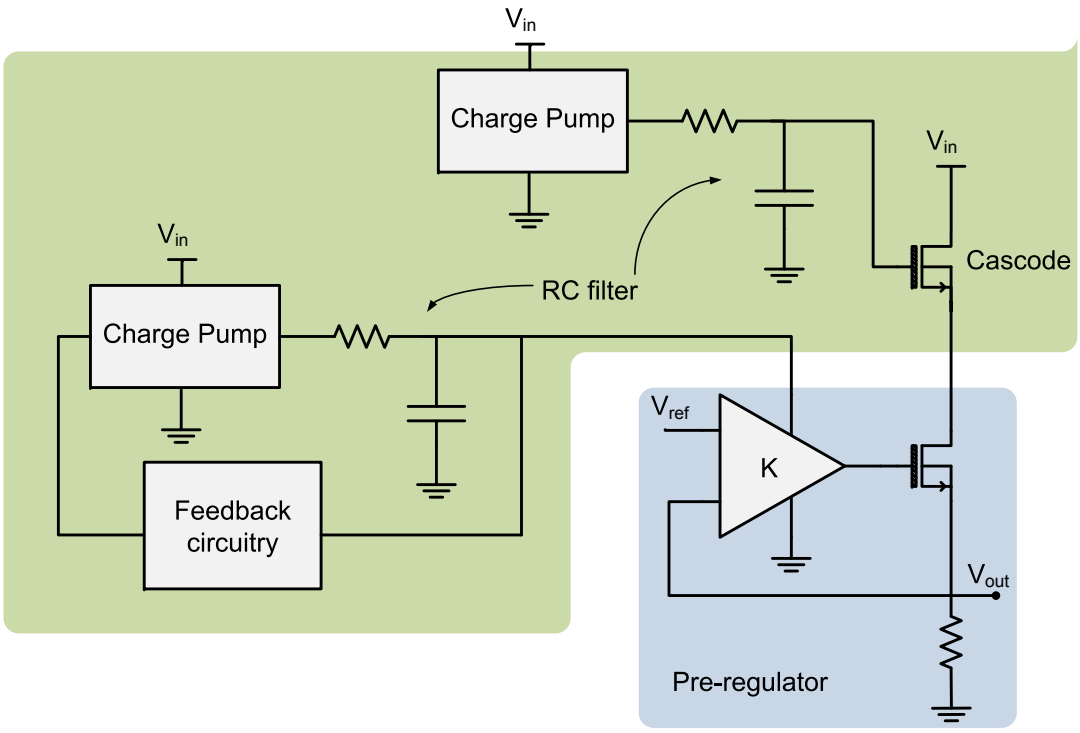


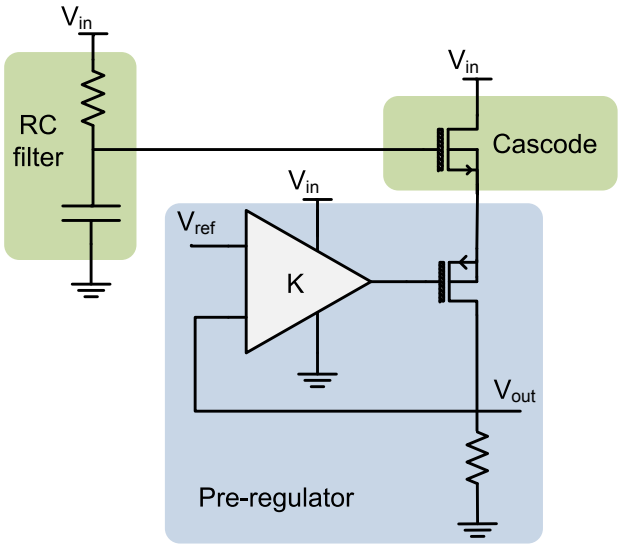
Figure 2.2: State of the Art technique to improve PSRR: use of a pre-regulator.

A different solution to improve PSRR is to utilize an NMOS transistor to isolate circuits from fluctuations in the power supply line [13]. It has been used effectively with linear regulators and can be also applied to reference circuits. Figure 2.3(a) presents a cascode for the NMOS pass transistor of a linear regulator, hence the source of the latter is isolated from the supply line instead of being connected to it. Meanwhile, since the NMOS is a source follower, it cannot be used with a gate voltage below the supply voltage; therefore the circuit requires a charge pump that generates a higher voltage. On the other hand, the supply of the error amplifier has also to be boosted using another charge pump, in order to maintain low dropout. The error amplifier, however, cannot be similarly cascoded since the gate of its NMOS cascode would require a boosted voltage of two gate-to-source drops above the output, leading to higher circuit complexity. Therefore, a RC filter is used to suppress fluctuations in the power supply line and the systematic fluctuations of the charge pump. Evidently, this approach results in large power consumption, layout area and system complexity.

A PSRR of $-40dB$ is demonstrated in [14], over a wide frequency range, using an NMOS transistor to cascode the PMOS pass transistor of a Miller-compensated linear regulator, as shown in Figure 2.3(b). Due to relatively high voltage headroom, the gate of the NMOS cascode is biased through the supply using a simple RC filter. The high voltage headroom also allows the error amplifier, which is powered directly from the supply, to use internal cascodes and gain boosting to improve its PSRR performance. This increases circuit complexity, dropout voltage, and power consumption. Moreover, the circuit used $1.2nF$ of on-chip decoupling capacitance that occupies



(a) Two charge pumps.



(b) Simplified Cascoding technique.

Figure 2.3: State of the Art techniques to improve PSRR

a prohibitive area for most modern SoC systems.

2.2 Case of Study

The use of cascode techniques to improve PSRR performance in reference circuits implies a substantial increase in layout area, along with higher power consumption and system complexity. The designed bandgap reference is intended to be used in a Charge Pump IP, so it makes no sense to use NMOS cascode techniques previously presented. Rather, a pre-regulator can be used to obtain good PSRR results at low frequencies; and decoupling capacitors can limit the PSRR curves at high frequency, where the pre-regulator is no longer capable of seeing perturbations, not even correct them. Thus, the case-of-study is focused to the use of a pre-regulator solution as the main responsible circuit to achieve the proposed PSRR specifications for this work. A pre-regulator is studied and designed in order to demonstrate the increase in PSRR performance achieved by this structure. Furthermore, the pre-regulator is added to the reference circuit and the system is simulated.

2.2.1 PSRR of a pre-regulator

A general electrical circuit has an input, an output and a power line as shown in Figure 2.4.

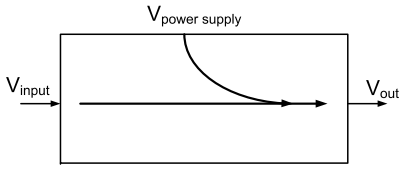


Figure 2.4: Block diagram of a general electrical circuit.

Every node in the circuit can be expressed referring to another node in the circuit, but sometimes it only matters the transfer function from the input (V_{in}) to the output (V_{out}) and from the power supply node ($V_{powersupply} \triangleq avdd$) to the output. If the transfer function of the power node to the output node is called the power supply gain (A_{avdd}), and the transfer function of the input node to the output node is called the open-loop transfer function (A), then the PSRR, in the frequency domain $s = jw$, is given by equation (2.1).

$$PSRR(s) = 20 \cdot \log \frac{A(s)}{A_{avdd}(s)} \, [dB] \tag{2.1}$$

It is evident that if $A_{avdd}(s)$ decreases, the PSRR increases; if $A(s)$ increases by increasing the gain-bandwidth product (GBW) of an amplifier, so PSRR increases too.

The equivalent mathematical equation for the output node, as a function of V_{in} and V_{out}, is described by the superposition of the power supply gain and the open-loop gain is expressed as in equation (2.2).

$$V_{out} = A_{avdd} \cdot avdd + A \cdot V_{in} \tag{2.2}$$

Thus, this analysis can be used to obtain a mathematical expression that models the PSRR of a linear regulator or pre-regulator.

The pre-regulator is simply a closed-loop system consisting of an error amplifier, a resistive feedback network and a series pass transistor. Its schematic is shown in Figure 2.5.

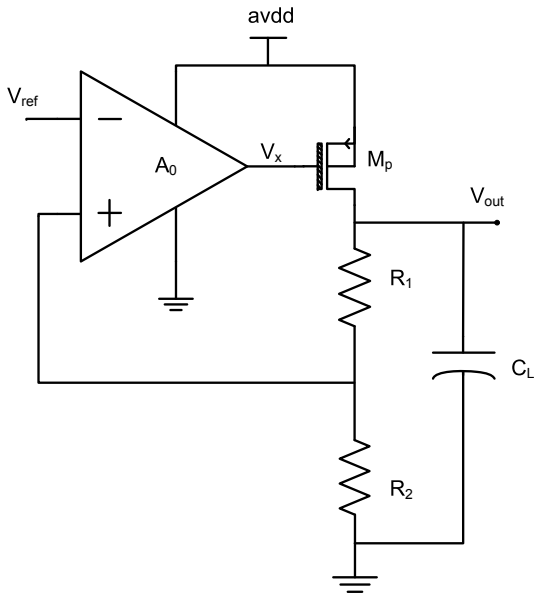


Figure 2.5: A typical topology for a linear regulator.

Equation (2.3) presents the dc value of the pre-regulator's output (V_{out}), where V_{ref} is, typically, the bandgap voltage which is supposed to present low noise characteristics and high immunity to fluctuations in the power supply line.

$$V_{out} = V_{ref} \cdot \left(1 + \frac{R_1}{R_2}\right) \tag{2.3}$$

In order to calculate the PSRR of the pre-regulator, the system can be represented by a block diagram using control-system theory, as shown in Figure 2.6.

Thereby, recalling equation (2.2) and assuming that the contribution of the reference voltage to supply noise is negligible, the small signal variations of the pre-regulator's output voltage due to the presence of noise in *avdd* can be given by equation (2.4).

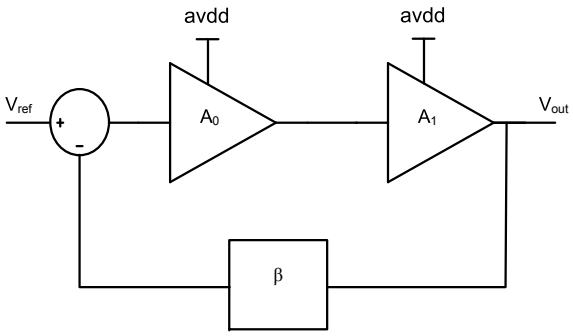


Figure 2.6: Control diagram of the pre-regulator.

$$\begin{aligned} V_{out} &= A_{avdd} \cdot avdd + A_0\beta \cdot A_1 \cdot (-V_{out}) \\ \Leftrightarrow V_{out} &= \frac{A_{avdd} \cdot avdd}{1 + A_0\beta \cdot g_{mp} r_{dsp}} \end{aligned} \tag{2.4}$$

In equation (2.4), β is the feedback factor $R_2/(R_1 + R_2)$, A_0 is the open-loop gain of the error amplifier, A_1 is the gain of the pass transistor given by $g_{mp} \cdot r_{dsp}$ (the transconductance and drain-to-source resistance, respectively).

The small signal model of the pass transistor shown in Figure 2.7 is used to calculate the mathematical expression of A_{avdd} and it considers that the influence of the feedback resistors is negligible.

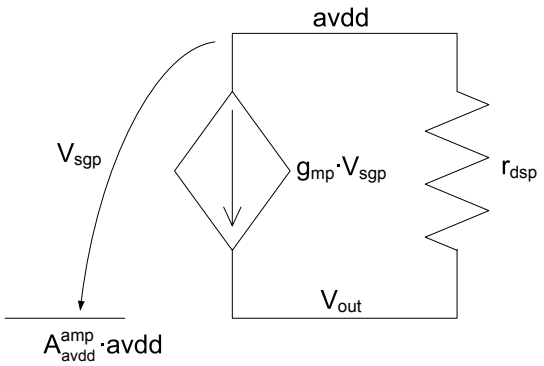


Figure 2.7: Small signal model of the pass transistor considering a PSRR anaylsis.

The presence of power supply fluctuations in the error amplifier is considered in the analysis so that the gate of the PMOS pass transistor is not connected to a small-signal ac ground, but to

the gain seen from the power supply to node V_x, in an open-loop configuration. From Figure 2.7, the transfer function from the power supply to the output of the pre-regulator is given by equation (2.5).

$$A_{avdd} = 1 + g_{mp} r_{dsp} \cdot (1 - A_{avdd}^{amp}) \tag{2.5}$$

In equation (2.5), A_{avdd}^{amp} is the power gain equals to $V_x/avdd$.

Now, using both equations (2.4) and (2.5), the PSRR of the pre-regulator can be expressed as in equation (2.6).

$$\begin{aligned} \frac{V_{out}}{avdd} &= \frac{1 + g_{mp} r_{dsp} \cdot (1 - A_{avdd}^{amp})}{1 + A_0 \beta \cdot g_{mp} r_{dsp}} \\ &= \frac{1}{1 + A_0 \beta \cdot g_{mp} r_{dsp}} + \frac{g_{mp} r_{dsp} \cdot (1 - A_{avdd}^{amp})}{1 + A_0 \beta \cdot g_{mp} r_{dsp}} \end{aligned} \tag{2.6}$$

Rearranging this equation, the PSRR of the pre-regulator considering dc operation is given by equation (2.7).

$$PSRR_{dc} \cong \frac{1}{A_0 \beta \cdot g_{mp} r_{dsp}} + \frac{(1 - A_{avdd}^{amp})}{A_0 \beta} \tag{2.7}$$

From equation (2.7), a technique to achieve high PSRR performance is to increase the open-loop gain of the error amplifier, A_0, and reduce the gain factor β if possible. Another useful approach is to have A_{avdd}^{amp} such that $A_{avdd} = 0$. The basic idea is to have a subtractor stage inserted between the PMOS pass transistor and the error amplifier, which feeds the supply noise directly into the feedback loop and modulates the pass transistor gate with respect to the source terminal. Thereby, that would imply additional circuitry which can be resumed to higher power consumption and area cost for the system, so this solution is not taken in consideration.

A topology for the error amplifier has to be defined in order to calculate the power gain of the error amplifier, A_{avdd}^{amp}, as a function of transconductances and admittances that are present in the circuit. It was considered a single-ended folded cascode amplifier, as in Figure 2.8, with NMOS transistors in the differential pair and the small-signal model for a PSRR analysis is shown in Figure 2.9.

For this PSRR calculation, it is assumed that *agnd* is constant, both amplifier inputs are connected to small-signal grounds, and the error amplifier is in an open-loop configuration. The influence of M_3 transistor to the PSRR is negligible and so the transconductance of M_2 transistor because *agnd* and the polarization voltage of the current source, M_3, suffer no fluctuations and the power signal flows straight to the amplifier output without direct influence of the differential pair. Therefore, applying Ohm's Law to node V_2, it results the expression presented in equation (2.8).

$$avdd \cdot g_{ds11} - V_{out} \cdot g_{ds9} = V_2 \cdot (g_{ds2} + g_{ds11}) \tag{2.8}$$

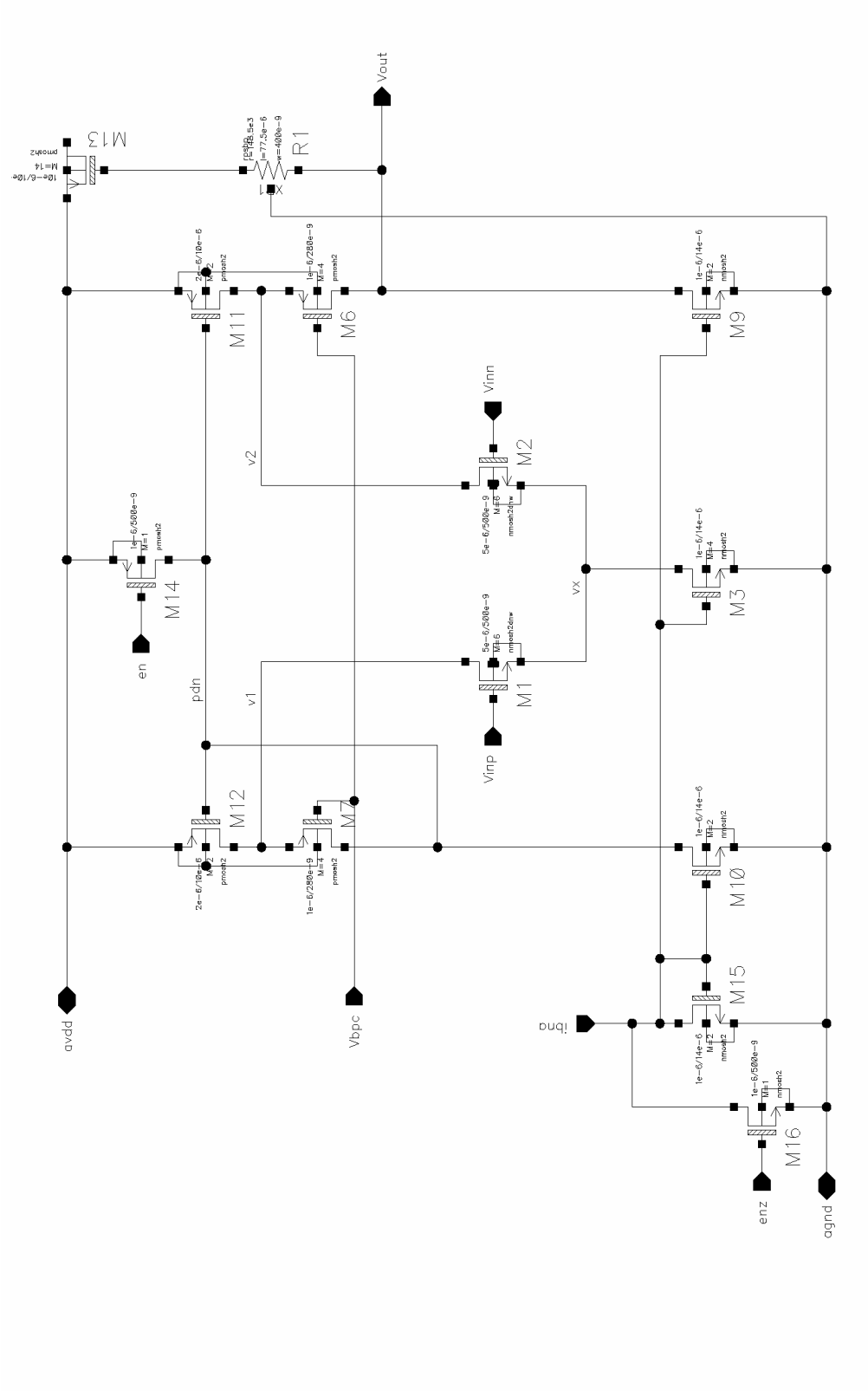


Figure 2.8: Error amplifier used in the pre-regulator.

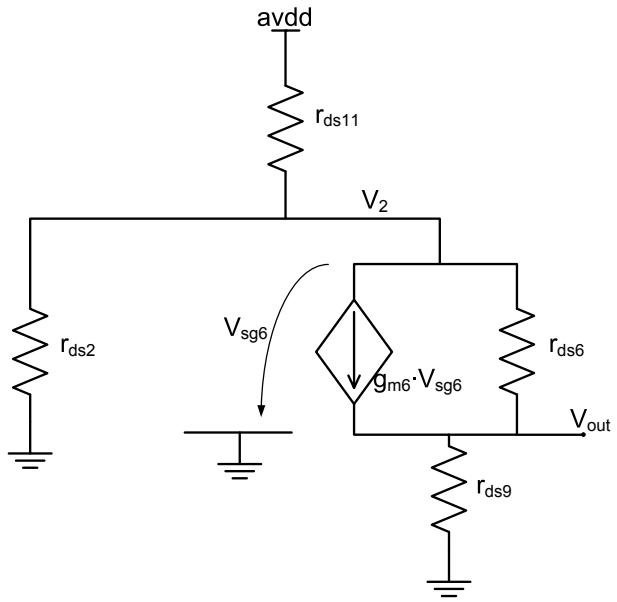


Figure 2.9: Small signal model of the error amplifier in an open-loop configuration.

Since V_x feeds the gate of the PMOS pass transistor, the drain currents of transistors M_6 and M_9 are equal and it results the expression of equation (2.9).

$$V_2 \left(g_{m6} + g_{ds6}\right) = V_{out} \left(g_{ds6} + g_{ds9}\right) \tag{2.9}$$

Substituting equation (2.8) in equation (2.9), the power gain of the error amplifier is given by equation (2.10).

$$\frac{V_x}{avdd} = \frac{g_{ds11}}{g_{ds9} + \frac{(g_{ds6}+g_{ds9})(g_{ds2}+g_{ds11})}{g_{m6}+g_{m6}}} \tag{2.10}$$

It is now possible to predict the PSRR of a pre-regulator using a single-ended folded cascode error amplifier for very low frequencies.

To consider the PSRR curve over the frequency spectrum, the PSRR analysis must include the capacitances connected to the significant nodes of the circuit. Hence, the bandwidth of the pre-regulator is now limited according to the capacitance connected to the gate of the PMOS pass transistor. The output capacitance, C_L, along with the output resistance, R_L, influence the frequency response of the pass transistor. Thereby, equation (2.4) can now be re-written as in equation (2.11).

$$V_{out} = A^{'}_{avdd} \cdot avdd + A^{'}_0 \beta \cdot A^{'}_1 \cdot (-V_{out}) \tag{2.11}$$

In equation (2.11), $A^{'}_0$ is the new open-loop gain of the pre-regulator given by equation (2.12).

$$A_0^{'} = \frac{A_0}{1 + sr_oC_A}, \tag{2.12}$$

$A_1^{'}$ is the new voltage gain of the PMOS pass transistor, r_o is the output resistance of the error amplifier and C_A is the output capacitance connected to the gate of the pass transistor. Considering both output capacitance and resistance, $A_1^{'}$ can be calculated by using the small-signal model of the pass transistor shown in Figure 2.10.

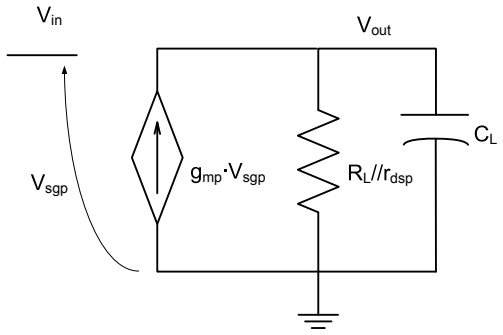


Figure 2.10: Voltage gain of the pass transistor considering a capacitive output impedance.

Assuming the drain-source capacitance negligible compared to the output capacitance, the voltage gain of the pass transistor is given by equation (2.13).

$$A_1^{'} = \frac{V_{vout}}{V_i} = \frac{-g_{mp}}{sC_L + g_{dsp} + 1/R_L} \tag{2.13}$$

Substituting equations (2.12) and (2.13) in equation (2.11), the gain from the power supply to the pre-regulator's output is expressed as in equation (2.14).

$$\frac{V_{vout}}{avdd} = \frac{A_{avdd}^{'}}{1 + \frac{A_0\beta \cdot g_{mp}}{(1+sr_oC_A)(sC_L+g_{dsp}+1/R_L)}} \tag{2.14}$$

The new power gain can be calculated from the small-signal model illustrated in Figure 2.11, and is given by equation (2.15).

$$A_{avdd}^{'} = \frac{sC_{dsp} + g_{mp}\left(1 - A_{avdd}^{amp'}\right) + g_{dsp}}{s\left(C_L + C_{dsp}\right) + g_{dsp} + 1/R_L} \tag{2.15}$$

Now, substituing the equation (2.15) in equation (2.14), the PSRR of the pre-regulator is defined as in equation (2.16).

$$PSRR = \frac{V_{out}}{avdd} = \frac{sC_{dsp} + g_{mp}\left(1 - A_{avdd}^{amp'}\right) + g_{dsp}}{s\left(C_L + C_{dsp}\right) + g_{dsp} + 1/R_L} \cdot \frac{1}{1 + \frac{A_0\beta \cdot g_{mp}}{(1+sr_oC_A)(sC_L+g_{dsp}+1/R_L)}}. \tag{2.16}$$

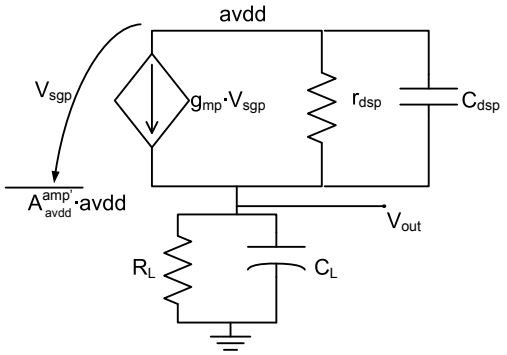


Figure 2.11: Small signal model of the pass transistor considering PSRR analysis.

A typical PSRR curve of a conventional pre-regulator is shown in Figure 2.12. As already demonstrated in equation (2.7), at low frequencies (region 1), PSRR is intimately related to the dc open-loop gain of the error amplifier. The bandwidth of the amplifier, the unity-gain frequency of the system and the pole corresponding to the output impedance impose different behaviours in the shape of the curve. Particularly, the unity-gain frequency represents the worst-case PSRR and it is typically situated in the range $1-10MHz$ (region 2). Intuitively, the loop gain provides high supply-ripple rejection at low frequencies, while the output capacitor shunts any ripple appearing at the output to ground at very high frequencies. Above $100MHz$ (region 3), the effects of parasitic capacitances prevail, and they can be explained as a consequence of large transistors and low impedance nodes.

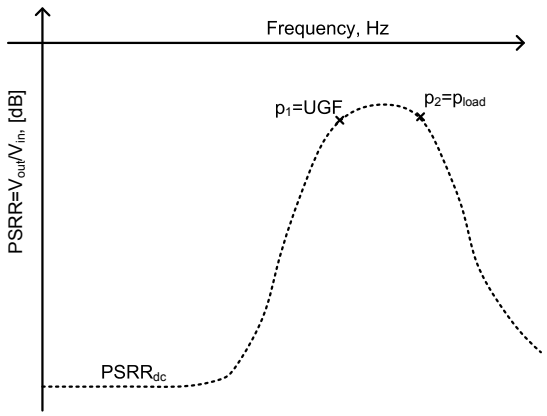


Figure 2.12: PSRR of a conventional linear regulator.

A mathematical expression for the PSRR of the pre-regulator has been obtained and a quantitative approach can be done to achieve high PSRR specifications over the spectrum of frequencies. This method is much more complex than the one presented in [15], although equation (2.16) gives a relatively good approximation to the variables that act upon the PSRR performance of the

pre-regulator. Using $Matlab$® and assigning values for the variables of equation (2.16), the curve of the PSRR over the frequency range is illustrated in Figure 2.13. The PSRR curve obtained has the same behaviour as the one in Figure 2.12 and it is possible to identify the three regions of the PSRR.

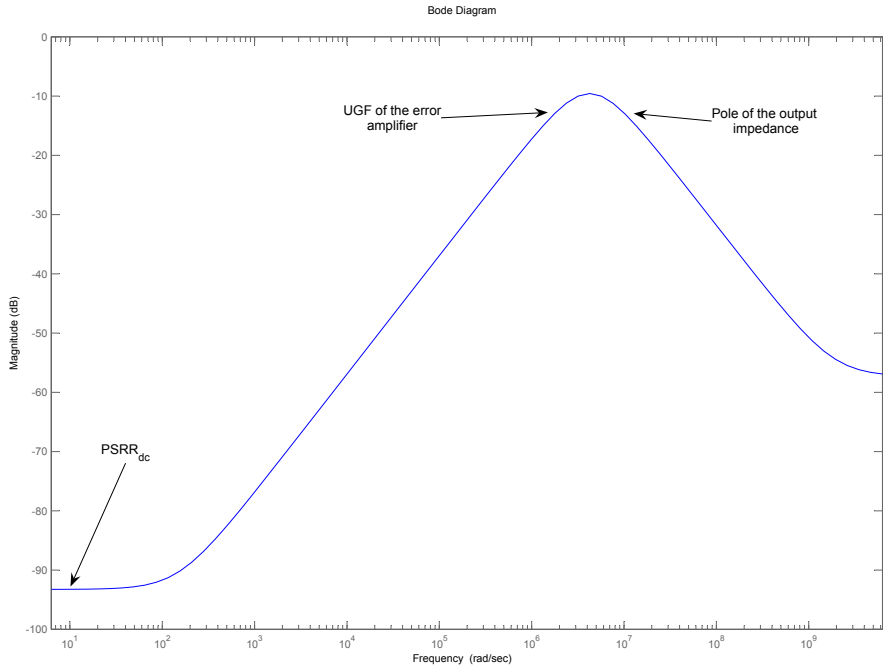
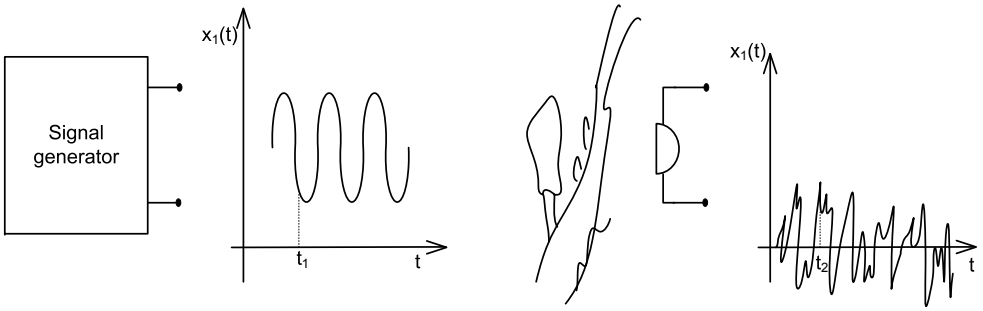


Figure 2.13: PSRR curve of a pre-regulator over a wide frequency range using the proposed mathematical expression.

2.2.2 Integrated Noise

Noise is a random process meaning that the value of noise cannot be predicted at any time even if the past values are known. Intuitively, and using a metaphor, the output of a sine wave generator is compared with that of a microphone picking up the sound of water flowing in a river, as in Figure 2.14. While the value of $x_1(t)$ at $t = t_1$ can be predicted from the observed waveform, the value of $x_2(t)$ at $t = t_2$ cannot. This is the main difference between deterministic and random phenomena. Hence, noise limits the minimum signal level that a circuit can process with acceptable quality. Noise represents a trade-off among power dissipation, speed and linearity.

Thus, another consideration in the ac performance of the pre-regulator can be assigned to the total integrated noise over the band of interest $(f_2 - f_1)$. In a conventional design, the total noise of the regulator is mainly contributed by different noise sources as illustrated in Fig.2.15. The feedback resistors, R_1 and R_2, generate an equivalent noise voltage given by $V_{n,R1}$ and $V_{n,R2}$;



(a) Deterministic phenomena **(b)** Random phenomena

Figure 2.14: Output of different kind of sources

$V_{n,ref}$ is the noise voltage of the reference voltage applied to the pre-regulator and $V_{n,in}$ is the input-referred noise of the error amplifier itself.

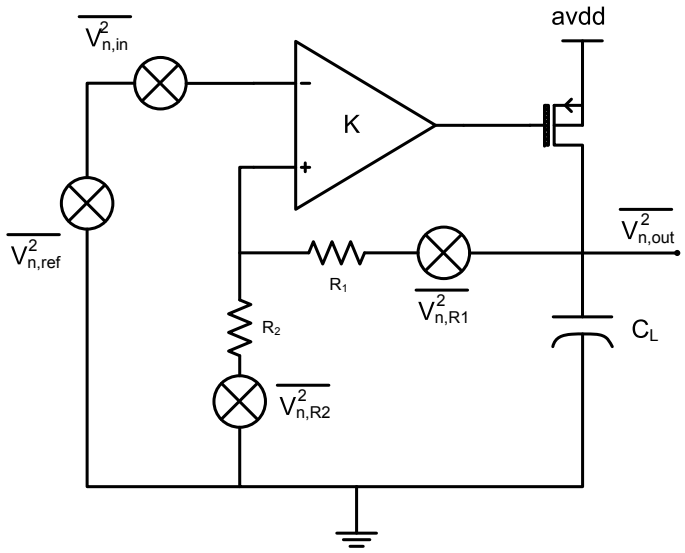


Figure 2.15: Noise sources of a conventional linear regulator.

The total noise power V_{n1}^2 due to the feedback network is given by equation (2.17).

$$V_{n1}^2 = V_{n,R1}^2 + \left(\frac{R_1}{R_2}\right)^2 V_{n,R1}^2 \tag{2.17}$$

The total noise power V_{n2}^2 due to the noise seen at the input of the pre-regulator can be expressed as in equation (2.18).

$$V_{n2}^2 = \left(\frac{1}{\beta}V_{n,in}\right)^2 + \left(\frac{1}{\beta}V_{n,ref}\right)^2 \tag{2.18}$$

In equation (2.18), β is the feedback factor $R_2/\left(R_1 + R_2\right)$. Moreover, the integrated noise related to the output of the pre-regulator, $V_{n,out}^2\left(f_2 - f_1\right)$, is given by equation (2.19).

$$\begin{aligned} V_{n,out}^2 &= \int_{f_1}^{f_2} \left(V_{n1}^2 + V_{n2}^2\right) df \\ &= \int_{f_1}^{f_2} \left(V_{n,R1}^2 + \left(\frac{R_1}{R_2}\right)^2 V_{n,R1}^2 + \left(\frac{1}{\beta}V_{n,in}\right)^2 + \left(\frac{1}{\beta}V_{n,ref}\right)^2\right) df \end{aligned} \tag{2.19}$$

In equation (2.19), $1/\beta$ is the closed-loop gain of the pre-regulator. There are two ways to reduce $V_{n,out}^2$: *(a)* increase the transistor's area of the first stage (such as input pair) and current consumption of the error amplifier in order to reduce V_{n2}^2; (b) reduce the values of the feedback resistors in order to reduce V_{n1}^2. This will, certainly, result in an increase in the quiescent current consumption. In the case of a SoC application, several similar linear regulators can co-exit on the same chip and the increase in area and current consumption can become a serious problem.

For the propose of this thesis, power consumption is a major specification and the feedback resistors used in the pre-regulator must be made as large as possible, in order to reduce the quiescent current that flows in the resistors. One possible way of reducing V_{n1}^2 is setting R_2 resistor larger than R_1 (which conjugates with power consumption proposes). On the other hand, V_{n2}^2 is reduced by increasing, as much as possible, the current consumption of the error amplifier. Furthermore, the differential pair of the error amplifier presents a large area and the current consumption of the amplifier is truly a compromise between total noise considerations and total power consumption.

2.3 Proposed Strategy

2.3.1 Block Diagram

Regarding the latter case-of-study which emphasises the PSRR performance and noise integration of linear regulators, the proposed system to achieve high dc and ac accuracy in the presence of power supply fluctuations and noise is presented in Figure 2.16. The pre-regulator works as a shield to the next analog block which, in this case, is the bandgap reference circuit, although it could be also a low dropout regulator. Any fluctuation in the power supply line is effective and largely attenuated until it reaches the core of the system; thereby, the output voltage reference is more stable and exhibits a high dc and ac accuracy.

Generally, linear regulators use the bandgap voltage as the reference for the error amplifier in order to, accurately, generate the output voltage. Unfortunately, during the system start-up, the BGR is not yet available and, therefore, the power supply voltage shall be used as the reference

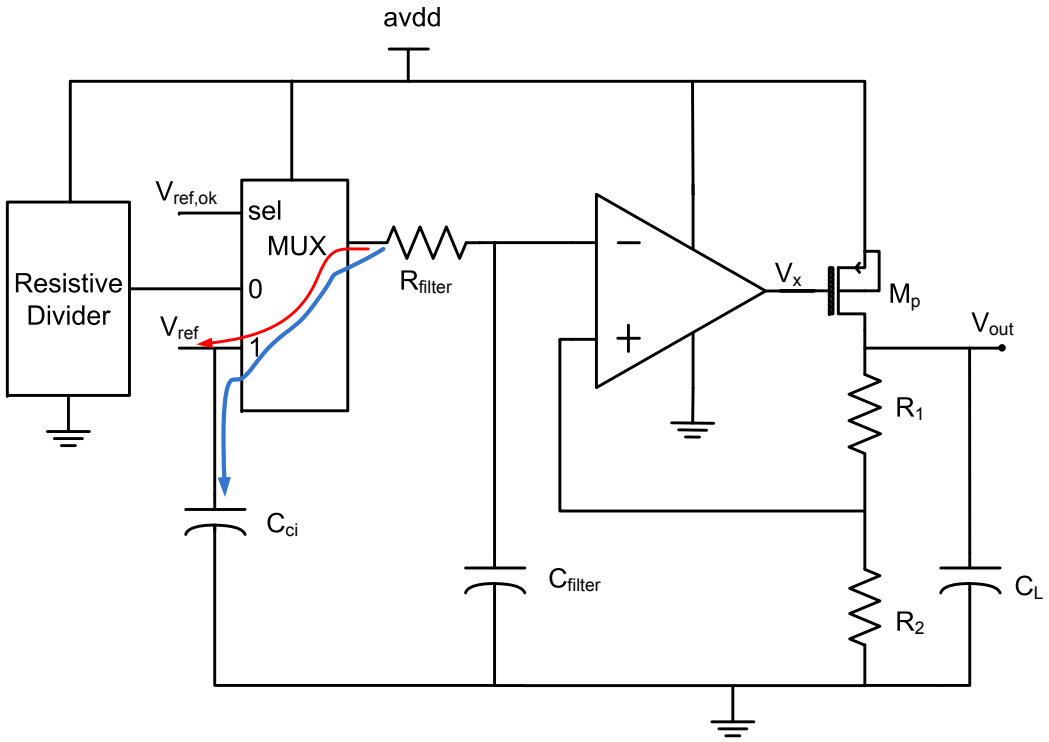


Figure 2.16: The proposed strategy for high PSRR.

for the pre-regulator. In view of that, a switch is introduced between the supply voltage and the bandgap voltage generated by the system. During power-on time, the reference used in the pre-regulator is given by a fraction of the battery voltage to assure that the switching process occurs with the minimum difference between the inputs of the analog multiplexer. At the time that the switching occurs, the pre-regulator's reference suffers a substantial changing in its value. To guarantee that the reference provided is not above the bandgap voltage, R_3 and R_4 resistors need to produce a voltage close to the bandgap voltage when the power supply voltage is equal to $3.6V$, i.e., its maximum value. At this time, the PSRR specifications aren't achieved but that is not a concern since the reference voltage is not yet prepared to supply the next analog blocks in the IP and, obviously, at an higher hierarchical level, the digital validation signal for the reference voltage is low. The PSRR performance of the system is only pertinent when the validation signal is high and that occurs when the multiplexer forces the reference voltage to be the pre-regulator's reference. The capacitance connected to the reference node of the pre-regulator has also to maintain the same value in order to avoid charge injection on the bandgap reference, as illustrated in Figure 2.16. Excluding C_{ci} in the design means that the bandgap voltage suffers a $\delta V/\delta t$ until charges are correctly distributed in the nodes involved (red arrow). A low-pass RC filter has been also added in the output of the multiplexer in order to reduce the voltage peak during the switching process.

This approach conjugates the high PSRR characteristics of the pre-regulators with the re-utilization of the bandgap reference as a stable and constant dc voltage which can be the reference to the circuit that supplies the voltage vital to its generation.

2.3.2 Circuit Design

The schematic of the pre-regulator is illustrated in Figure 2.17. The capacitors used are all MOScap, since linearity is not a concern. The low-pass RC filter is comprised of a $386k\Omega$ (R_5) and $6pF$ capacitor (M_4), which results in a filter pole of roughly $70kHz$. The output capacitance is $7.3pF$, while the capacitor used to compensate charge injection effects in the bandgap voltage reference, M_3, presents a capacitance of $10.4pF$. The total on-chip capacitance utilized is $27pF$. The PMOS pass transistor is always working in saturation region and the error amplifier is simply a single-ended folded cascode.

The feedback loop resistors are designed to accomplish power consumption and integrated noise considerations. R_2 resistor is $3,2$ times larger than R_1. Recalling equation (2.3), that gives the voltage gain of the pre-regulator, and assuming the voltage reference to be $1.2V$, the output voltage of the pre-regulator is equal to $1.5V$. This value is high above the bandgap voltage, and since the pre-regulator's output is the supply voltage for the bandgap core, it, naturally, allows the transistors to be functioning with good margins and with the correct operating point over corner simulations.

The switch is implemented with only two PMOS transistors (M_7 and M_8). The gate signal that enables or disables them is generated in a bandgap voltage validation block, meaning that, when the bandgap voltage reference is low, M_8 source-gate voltage is above the threshold voltage and it is enabled. The switching occurs when the gate signal goes high (bandgap voltage is still converging to the final dc value but almost stable), and the capacitor M_3 avoids charge injection in the reference voltage. The switching is also much smooth, due to the RC filter.

Recalling the schematic of the error amplifier in Figure 2.8, the compensation is achieved by a series RC circuit placed between the power supply and the output of the error amplifier. All the polarization signals are obtained from a master bias cell that is designed in a higher level of abstraction. M_{14} and M_{16} are power-down transistors controlled by the external enable signal. The pass transistor used in the pre-regulator isn't much large because the driving current is strictly the necessary to make the bandgap core to work, added to the load current of the bandgap.

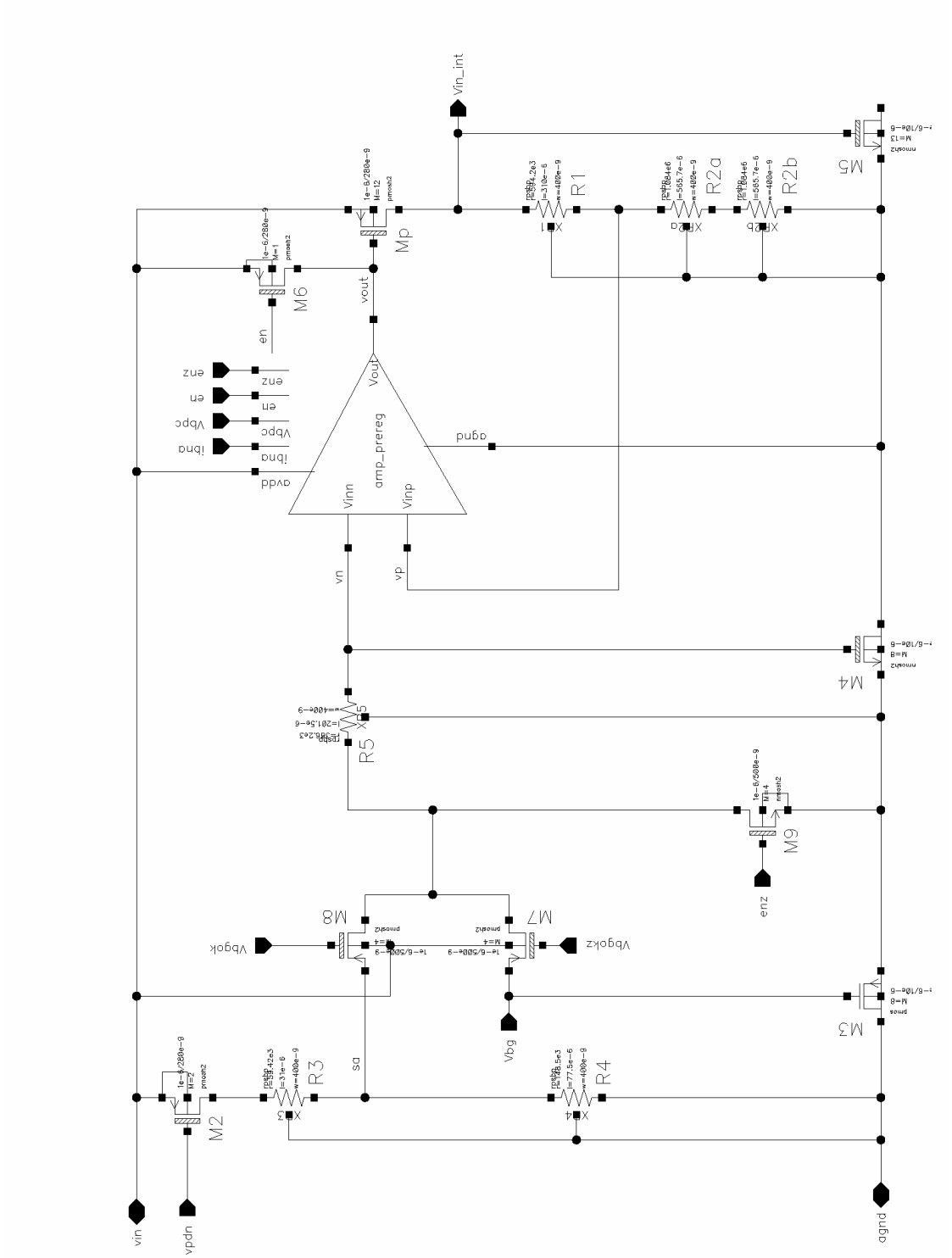


Figure 2.17: Schematic of the pre-regulator: voltage divider, analog multiplexer, error amplifier and pass transistor with the feedback loop.

2.4 Synopsis

State-of-the-Art techniques to achieve high levels of PSRR impose additional complexity to the system, tend to increase the power consumption and to utilise off-chip capacitors. The proposed technique makes use of a pre-regulator which substantially increases the ac performance of the system considering low frequency ripples in the power supply voltage, and on-chip capacitors to suppress high frequency fluctuations. The reference of the pre-regulator is a highly bandgap dependent voltage, since it is forced as the pre-regulator's reference, as soon as it is stable and with the correct dc value. Hence, the immunity of the system to power supply fluctuations is larger comparing to pre-regulator solutions that utilises the power supply voltage as the reference of the pre-regulator. $Matlab$® simulations show that the PSRR of the proposed strategy is able to provide $-93dB$ for low frequencies. The entire pre-regulator uses only $27pF$ of on-chip capacitance and is, thereby, compact as far as die area is concerned.

3

Low Power Consumption

Contents

3.1 Motivation

The density and computing power of integrated circuits are limited primarily by power dissipation concerns. As circuits shrink, sub-threshold leakage current is becoming much more important. This leakage current results in power consumption even when no switching is taking place (static power consumption), and with modern chips this current is frequently more than 50% of power used by the SoC. This loss can be reduced by raising the threshold voltage and lowering the supply voltage. Both of these changes slow the circuit down significantly, and so some modern low-power circuits use dual supply voltages to provide speed on critical parts of the circuit, and lower power on non-critical paths. Some circuits even use different transistors (with different threshold voltages) in different parts of the circuit in an attempt to further reduce power consumption without significant performance loss. Another method used to reduce static power consumption is the use of sleep transistors (act as switches) to disable entire blocks when they are not in use. By shutting down a leaky functional block until it is used, leakage current can be reduced significantly. For some embedded systems that only operate for short periods at a time, this can dramatically reduce power consumption. Since systems that are dormant for long periods of time and ”wake up” to perform a periodic activity are often in isolated locations monitoring some sort of activity, they are, generally, battery powered and power consumption is a key design factor.

In practice, while adiabatic circuits have been built, it has proven very difficult to use it to reduce computation power substantially in practical circuits. The weight and cost of power supply and cooling systems generally depends on the maximum possible power used at some instant. Most desktop computers design power and cooling systems around the worst-case CPU power dissipation at the maximum frequency, maximum workload, and worst-case environment. To reduce weight and cost, many laptop computers systems choose to use a much lighter, lower-cost cooling system designed around a much lower Thermal Design Power, which is somewhat above expected maximum frequency, typical workload, and typical environment. Typically such systems reduce (throttle) the clock rate when the CPU die temperature gets too hot, reducing the power dissipated to a level that the cooling system can handle.

This chapter presents the proposed strategy to achieve the specifications of the work, as far as power consumption is concerned. Along with it, it is, firstly, described the functionality and limitations of the master bias cell block.

3.2 Master Bias Cell

The current generation is the first circuit that must be enabled, since a reference current is needed to polarise the start-up circuit of the bandgap core and the entire pre-regulator block. Furthermore, the only available voltage is the supply voltage, so the dc value of the current may change as the supply voltage; although, the proposed current source is well immune to this con-

sideration. Figure 3.1 illustrates the schematic of the master bias cell, including the auxiliary start-up circuit and the current mirrors that polarise the error amplifier of both bandgap core and pre-regulator, but also the current sources used in the validation block.

The principle is based on applying the emitter-base voltage of a bipolar transistor to a resistor of known value, so that it produces a current of well known value. The topology suffers from the same "'zero-current"' mode issue as the previous typical bandgap structure presented in Section 1.3, so the start-up circuit ensures that this unwanted stable state is never verified, but when the system is in power-down mode.

The whole circuit has many branches which increase the total current consumption, so the objective is to minimize the current flowing in each one. Thus, there is, certainly, a compromise between the current consumption in each branch and the current mirror ratio of the transistors, that is to say, a compromise between power consumption and area. Considering the non-zero-current mode and since the ratio of the current mirror is $1:1$ (M_0 and M_1; M_2 and M_3), the emitter-base voltage of the bipolar transistor, which is loyalty reproduced into node a, generates a current given by V_{EB}/R_1. The start-up sequence of the circuit resumes to:

1. the sleep signal ($vpdn$) goes low and M_9 sleep transistor goes on, along with M_5, which imposes an initial current flowing through M_1 and the bipolar, making the current source to go out of the "'zero-current"' mode;

2. as the voltage at node va increases, M_7 becomes on (M_{10} is already on), which decreases the gate voltage of M_5, forcing it to cut-off;

3. as soon as the reference voltage is stable, $vpdn$ goes high, M_9 and M_{10} cut-off and the only current consumption is given by the current branches of the master bias cell.

The resistor R_1 presents a large value, so it generates a current of roughly $180nA$. This current could be even smaller, but, despite the area costs, it would be comparable with leakage current values which increase as the technology is more and more sub-micrometric. Additionally, a second resistance, R_2, has been placed between M_7 and M_{10}, so it reduces the total current consumption of this block during start-up. Its value is set small compared to R_1, in order to minimize area costs. The current mirrors are designed to have a large channel length, which increases the overdrive voltage of the transistors and also helps minimizing the mismatch between them. Enable - "'en"' - and its complementary, enablez - "'enz"' - signals feed the gates of the PMOS and NMOS power-down transistors, respectively.

The drawback of the topology is to present a large deviation in the dc value of the generated current, due to process variations such as resistance deviation, mosfet and bipolar parameters, as shown in Figure 3.2. This surely implies small variations in the dc value of the bandgap voltage reference, which can be decreased with the discussed resistor trimming. Although this circuit is

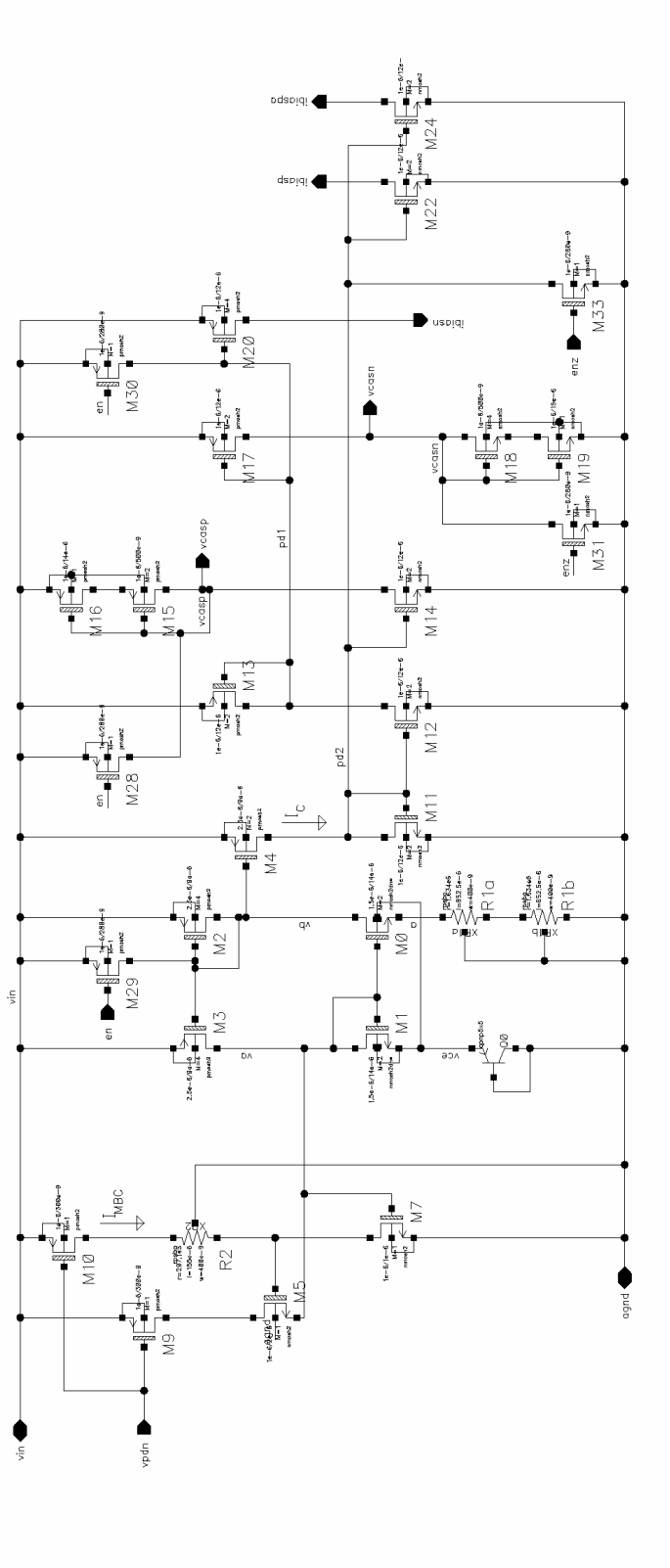


Figure 3.1: Schematic of the master bias cell.

industrially used because the reference current is independent of the instant power supply voltage value.

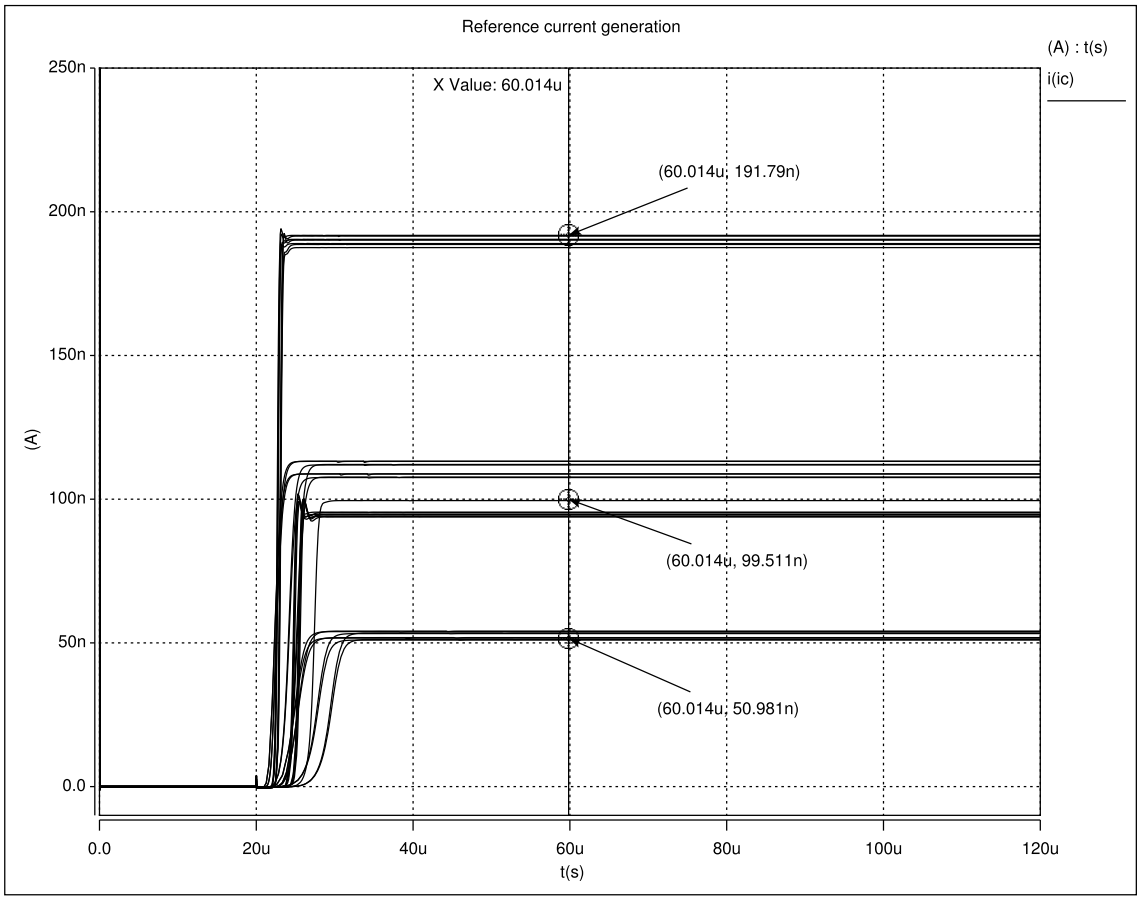


Figure 3.2: Maximum dc deviation of the current source.

3.3 Proposed Strategy

A modern bandgap voltage reference IC results from the conjugation of analog and digital blocks which can be enumerated as a master bias cell; a high PSRR strategy block; and a digital control block that produces a flag signal when the reference voltage is ready to be used in the next analog blocks. Figure 3.3 illustrates a simplified diagram of the sources of power consumption in a reference voltage circuit.

Most of these blocks include start-up circuits to prevent zero mode conditions and also auxiliary circuits that are only used in specific periods of time. The proposed strategy uses transistors that act as switches to disable these blocks when not in use. Besides temperature and process parameter tolerance (ensured through extensive corner simulations), one of the major concerns in this design was to achieve very low power consumption. Therefore, analog blocks are supplied with very low current that still keep them working within the expected specifications in transient

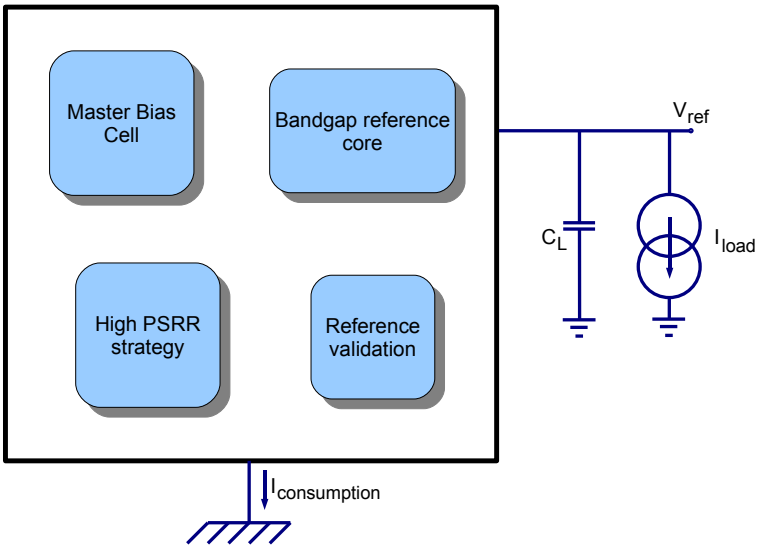


Figure 3.3: Conceptual block diagram of the bandgap voltage reference.

response and temperature sweep analysis.

The power consumption of the proposed bandgap reference circuit can be separated into two parts: during the system start-up time, in which the consumption is mainly due to the current that flows through the current source's start-up circuit and to the current required by the voltage divider used in the pre-regulator; and steady-state mode, where the bandgap voltage reference has already reached its final dc value and is completely stable. The current consumption during the start-up is, typically, three times larger than the one in steady-state mode. This is only true if the bottleneck imposed by the start-up circuit and the voltage divider is overcome, and also if in steady-state mode, these auxiliary circuits are in sleep mode. Moreover, the high ratio between the two consumption states can be reduced making the resistors larger, but the trade-off is certainly the layout area cost.

Thereby, when the reference circuit is in steady-state, the total power consumption resumes to the consumption of the operational amplifier in the bandgap reference core and both branches that feed the inputs of it; the error amplifier and the feedback resistors of the pre-regulator; the reference current generation circuit and current mirroring; and the digital blocks which contribution can be neglected. The circuit design is then focused in reducing the contribution of the bottleneck consumption in steady-state and by supplying the analog blocks with very low current. Figure 3.4 shows a simplified diagram of the proposed strategy to achieve low power consumption and emphasises to the branch currents that being auxiliary (and only needed during the system start-up) shall be cut-off.

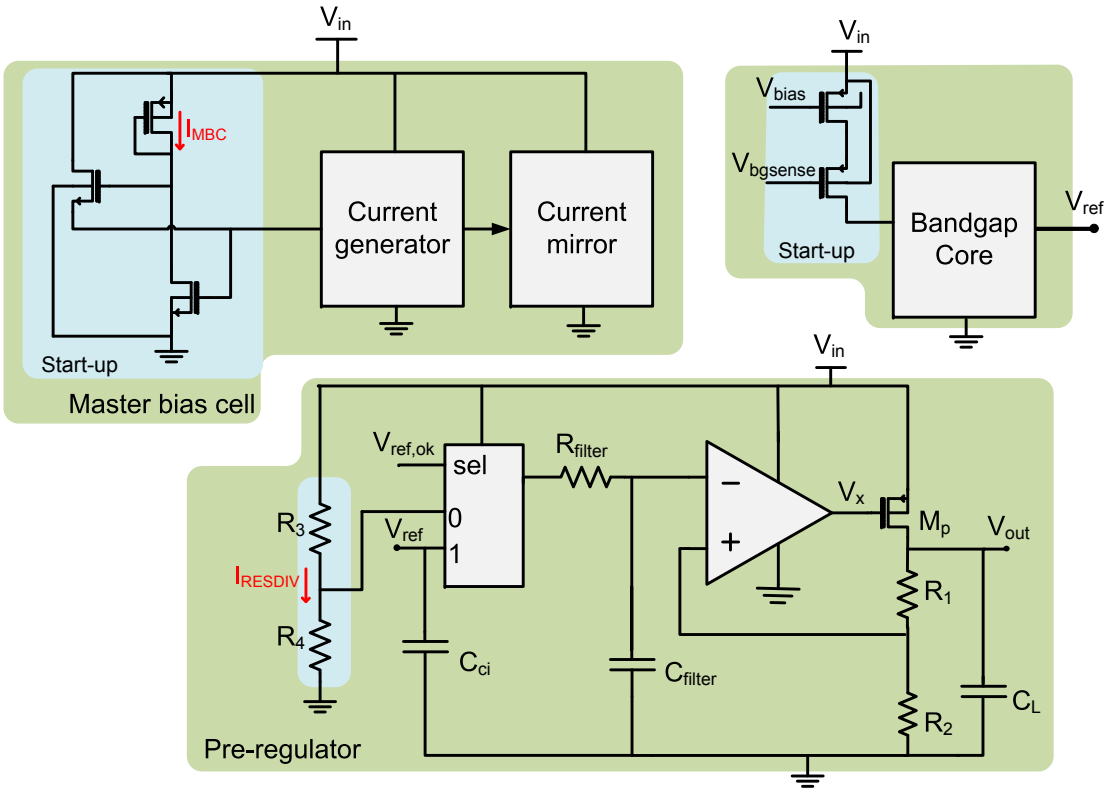


Figure 3.4: Proposed strategy.

3.3.1 Circuit Design

Digital validation of the bandgap voltage is an important feature in the system, because it can be used to reduce power consumption that is only necessary during the start-up. Hence, it is proposed a digital block that senses the bandgap voltage reference and validates it; that is to say, it is able to announce if the reference voltage is already stable and with the correct dc value. The proposed block is illustrated in Figure 3.5.

The W/L relationship of M_1 and M_7 transistors and the delay chain define the reference voltage value at which the signal at the output goes high. The delay time is produced due to a chain of inverters, including a current source that forces a very low current to be driven to the capacitor formed by M_{21}. Thus, increasing considerably the delay time. Typically, the output signal goes high when the bandgap voltage reference has reached 70% of its final value. The capacitance can also be trimmed to ensure a predefined time and that the output signal only goes high after the bandgap value is stable. Hence, the design of the delay chain is completely flexible. In the very start-up of the system, the polarization signal *vbiasp* is zero, so M_{13} and M_{16} transistors ensure that the source of M_1 and M_4, respectively, is actually the supply voltage. On the other hand, when the bandgap voltage reference is zero, M_7 is off and M_1 is on, so the chain of inverters forces the output to be low. Meanwhile, the reference voltage starts to converge to

the final value and M_7 goes on (M_1 becomes off) if its gate-to-source voltage is higher than the threshold voltage; consequently, the output goes high.

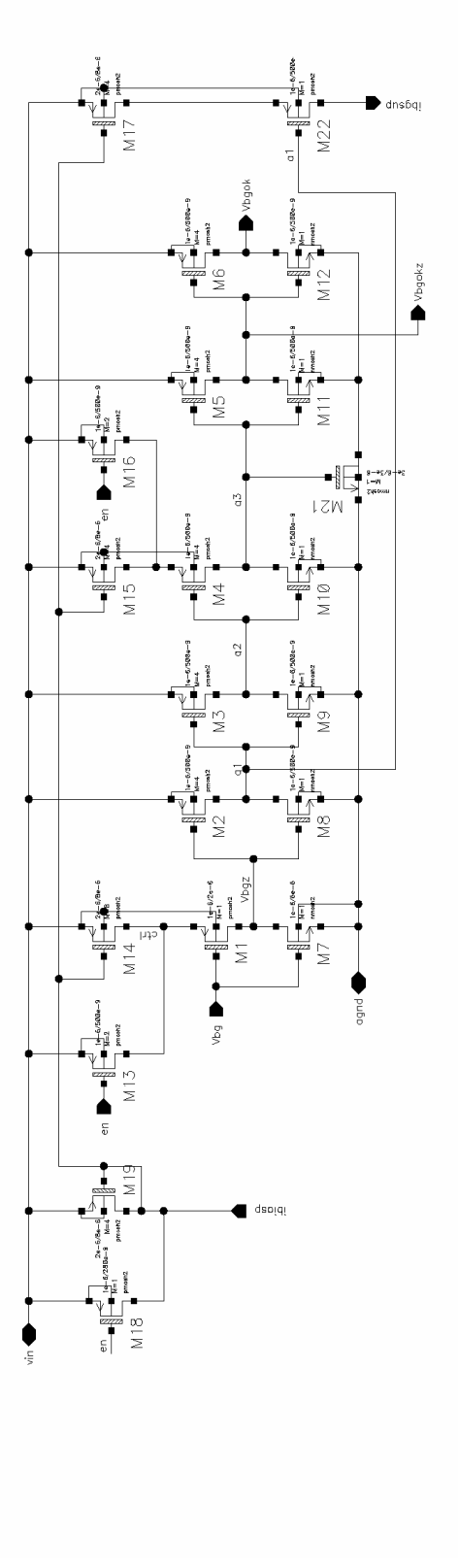


Figure 3.5: Reference validation block.

When the bandgap reference is stable, the power consumption is strictly the necessary to make the system work; that is to say, the auxiliary circuits (used to force the reference voltage during start-up and to avoid the reference convergence to a 0V output) are off. The low power consumption system diagram is presented in Figure 3.7.

When the system is in power-down mode, the validation signal of the reference is low, and since the sleep transistors used in the pre-regulator and master bias cell are PMOS, they would be turned-on. That would, certainly, imply unwanted consumption while the bandgap reference is supposed to be "‘sleeping"’. Hence, an additional "‘nand"’ block is added to the circuit and it prevents this situation to ever happen. Its output only goes low when the system is turned-on and during start-up time, i.e., when the bandgap voltage reference is still converging to its final value. The truth table of the "‘nand"’ block is presented in Table 3.1 and the schematic of the nand is in Figure 3.6.

Table 3.1: Truth table of the sleep signal.

$enable$ ("a")	$\overline{V_{ref,ok}}$ ("b")	V_{sleep} ("$vout$")
0	0	1
0	1	1
1	0	0
1	1	1

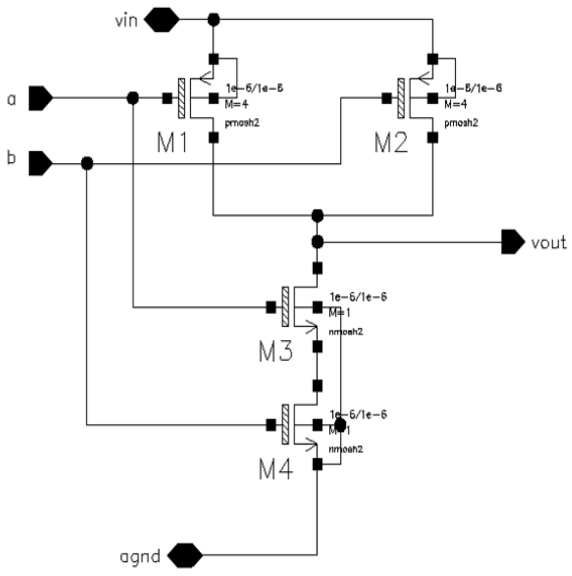


Figure 3.6: Schematic of the nand.

So, the output signal $V_{sleep} = \overline{enable \cdot \overline{V_{ref,ok}}}$ and this is used to feed the gates of the switching transistors (M_2 transistor of the pre-regulator, M_9 and M_{10} transistors of the current source).

The start-up circuit of the bandgap core is also designed in the validation block. It is constituted by a current source (M_{17}), that limits the current that flows in the bipolar of the BGR core, and a switch (M_{22}) that goes off when $V_{ref,ok} =' 1'$.

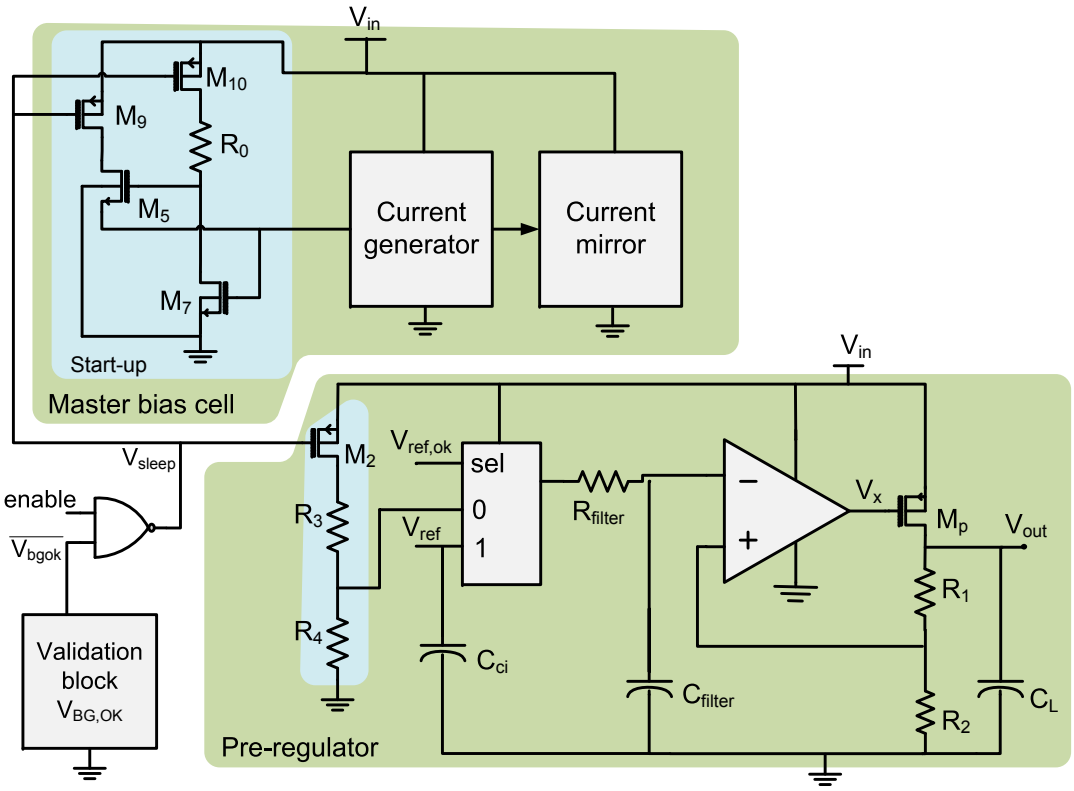


Figure 3.7: System diagram of the low power consumption strategy.

3.3.2 Simulation results

The low power consumption strategy is illustrated in Figure 3.8, where it is only considered the typical case. It was simulated using $Hspice$® and the output load of the digital circuitry is the master bias cell and the pre-regulator. It is clear that the worst situation of current consumption is during the start-up of the system (from $20\mu s$ to about $45\mu s$), where the transistors that act as switches are *on* ($V_{sleep} =' 0'$ and $a1 =' 0'$) and thus, enabling the auxiliary circuits to operate. Note that the validation signal, $V_{bg,ok}$, is low meaning that the BGR circuit is not stable and in the correct state of operation. After this period of time, the validation signal becomes high and the auxiliary circuits stop consuming power. The signal $a1$ that controls the bandgap core start-up circuit also becomes high, disabling it. Table 3.2 summarizes the current consumption of each block used in the simulation testbench.

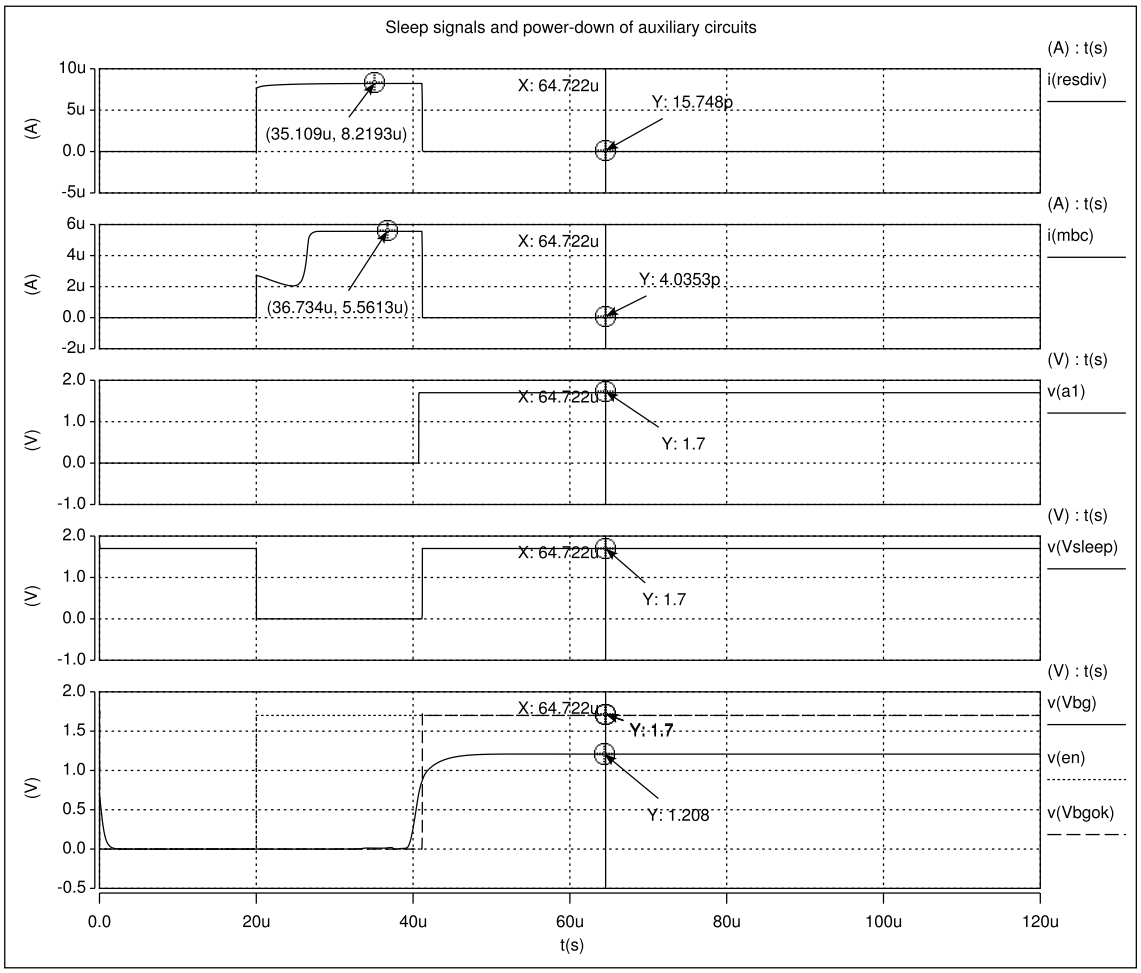


Figure 3.8: Simulation results of the validation signals and sleep mode.

Table 3.2: Current consumption of each block used in the simulation testbench.

Block	Current consumption (μA)
Pre-regulator	1.24
Master bias	1
Reference validation	0.046
Nand	≈ 0

3.4 Synopsis

Along with high immunity to supply voltage fluctuations and average value, independence to temperature sweeps and process variations, modern SoC applications shall present high power efficiency, not only to increase their density and computation power, but also to reduce the weight and cost of power supply and cooling systems in general integrated systems. The proposed strategy, implemented in a 65nm CMOS technology and simulated using $Hspice$®, uses transistors as switches placed in the current path of auxiliary circuits, controlled by digital circuitry that only enables them during the start-up of the BGR. After this small period of time, the reference voltage is able to be used by the next blocks of the SoC and the total power consumption is only given by the consumption of each analog block that constitutes the reference circuit. Furthermore, to guarantee the latter consideration, the analog blocks are fed with the minimum current that still ensures their functionality and specifications.

4

System design

Contents

Based on the proposed techniques, the PSRR performance and the power consumption of the conventional bandgap voltage reference can thus be improved. Chapter 2 presented a pre-regulator strategy as the fundamental block to provide high PSRR performance over the low frequencies of the spectrum and on-chip capacitance to reduce high frequency fluctuations. An analog switch forces the pre-regulator's reference to be the bandgap voltage reference while it is in steady-state. Thus, the PSRR performance is even more effective. The low power consumption strategy presented in Chapter 3 appeals to the use of transistors that act as switches which reduce by three times the total current consumption in the reference circuit. This optimization is possible by introducing digital circuitry that validates the bandgap reference whether it is stable or not. Along with it, the analog blocks are supplied with the minimum current possible to make them work within the specifications. This chapter presents system and circuit level considerations for the integration of the blocks that constitute the reference circuit, in order to build a high PSRR, low power consumption and accurate CMOS bandgap voltage reference IP core.

4.1 Bandgap Core

The bandgap reference core was designed according to the specifications of the work. Recalling the typical bandgap architecture in Figure 1.4 of Chapter 1, PSRR specifications imply that each branch that constitute the inputs of the error amplifier cannot be supplied directly from the supply voltage. Along with this concern, different architectures that include more than two bipolar transistors increase the probability of obtaining errors in the reference voltage (V_{BE} spread) and additional power consumption to the system.

The architecture used for the bandgap reference core is presented in Figure 4.1. This is a usual topology also used in [11] and [16].

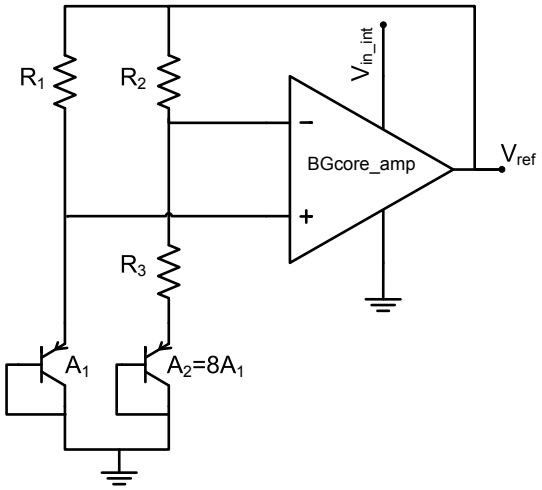


Figure 4.1: Schematic of the proposed architecture for the bandgap reference core.

Notice that this topology also suffers from the "'zero-current"' or off mode, so a start-up circuit must be designed in order to force a non-zero current through Q_1 bipolar transistor that makes the bandgap core to start converging to the correct stable point. Now, recalling the analysis to obtain a mathematical expression for the reference voltage as in equation 1.11, the output reference voltage is given by equation (4.1).

$$V_{ref} = V_{EB1} + \frac{R_1}{R_3}\Delta V_{EB} \tag{4.1}$$

The K factor is then given by R_1/R_3 and the trimming process during the test of IP core has to be done in order to achieve a good temperature coefficient. This is a consequence of not using second-order TC curvature correction, since that would imply an additional complexity, power consumption and area cost.

Now the error amplifier implemented is a single ended folded cascode with an output stage that consists on a PMOS transistor in a common-source topology (M_{10}). The schematic is presented in Figure 4.2. There is no need to buffer the output reference voltage outside the error amplifier, since the load current is completely driven by M_{10} transistor. Besides, the bandgap reference circuit is supposed to drive a small current, so this feature is very useful to reduce area and power consumption because the drain current is strictly equal to the load current. Furthermore, M_{10} provides an increment in the open loop gain of the error amplifier. It is able to drive $10\mu A$ to the next building block without compromising performance.

Cascode transistors (M_4 and M_5) and the input differential pair are working in sub-threshold region, in order to increase the opamp's open loop gain. The folded cascode amplifier has an output resistance given by equation (4.2).

$$r_{o,fc} = r_{ds9} \parallel [g_{m4} r_{ds4} \cdot (r_{ds6} \parallel r_{ds2})] \tag{4.2}$$

Combining equation (4.2) with the output stage, the error amplifier's open loop gain is given by equation (4.3).

$$A_V = \frac{V_{out}}{V_{in}} = g_{m2} g_{m10} r_{ds10} R_L r_{o,fc} \cdot \frac{1}{1 + s\frac{r_{ds10} R_L C_L}{r_{ds10} + R_L}} \tag{4.3}$$

C_L and R_L represent the output impedance of the bandgap voltage reference, r_{ds10} and g_{m10} are the resistance and the transconductance of the output stage, respectively.

The channel length of the current sources (M_3, M_8 and M_9) is large to increase their drain-source resistance, because this helps to shield the high frequency fluctuations from the supply voltage, *avdd*, to the output, the reference voltage. The output stage transistor is designed to always operate in saturation region, for the process conditions taken in consideration (mos and bipolar parameters, resistance deviation, power supply and temperature range). The capacitors M_{11} and M_{12} help to stability and PSRR, respectively. M_6 and M_7 transistors are designed with

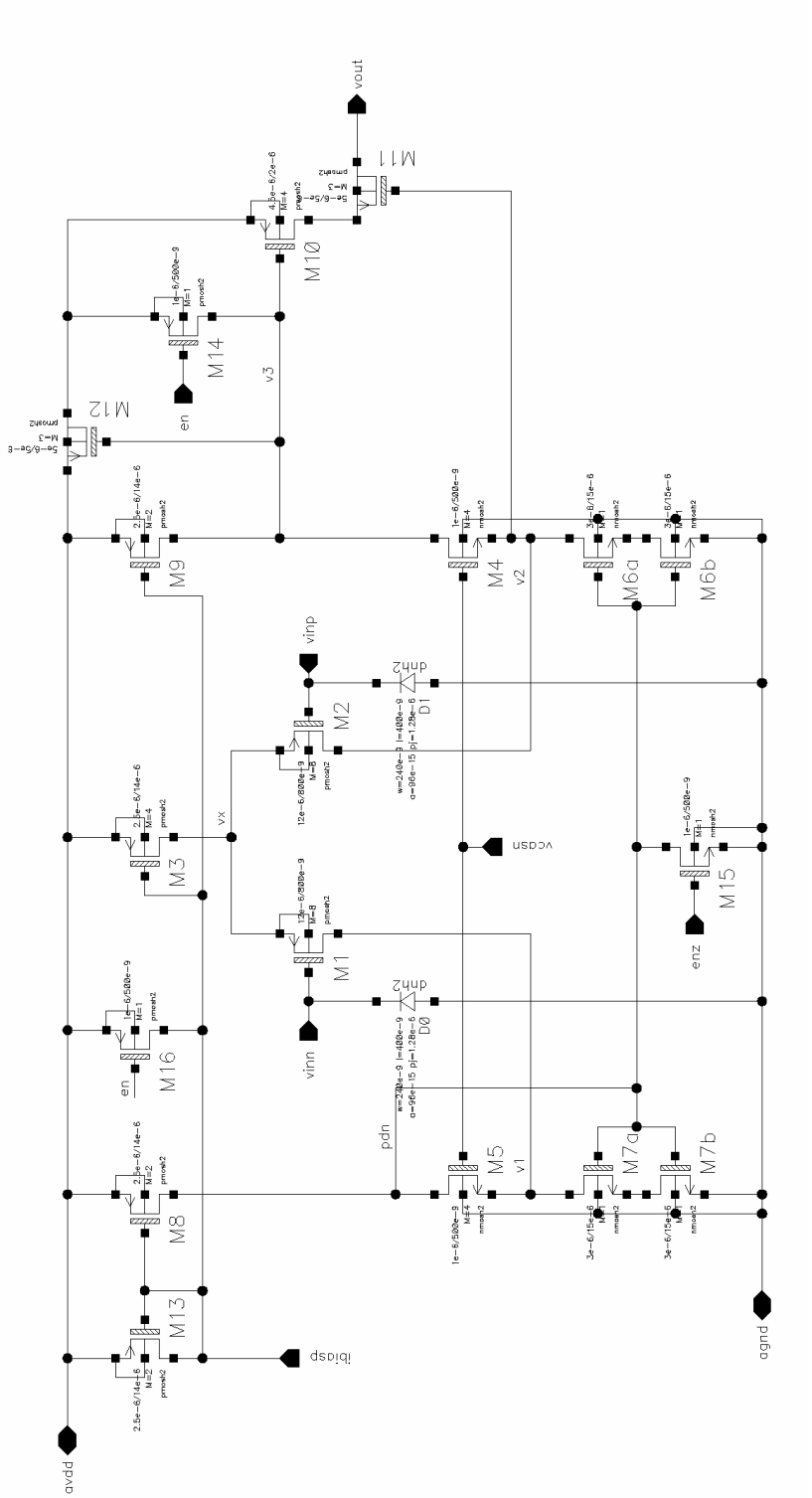


Figure 4.2: Schematic of the error amplifier used in the reference core.

large channel length to ensure a better current mirror and to guarantee that the mismatch between the transistors is even smaller.

Offset voltage was also taken into account as described later in Section 6.1.

4.1.1 Power-down mode

Another consideration has been assigned to the power-down mode (*enable='0'*), where it is supposed that the reference circuit consumes less than $100nA$. That would represent a power-down current consumption that is only 2% of the one in steady-state operation. This process is achieved by introducing a short-circuit between the gate and source of current mirror transistors. Recalling the pre-regulator's schematic from Figure 2.17, transistor M_6 ensures that when enable signal is low, the output of the pre-regulator goes to $0V$, since the PMOS pass transistor cuts-off. Also, M_{14} and M_{16} in Figure 2.8, M_{28}-M_{31} and M_{31} in Figure 3.1 and both M_{14}-M_{16} in Figure 4.2, ensure that the current mirror is completely inactive because the transistors are cut-off. Likewise, the sleep signal is high if $enable = 0$ (due to the nand block), which means that the PMOS transistors that act as switches are cut-off, producing no current consumption in the auxiliary circuits during power-down mode. Also, the start-up circuit of the BGR (in Figure 3.5) is off when power-down mode is enabled because M_{17} is cut-off.

4.2 Circuit Design

The block diagram of the bandgap voltage reference is presented in Figure 4.3. For low power proposes, an experimental study has been done to achieve a good compromise between ac performance and current consumption required by the operational amplifier. The current consumption is the minimum value required to achieve an open-loop gain of $+45dB$, which was considered the minimum required for the BGR specified accuracy of $\pm 5\%$. A lower gain would cause a prohibitive difference between the inputs of the amplifier. Hence, the collector current of each bipolar is set to $1\mu A$ and the error amplifier's current consumption is set to be $500nA$.

The start-up sequence of the proposed reference circuit is initiated by an external enable signal coming from a supply-voltage-based clock generator. The output of the $V_{ref,ok}$ block is low, hence the sleep signal goes also low which makes the current source to start-up and generates the current reference of the circuit. At this moment, the analog blocks start working because the gate voltage of cascode and current source transistors has reached the exact polarisation value. The pre-regulator, which reference is a fraction of the supply voltage, produces the first output voltage that supplies the error amplifier of the bandgap core. Meanwhile, the start-up circuit of the bandgap core allows current flowing through the Q_1 bipolar transistor and thus, the bandgap voltage reference leaves the off mode state and starts converging to the correct dc value. Reaching about 70% of its final value, the output of the $V_{ref,ok}$ block goes high, which makes the

sleep signal to go high as well. This fact allows the system to cut-off the auxiliary circuits and hence to reduce three times the power consumption in the reference circuit. At this time, the pre-regulator switches its reference voltage to the bandgap voltage reference, producing a new stable supply voltage to the error amplifier of the bandgap core. During the switching, charge injection is compensated by introducing equal capacitance between the nodes. The bandgap voltage reference is now stable and with the correct dc value of $1.208V$ at $50°C$. The system keeps this state until power-down mode is activated.

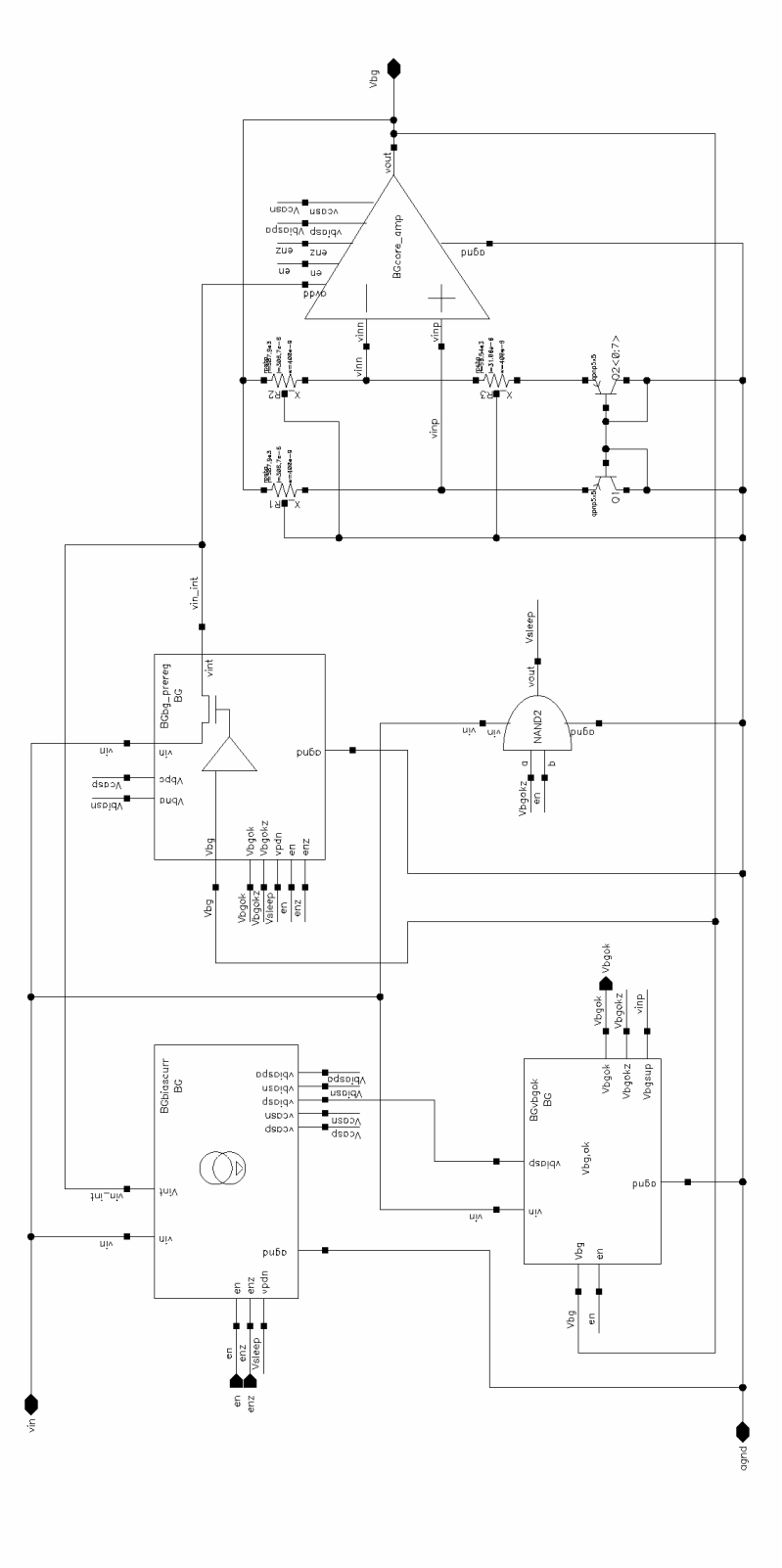


Figure 4.3: Diagram of the proposed bandgap voltage reference circuit.

5

Simulation results

Contents

After defining the blocks that constitute the proposed bandgap voltage reference in the previous chapters, the schematics were implemented using the schematic editor from *Cadence*® *Virtuoso*® Custom IC Design tools and $TSMC$® 65nm CMOS technology. The simulations were done using *Hspice*®.

5.1 Default Simulation Conditions

The characterization of the proposed bandgap voltage reference has been done with some dynamic parameters such as supply voltage, output bandgap voltage, output load current and temperature. In order to verify the functionality of the designed reference, MOS and bipolar parameters, along with resistance deviation have been introduced into the simulation. Table 5.2 presents the corners idenfitication.

Table 5.1: Corner identification.

Corner	**Supply voltage (V)**	**Temperature (°C)**	**Resistance ($\%$)**	**MOS and Bipolar**
Best	3.6	-40	-30	FastFast
Typical	-	50 (ROOM)	-	Typ
Worst	1.7	125	+30	SlowSlow

The simulation setup diagram is presented in Figure 5.1.

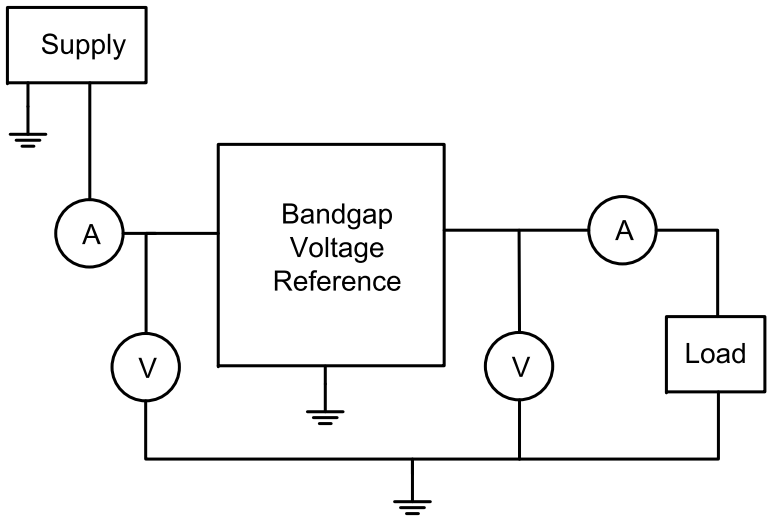


Figure 5.1: Test setup diagram.

The load block is constituted by an output impedance equal to a $1pF$ capacitance in parallel with a $120k\Omega$ resistance; hence, the driving current of the reference circuit simulated is roughly

$10\mu A$ since the reference voltage is expected to be $1.2V$.

5.2 Transient

Figure 5.2 shows the power-up response of the bandgap voltage reference. As soon as the *enable* signal goes high at $20\mu s$, the output voltage of the bandgap core leaves the "zero-current" mode and it starts converging to its final value. Typically, the stable dc voltage of the reference circuit is $1.208V$, when the system is at room temperature. Considering the 32 corners of the simulation, the deviation in the stable dc voltage between the maximum and minimum corners is $38.2mV$ which is within the specified accuracy reuse of $\pm 5\%$.

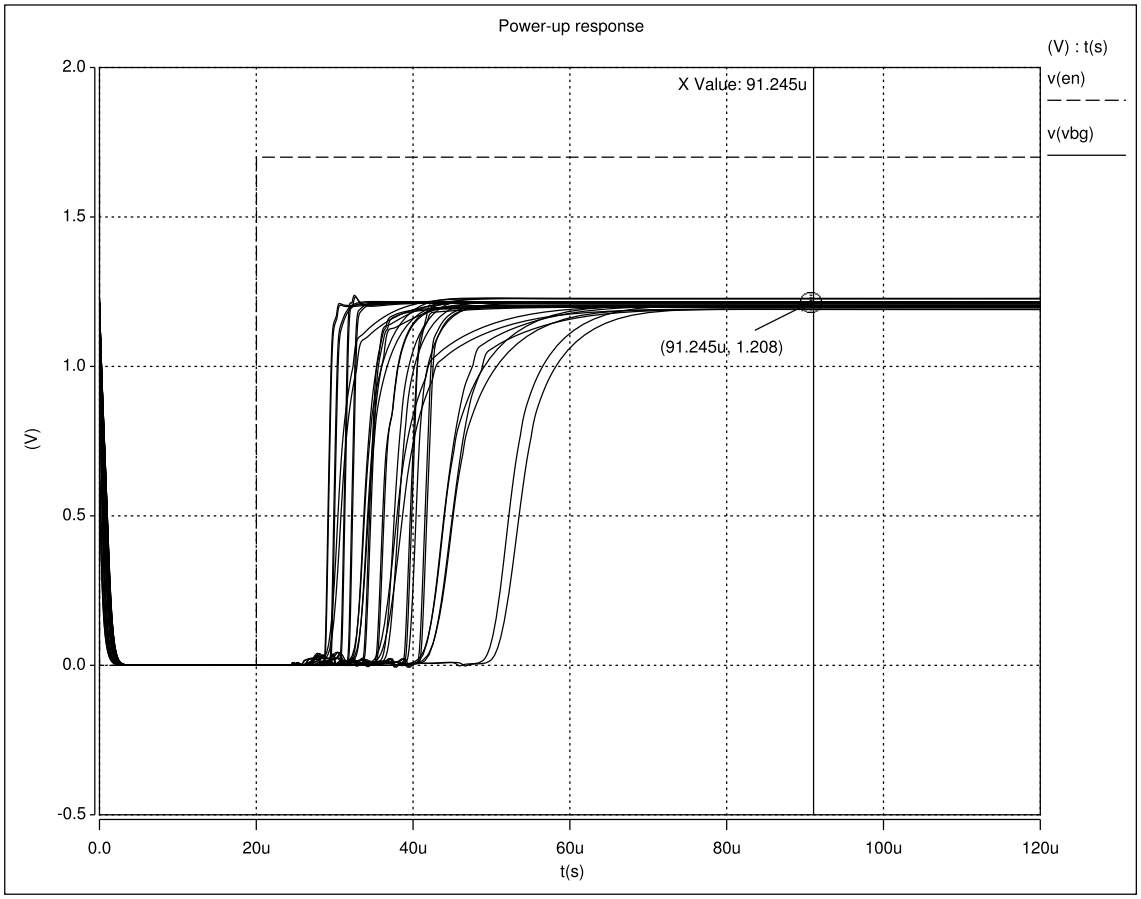


Figure 5.2: Power-up response of the reference circuit.

Figure 5.3 shows the system start-up time where, in typical case, it takes $32.2\mu s$ to reach the correct dc value. The worst corner in the transient response ($V_{in} = 1.7V$, $T = 125^{o}C$, slow resistor, fast bipolar, slow-slow mos) takes $56.6\mu s$ and the best corner ($V_{in} = 3.6V$, $T = -40^{o}C$, fast resistor, slow bipolar, fast-fast mos) takes $20.2\mu s$. Naturally, the bandgap reference circuits are faster with higher supply voltages and low temperature.

The power-down mode is illustrated in Figure 5.4 and it demonstrates that the reference vol-

tage goes to $0V$ right after $4\mu s$. On the other hand, the sleep signal goes high in order to cut-off the transistors that act as switches of the pre-regulator and master bias cell.

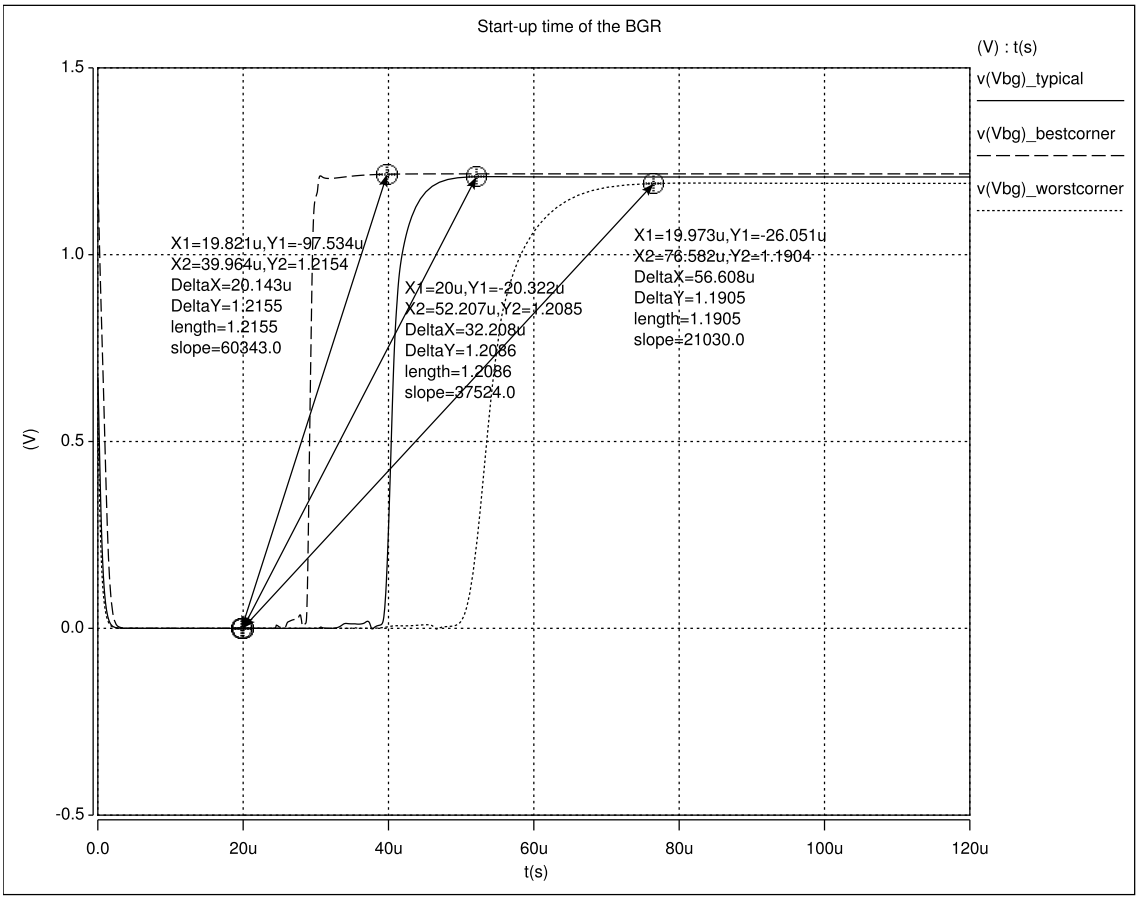


Figure 5.3: Start-up time response of the reference circuit.

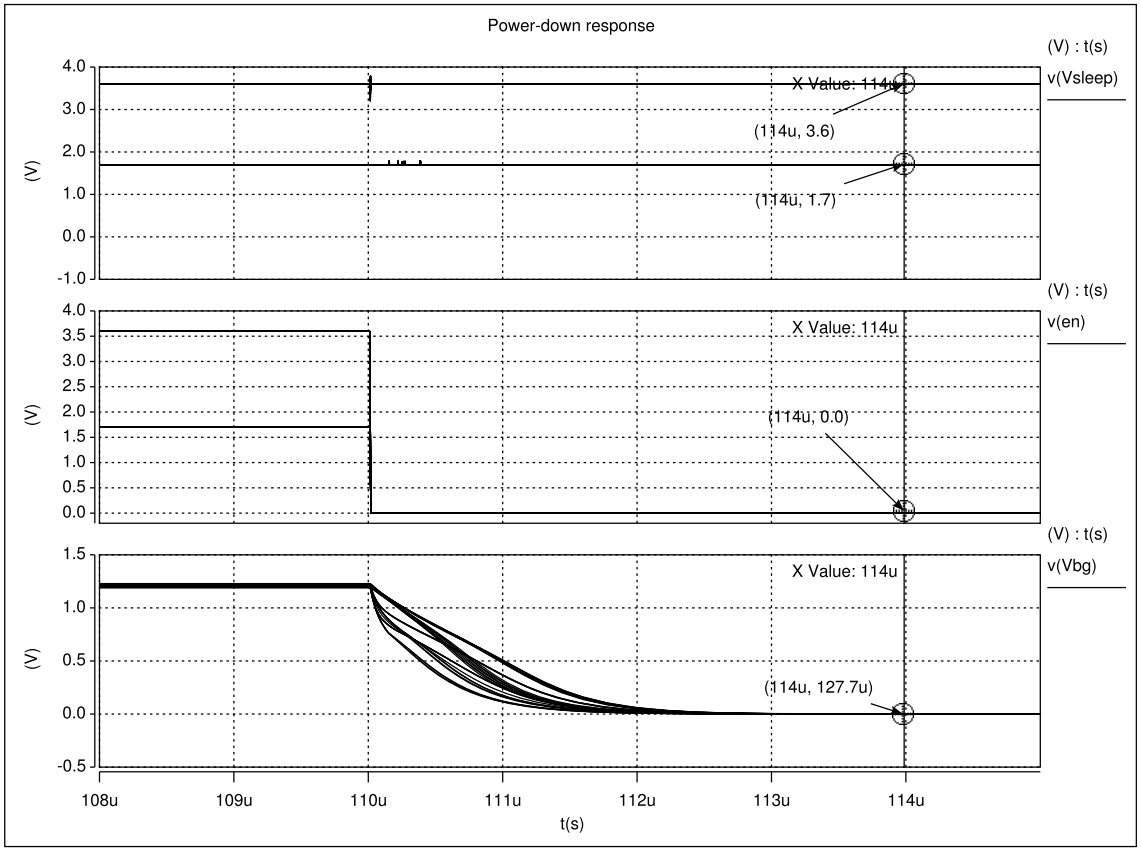


Figure 5.4: Power-down mode of the reference circuit.

5.3 PSRR Performance

The PSRR simulations demonstrates the effectiveness of the proposed strategy presented in Chapter 2. Figure 5.5 shows a comparison between the PSRR performance obtained with and without using the pre-regulator. The difference is $-67dB$ for low frequencies, and the bandgap performance with the pre-regulator at high frequency is a consequence of using decoupling capacitors. The use of the pre-regulator is, indeed, a great way of obtaining good ac accuracy, and especially until the error amplifier of the pre-regulator is still able to sense perturbations and compensate them.

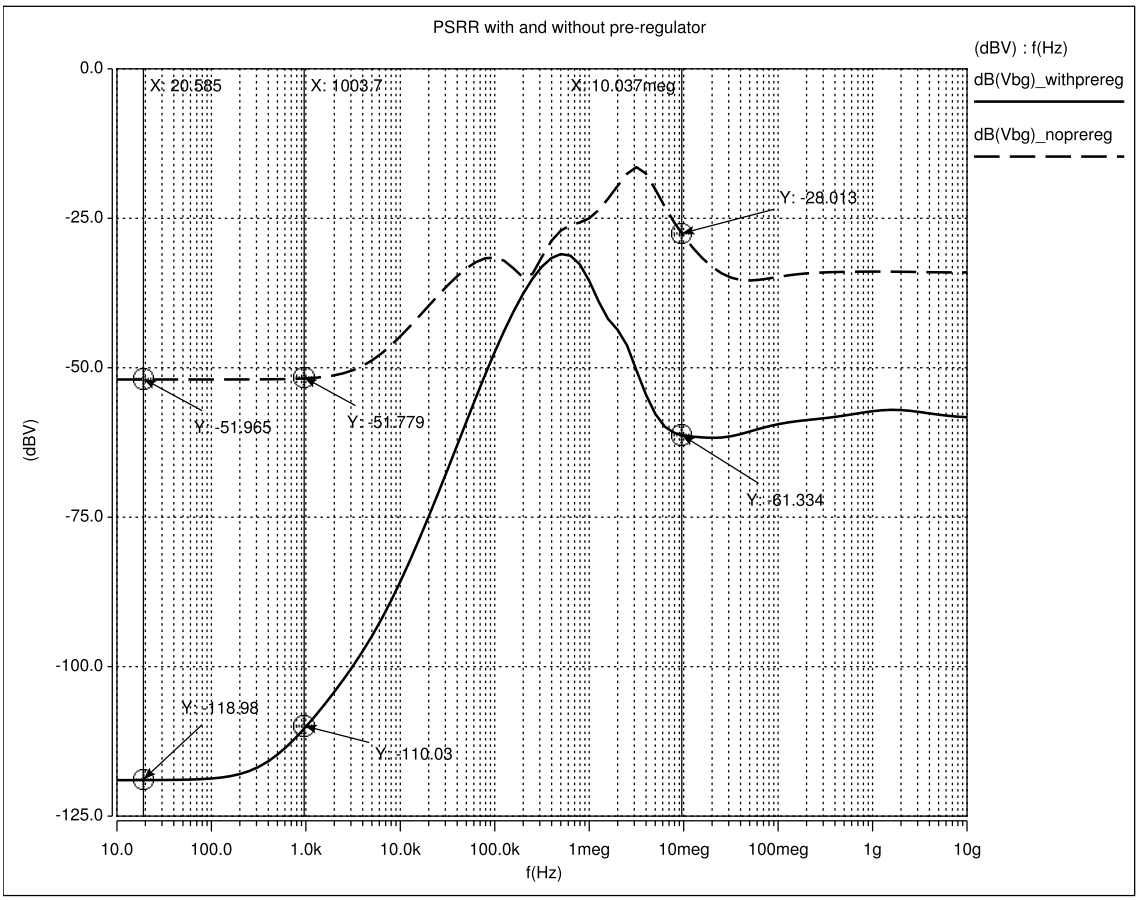


Figure 5.5: PSRR comparision.

The PSRR of the proposed reference circuit is shown in Figure 5.6, considering corner simulations. It is visible the three regions of a typical PSRR curve as Figure 2.12 suggested. The simulated PSRR entirely meets the primary specifications. At low frequencies and considering the typical corner, the BGR is able to attenuate the power supply ripples by $-118dB$, meaning that a ripple with $100mV$ of amplitude reaches the output of the circuit with $0.126\mu V$. At $1kHz$, the worst corner presents $-76dB$ which is, even though, below the primary specification of $-70dB$ for the typical corner. On the other hand, the best corner reaches $-112dB@1kHz$. The unity gain

frequency of the BGR is around $200kHz$; the minimum PSRR performance is $-22.79dB@500kHz$ when the supply voltage is $1.7V$, the temperature is -40^oC, the resistors are fast, bipolars are slow and mos are slow-slow. The usual switching frequency of a modern DC-DC converter is $2MHz$ and the PSRR of the BGR at this frequency is $-43.7dB$ (typical) and $-37.2dB$ in the worst corner ($V_{in} = 1.7V$, $T = 125^oC$, fast resistors, slow bipolars and slow-slow mosfets). Finally, the PSRR performance at the specified frequency $10MHz$ was set to $-40dB$ and the simulation results show that it is $-61.3dB$ (typical), $-59.8dB$ in the worst corner ($V_{in} = 1.7V$, $T = -40^oC$, slow resistors, slow bipolars and fast-fast mosfets) and $-65.7dB$ when the battery supply is $3.6V$, temperature is 125^oC, resistors are fast, bipolars are slow and mosfets are fast-fast. Considering a Charge Pump IP with a switching frequency of $1.5MHz$, the ripple is attenuated by above one hundred times at the output of the BGR (typical).

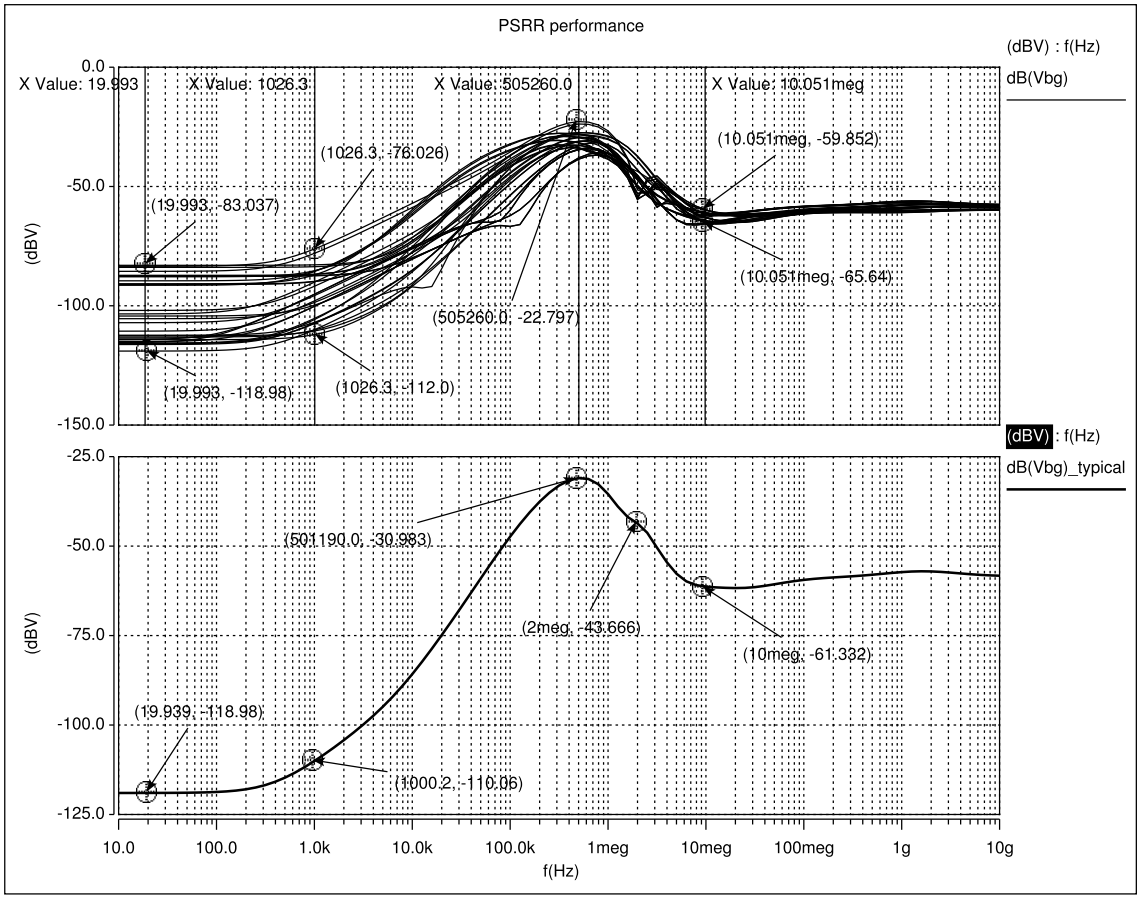


Figure 5.6: PSRR of the proposed reference.

5.4 Power Consumption

In steady-state operation, the total current consumption of the bandgap reference is illustrated in Figure 5.7. The typical corner shows a current consumption of $4.9\mu A$ which is below the primary specification of $5\mu A$. The total voltage source power dissipation is $25.2\mu W$.

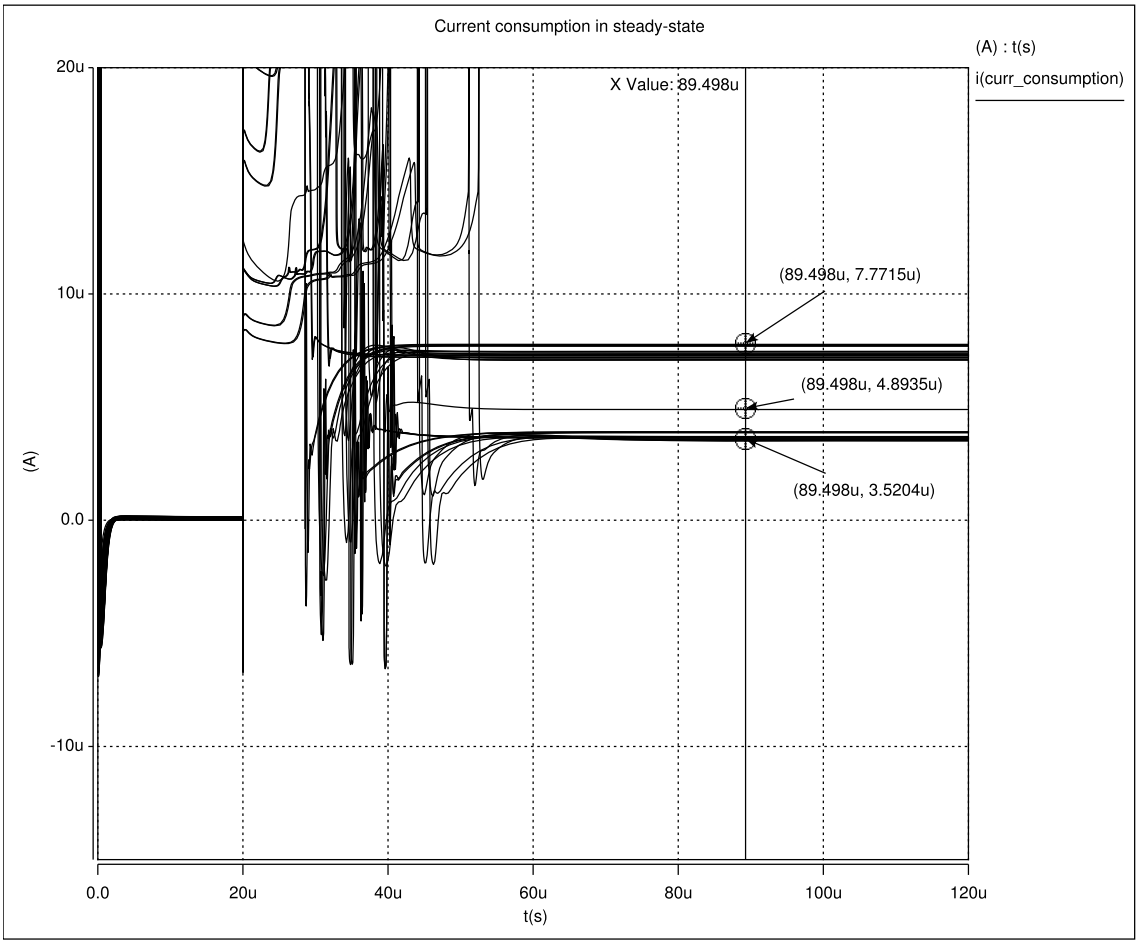


Figure 5.7: Total current consumption in steady-state.

The current consumption of the bandgap reference circuit is mainly given by the analog blocks as illustrated in Figure 5.8.

During the start-up of the system, the current consumption is the worst case ever, as shown in Figure 5.9. Typically, the mean value is around $15\mu A$ and the start-up circuit of the master bias cell and the resistive divider of the pre-regulator are the responsible for the high current consumption in this period of operation. The voltage peaks are due to digital switching and they don't represent any issue in terms of current density because they only occur for few ns.

Figure 5.10 shows the current in each block when power-down mode is activated ($enable =' 0'$) and, typically, the power consumption is below $100nA$ which is a good achievement. This value represents, approximately, 2% of the total power consumption when the bandgap reference circuit

is enabled, stable and with the correct dc value.

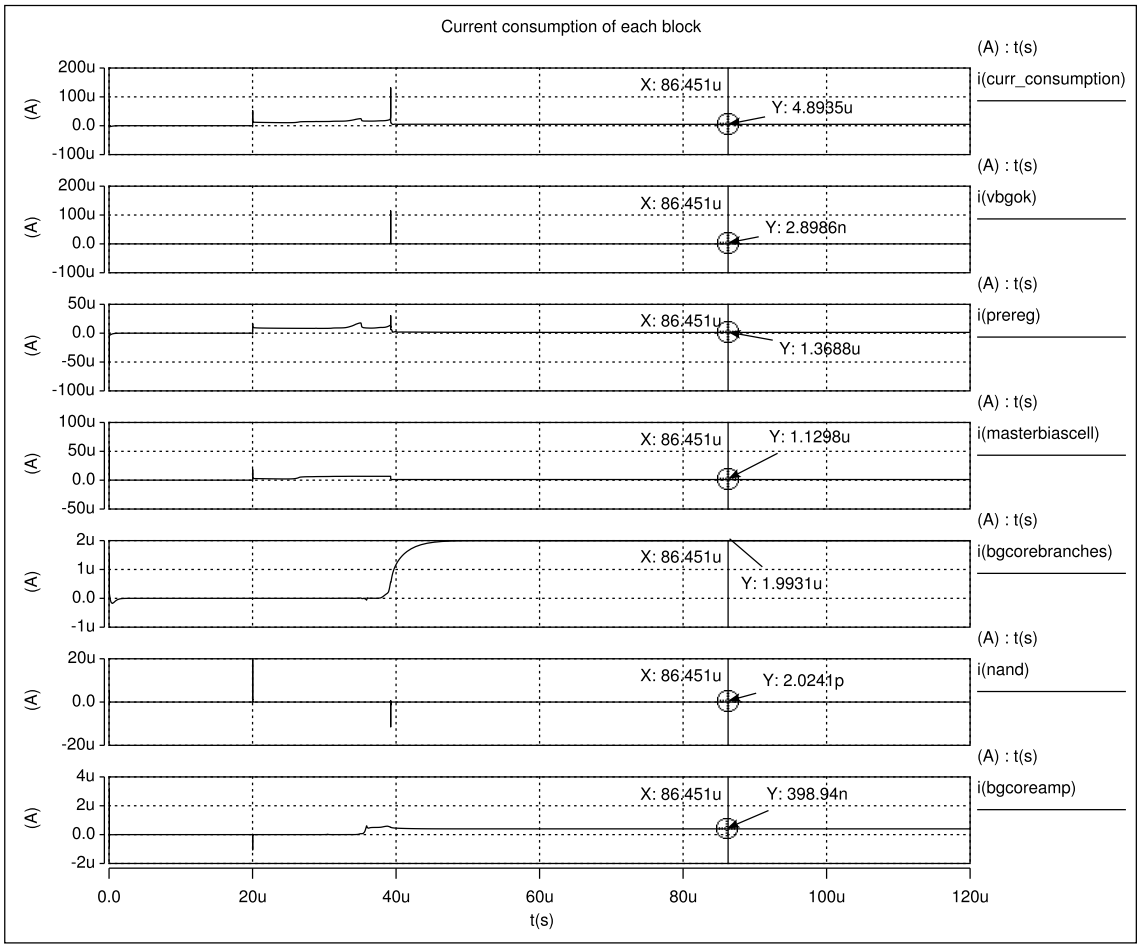


Figure 5.8: Current consumption of each block.

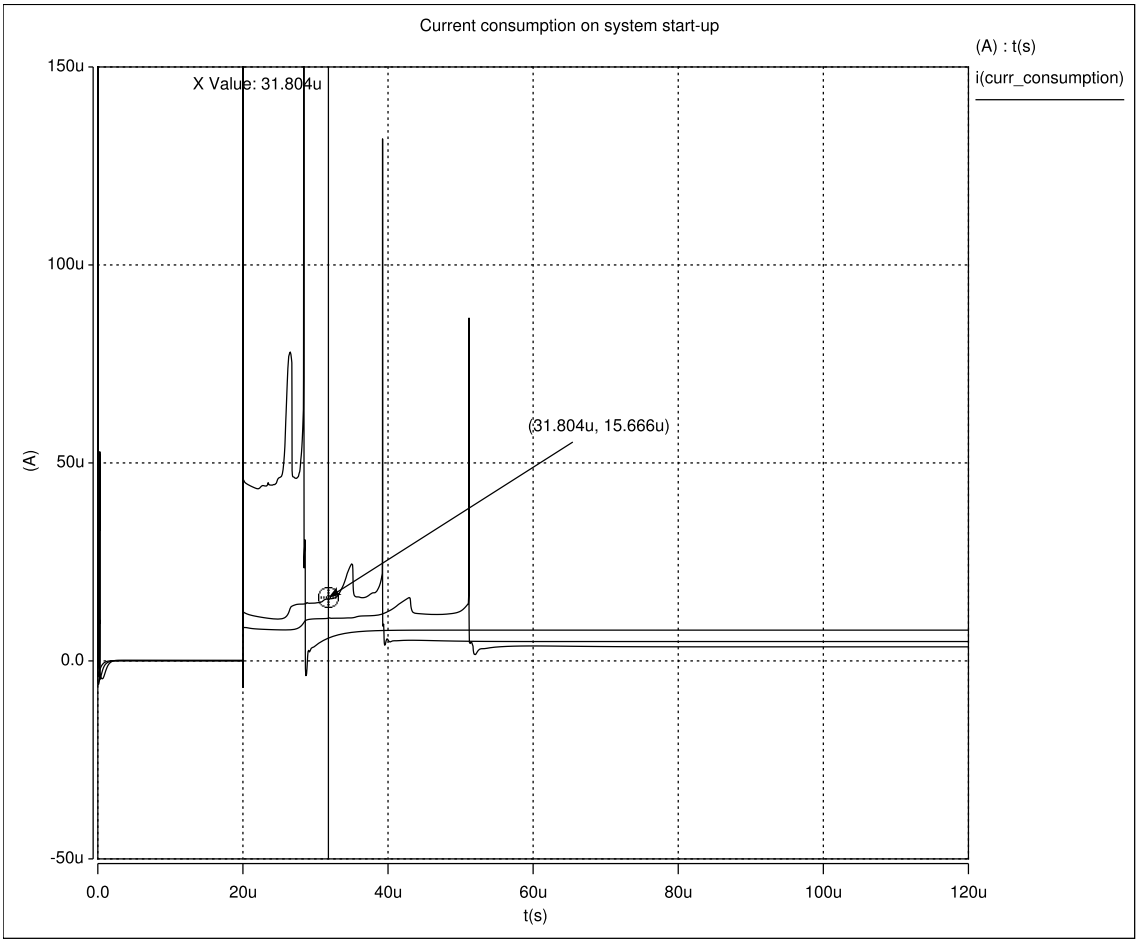


Figure 5.9: Total current consumption during start-up time.

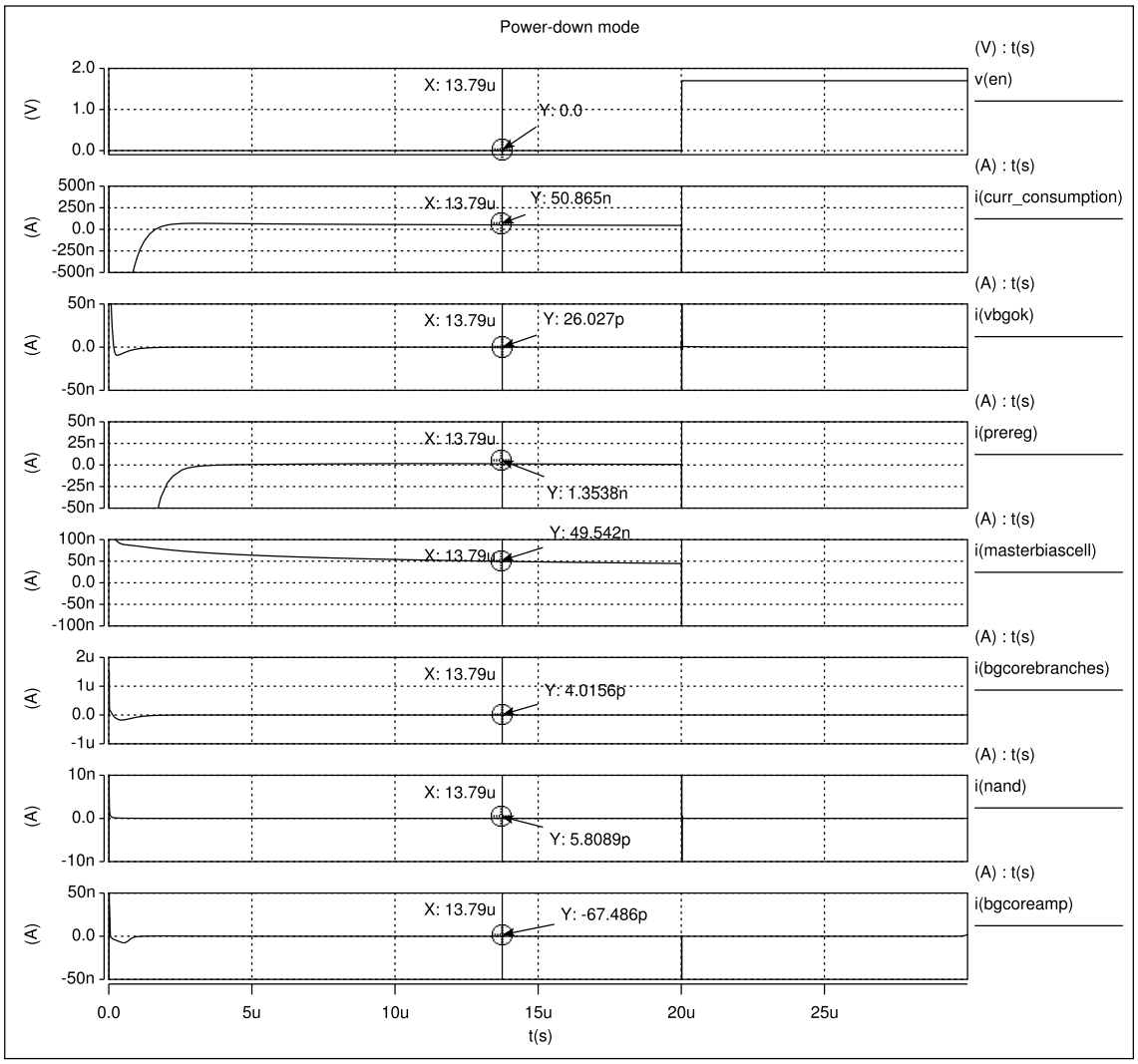


Figure 5.10: Power-down current consumption.

5.5 Temperature Curvature

The temperature curvature of a BGR circuit is also a vital result to the good functionality of the core over different environments. Figure 5.11 presents the temperature curvature of the proposed reference considering 16 corners. They are organised in four groups plus typical and their concave bell shape is intimately related to fabrication technology, particularly, the bipolars, mosfets and resistors.

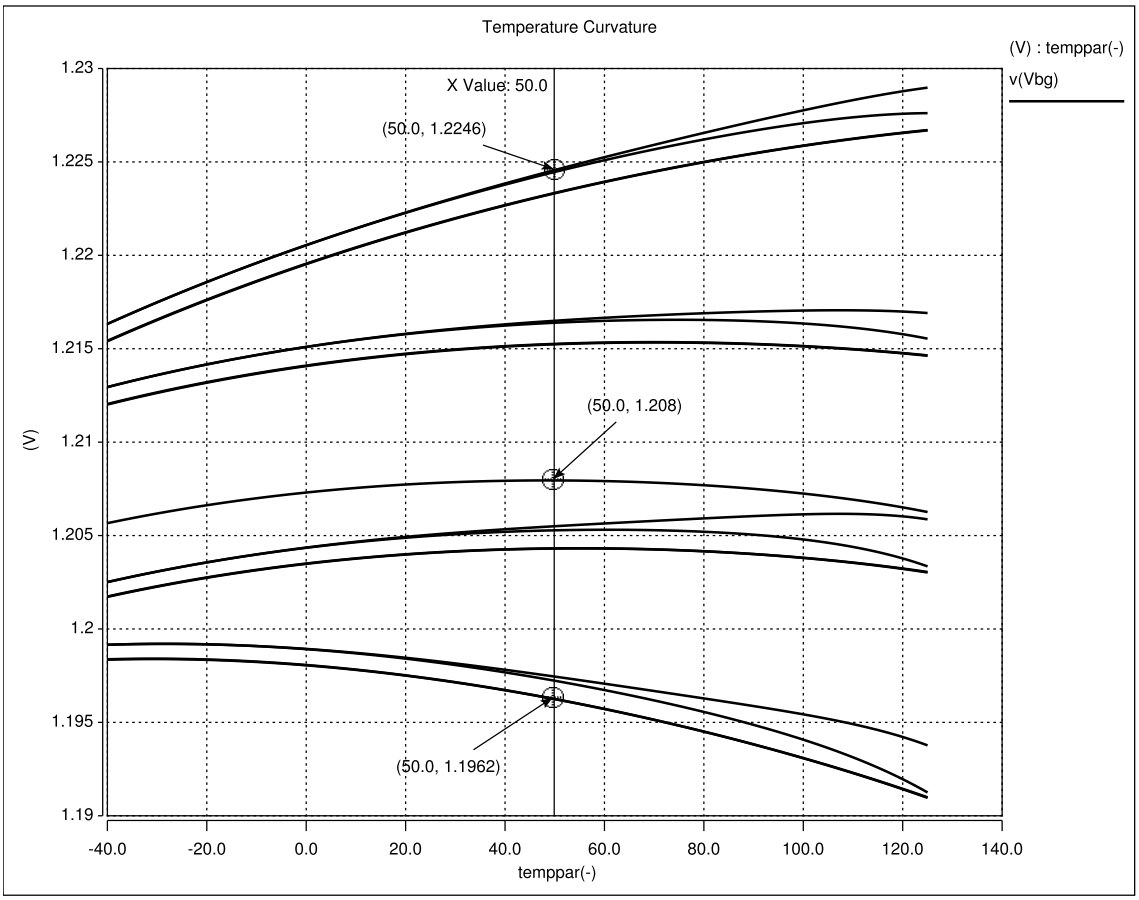


Figure 5.11: Temperature sweep.

Considering room temperature, the bandgap voltage reaches a maximum dc deviation of $28.4mV$ from typical.

Figure 5.12 isolates the typical and maximum deviation corner and it can be used to evaluate the temperature coefficient (TC) value of the bandgap reference circuit. Recalling the definition of TC from equation (1.14), the dependence to temperature of the proposed BGR circuit is $(1.2063 - 1.2057) / (165 \cdot 1.208) \simeq 3ppm/^{o}C$. During the functionality test process of the bandgap voltage reference, it is imperative to trim the value of the resistors that generate the bandgap reference, in order to obtain the lowest temperature dependence which is, in fact, the typical. The worst corner shows that the maximum TC is $(1.229 - 1.2163) / (165 \cdot 1.208) \simeq 64ppm/^{o}C$.

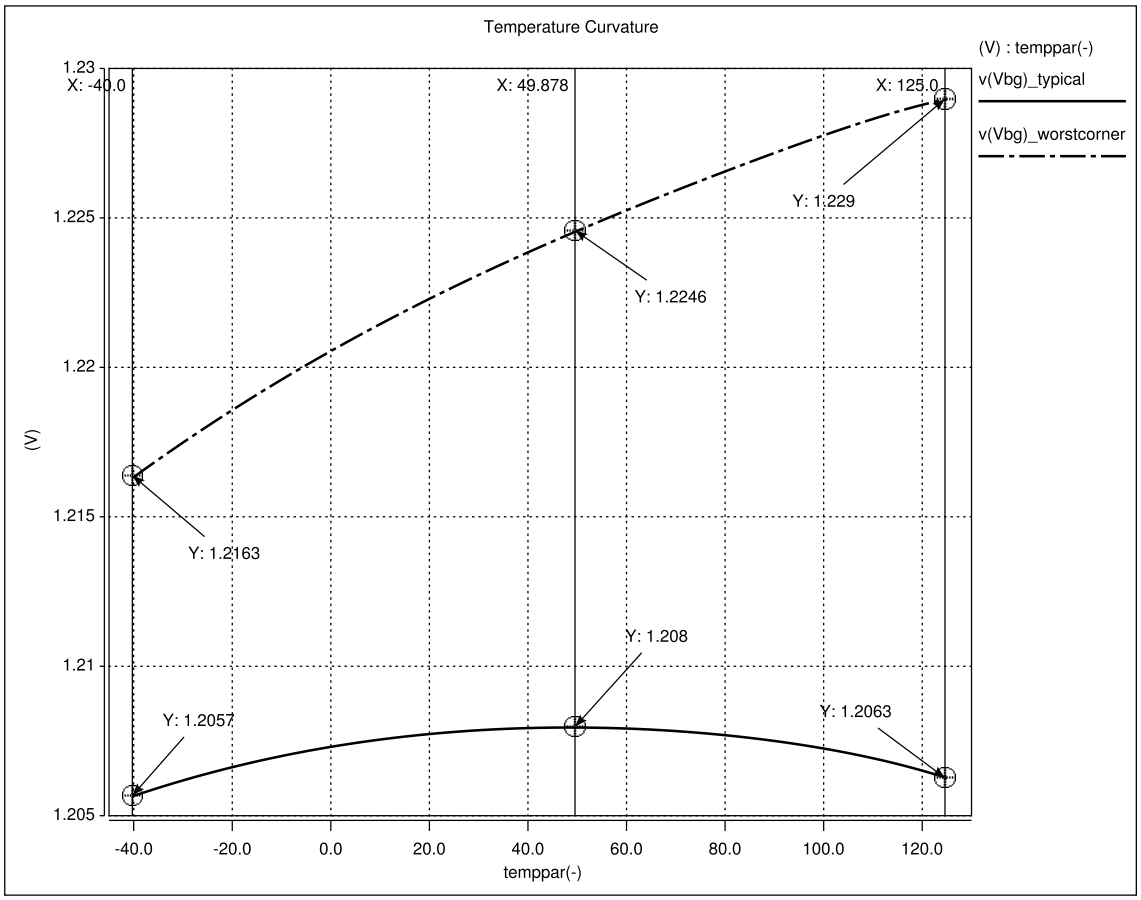


Figure 5.12: Curvature of the worst and typical corners.

5.6 Monte Carlo

The reliability of the designed bandgap reference circuit is simulated using a Monte Carlo analysis with 100 rounds that sweeps the reference voltage between the minimum and maximum temperatures. Figure 5.13 shows that the reference voltage is well concentrated around $1.2V$, although there are a few curves that represent cases in which the probability of occurrence is very low, thus, they are outside the $3 - sigma$ boundary and thus can be neglected. The offset of the bandgap voltage compared to the ideal $1.2V$ is $50mV$ at room temperature.

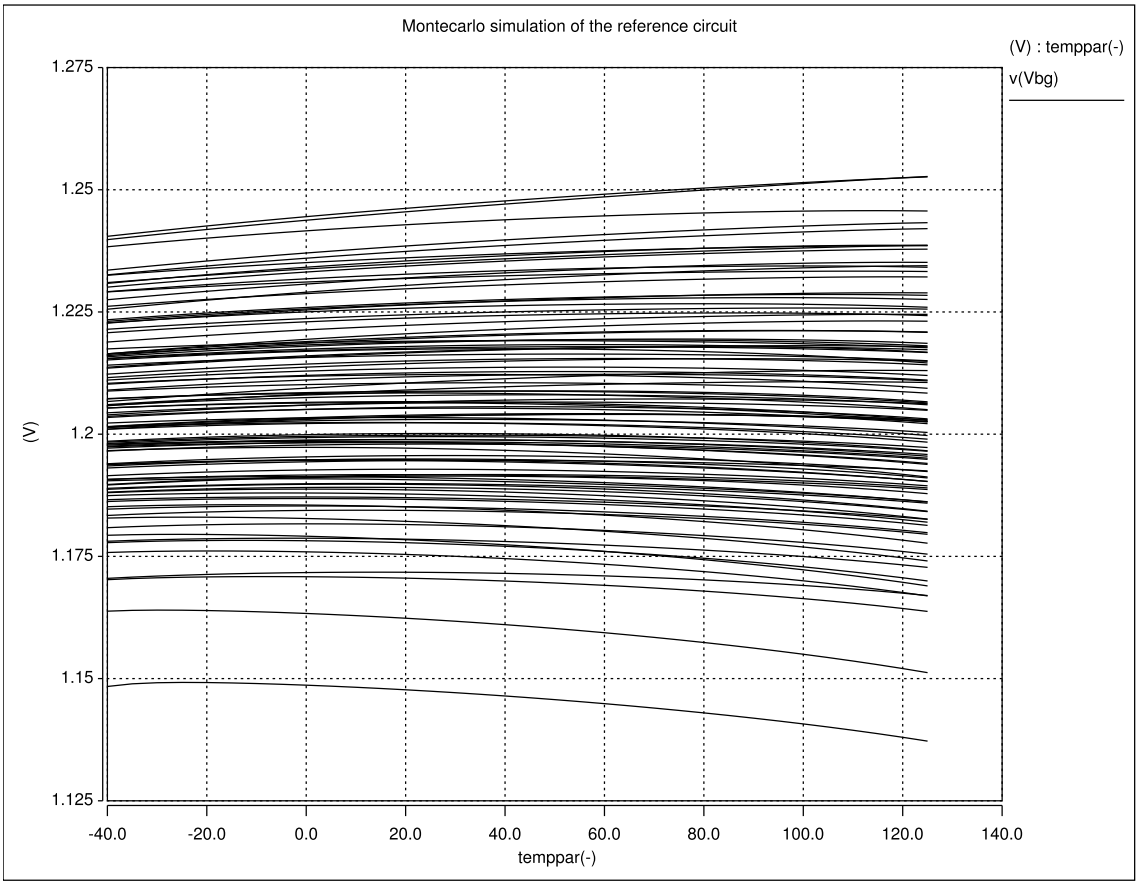


Figure 5.13: Temperature sweep of the reference voltage using Monte Carlo simulation.

5.7 BGR final datasheet values

A summary of the achieved specifications for the proposed bandgap voltage reference is presented in Table 5.2.

Table 5.2: Specifications of the proposed Bandgap Voltage Reference.

Parameter	Conditions	MIN	TYP	MAX	Unit
Input voltage range, V_{in}	-	1.7	-	3.6	V
Operating Junction Temperature	Designed for electro migration at $110°C$	-40	50	125	$°C$
Bandgap Voltage, V_{ref}	-	1.1962	1.208	1.2246	V
Bandgap Voltage Accuracy	-	-4	-	$+4$	%
Output current	-	-	10	-	μA
Bandgap Trimming	-	-	15.3	-	mV
Start-up time	$enable =' 1'$; to reach V_{ref}	20.2	32.2	56.6	μs
Temperature Coefficient	Over temperature range	-	3	64	$ppm/°C$
Total capacitance	no external capacitors	-	27	-	pF
Quiescent Current	Steady-state	3.6	4.9	7.8	μA
	Power-down mode	-	< 100	-	nA
PSRR	$@1kHz$	-112	-110	-76	dB
	$@10MHz$	-65.6	-61.3	-59.9	dB
Core Area	-	-	0.04	-	mm^2

Note that the scope of the work was to design and implement a BGR circuit with restrict specifications in terms of power consumption and power supply rejection ratio, namely, $5\mu A$ of total current consumption, $-70dB@1kHz$ and $-40dB@10MHz$, respectively. The full primary specifications of the BGR can be found in Section 1.2 and once compared to the ones achieved, the proposed BGR is a low power consumption IP core, highly independent to dc fluctuations and ac ripples that may be coupled in the power supply line, where the final results are even better than the primary specifications.

6

Layout

Contents

6.1 Design Towards Matching

Mismatch that can be observed between the parameters of a group of equally designed devices is the result of several random processes which occur during every fabrication. This definition excludes batch-to-batch or wafer-to-wafer variations of the absolute value of parameters and unwanted offsets caused by electrical, lithographic or timing differences.

6.1.1 Matching of MOS Transistors

Threshold voltage (ΔV_T) and Current factor ($\Delta\beta$; where $\beta = \mu C_{OX} W/L$) differences are the dominant sources of mismatching between MOS transistors [17]. These random differences have a normal distribution with zero mean and their standard deviation depends on device area $W \cdot L$ and device spacing distance [18] [19]. For the propose of this thesis, only area effects are taken into consideration. Thus, the standard deviation ΔV_T and $\Delta\beta$ defined by two closely spaced identical transistors are given by equations (6.1) and (6.2), where A_{V_T} and A_β are process-related constants [20].

$$\sigma(\Delta V_T) = \frac{A_{V_T}}{\sqrt{W \cdot L}} \tag{6.1}$$

$$\sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{\sqrt{W \cdot L}} \tag{6.2}$$

The model valid for all regions of operation that describes the variance for the relative current difference of two identical transistors biased with the same gate-to-source voltage is defined by equation (6.3).

$$\sigma^2\left(\frac{\Delta I_{DS}}{I_{DS}}\right) = \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \left(\frac{g_m}{\beta}\right)^2 \sigma^2\left(\Delta V_T\right) \tag{6.3}$$

Therefore, for a transistor biased in strong inversion and in saturation, the g_m/I_{DS} can be approximated by $2/(V_{GS}V_T)$. Substituting equations (6.1) and (6.2) in equation (6.3), it results that the variance of the current difference is inversely proportional to the area of the transistor as expressed by equation (6.4).

$$\sigma^2\left(\frac{\Delta I_{DS}}{I_{DS}}\right) = \frac{1}{WL}\left[A_\beta^2 + \frac{4 \cdot A_{V_T}^2}{\left(V_{GS} - V_T\right)^2}\right]. \tag{6.4}$$

However, if the corner gate-overdrive voltage is defined as $(V_{GS}V_T)_i = 2 \cdot A_{V_T}/A_\beta$, and considering that in most practical circuits $(V_{GS}V_T)$ is much smaller than $(V_{GS}V_T)_i$, the effect of V_T mismatch is dominant over β mismatch. As a result, equation (6.4) written as a function of standard deviation can be approximated by equation (6.5).

$$\sigma\left(\frac{\Delta I_{DS}}{I_{DS}}\right) \approx \frac{1}{\sqrt{WL}}\left[\frac{2 \cdot A_{V_T}}{\left(V_{GS} - V_T\right)}\right]. \tag{6.5}$$

The minimal transistor dimensions that imply a minimum transistor difference error can be expressed from equation (6.5), and they are dependent on the technology and on the bias point of the transistors. The rearranged expression is given by equation (6.6).

$$\sqrt{WL} \approx \frac{2 \cdot A_{V_T}}{\sigma\left(\frac{\Delta I_{DS}}{I_{DS}}\right) \cdot (V_{GS} - V_T)} \tag{6.6}$$

Assuming the mismatch parameters of Table 6.1 and from equation (6.5), the area of the current sources in Figure 4.2 (M_{13}, M_8, M_3 and M_9) can be used to evaluate the current standard deviation as in equation (6.7). The overdrive voltage of the transistors is $150mV$ which is the expected value according to simulations.

$$\sigma\left(\frac{\Delta I_{DS}}{I_{DS}}\right) \approx \frac{1}{\sqrt{2.5 \cdot 2 \cdot 14}} \frac{2 \times 5.9}{0.150} = 9.4\% \tag{6.7}$$

Hence, the standard deviation leads to a Yield of 90.6% which is, in fact, higher than the usual value of 1% assumed in these contexts. The improvement of this result to a standard deviation of 1% implies that the area of the transistors must be $(78.7 \times 78.7)\mu m^2$, resulting in a huge area cost. In view of that, the transistors are designed to have large channel-length, comparing to the minimum accepted by the technology, to increase area and also the overdrive voltage. The overdrive voltage is important because the better the transistors are in saturation region (and with equal drain-to-source voltages), the better the current mirror is achieved.

Table 6.1: Mismatch parameters.

Transistor	A_{V_T} $[\% \cdot \mu m \cdot V]$
PMOS	5.9
NMOS	6.4

Using equation (6.1) and assuming a confidence interval of 99.73% - which corresponds to three standard deviations - the threshold voltage can be also evaluated as in equation (6.8).

$$3\sigma(\Delta V_T) = \frac{3 \times 5.9}{\sqrt{2.5 \cdot 5 \cdot 14}} = 2.2\% \tag{6.8}$$

The $3-sigma$ mismatch produced by the threshold voltage of the transistors is not uncommon, although, since it has non-linear temperature dependence [21], the offset voltage also varies non-linearly with temperature; thereby the compensation process, even using trimming, can be difficult. The same methodology could be applied to the NMOS transistors resulting in the same qualitative results.

6.1.2 Resistor Mismatch

Based on Pelgrom model [20], the resistors can be viewed as two rectangular devices dependent on the area and their standard deviation can be expressed as in equation (6.9).

$$\sigma_R \left(\frac{\Delta R}{R} \right) = \frac{K_R}{\sqrt{W \cdot L}} \tag{6.9}$$

The area of each resistor is obtained by defining the variance of the resistor and using the value of the process-related parameter for the resistor type used in the layout. The resistors shall be made of the most highly resistive layer that the foundry supports.

When very accurate resistor ratios are required and the ratio can be expressed as a ratio of integer values, then an architecture similar to that shown in Figure 6.1 must be used [1].

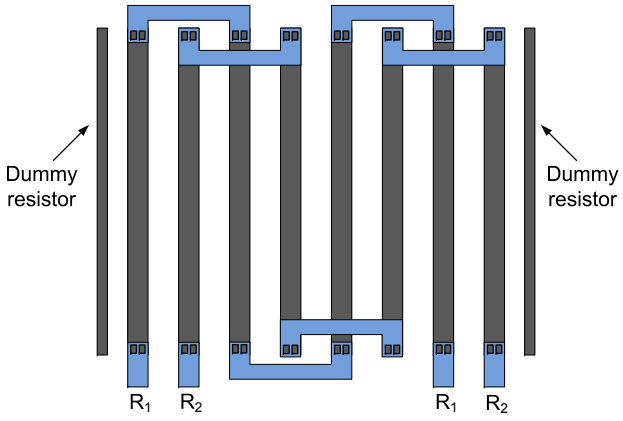


Figure 6.1: Accurate layout for a resistor.

Each resistor consists of several fingers connected in series using low-resistive metal. This approach matches errors caused by the contact impedance between R_1 and R_2 resistors. Also, two dummy fingers have been included to match boundary conditions. This structure might result in about 0.1% matching accuracy of identical resistors if the finger widths are relatively wide (say, $10\mu m$ in a $0.8\mu m$ technology). For low-noise proposes, it is a good idea to place a metal shield over the top of each resistor, although it results in a corresponding increase in capacitance. These techniques were used in the layout of the bandgap core's resistors. The resistors of the pre-regulator and master bias cell are isolated from the bandgap core ones to facilitate trimming. They create a pattern of four groups of each resistor, alternately placed, which results in higher immunity to temperature gradients. The conceptual diagram is presented in Figure 6.2.

6.2 Implementation

The transistors used in current mirrors are previously designed with an even number of fingers so that the matching is more effective.

The resistors used in the layout are all designed using highly resistive poly-resistors that can be implemented in an acceptable area and present a relatively high precision. The typical value for the resistor mismatch is about $\pm 1\%$. All the capacitors are designed using MOScap because

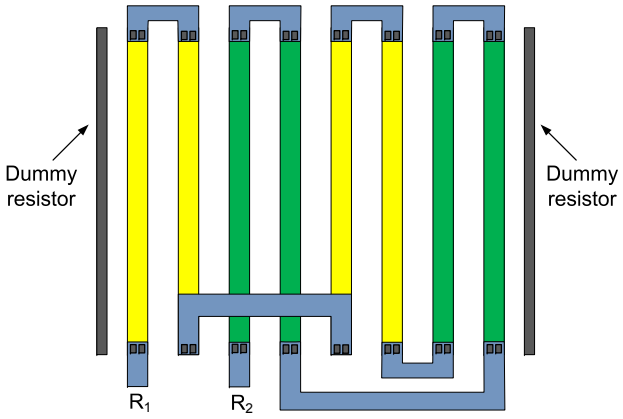


Figure 6.2: Layout for the pre-regulator and master bias cell resistors using only 2 groups of each resistor.

linearity is not a concern in the project. The transistors used in the design of the BGR are all high voltage because low voltage transistors can only stand a maximum drain-source voltage of $1.2V$. The exception is the capacitor M_3 in the pre-regulator block (Figure 2.17) because the reference voltage is always equal or below $1.2V$.

The active area of the bipolars is $A_1 = 8A_2$, not only to create the differential emitter-base voltage, but also to ensure a good matching between the transistors. Figure 6.3 shows the layout structure of the bipolars.

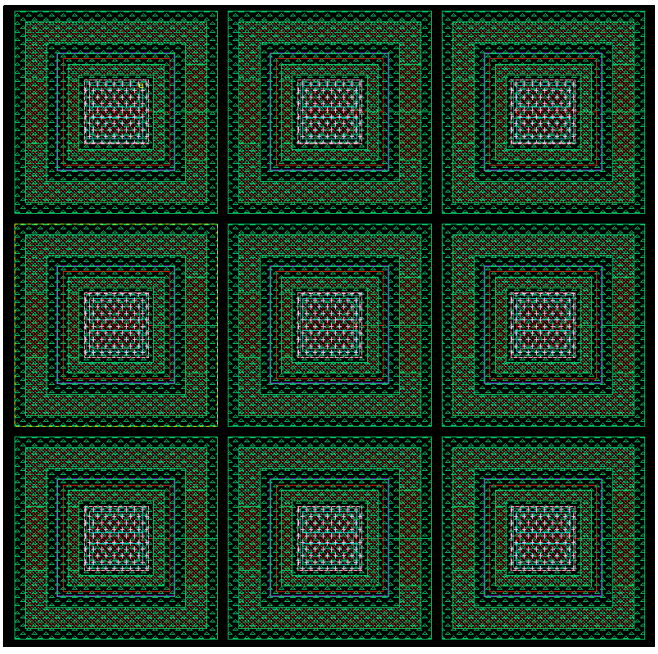


Figure 6.3: Accurate layout structure for the bipolars that reduce mismatching and relative temperature dependence.

The bipolar in the middle of the structure is Q_1 and the rest 8 bipolars are Q_2. Any temperature gradient always affects the bipolar transistors in the same manner, so the relative temperature immunity of the bipolars is much higher (common centroid design).

Figure 6.4 shows the top layout of the proposed bandgap reference circuit. The total area occupied is $0.04mm^2$ which is within the primary specifications.

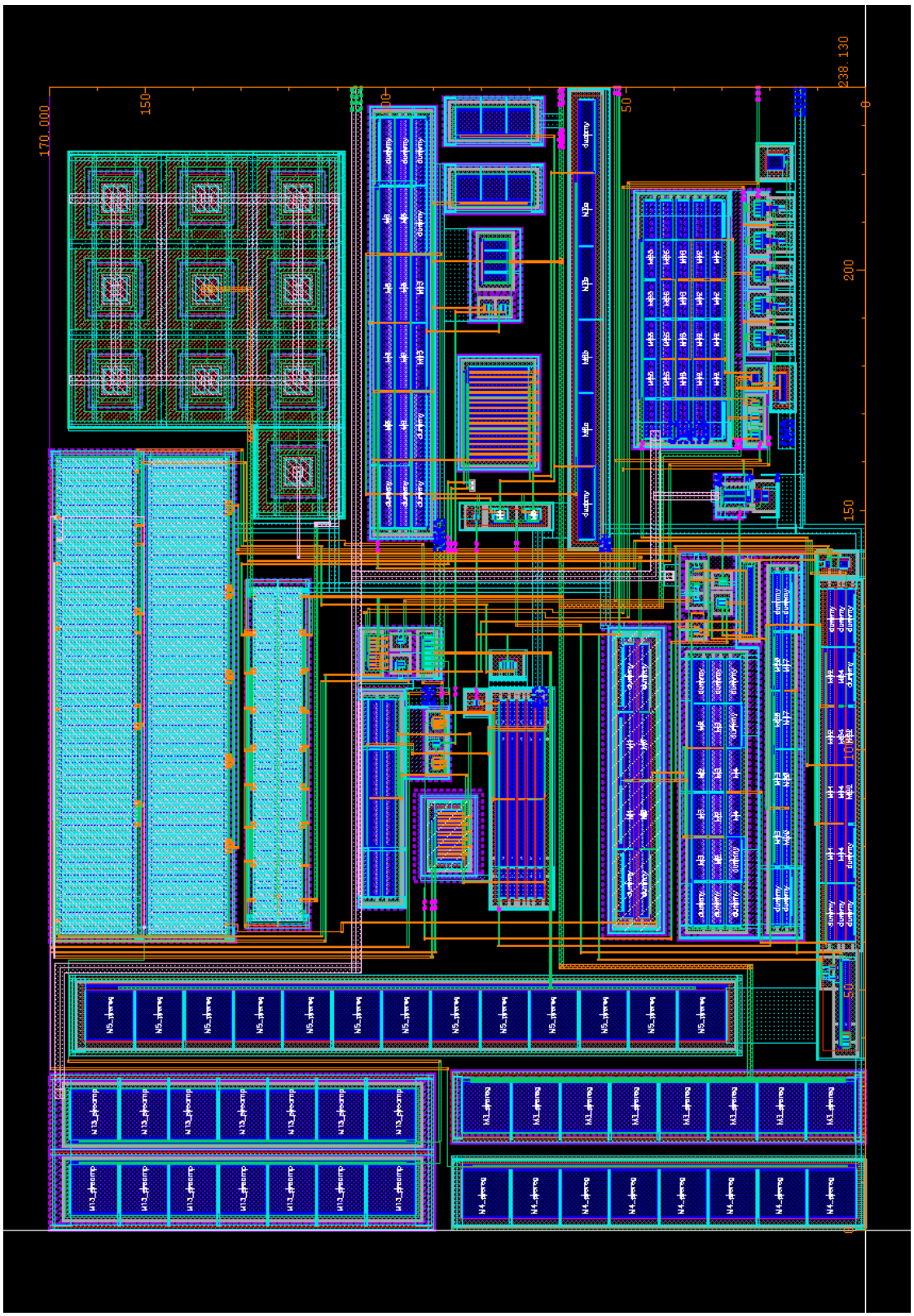


Figure 6.4: Top layout of the proposed bandgap voltage reference.

7

Conclusions

Contents

Within the scope of this thesis, a bandgap voltage reference circuit was designed and implemented. The primary specifications imposed were not achievable using a typical bandgap design, namely, it is not possible to achieve the required level of noise immunity, low power consumption and dc accuracy. Thus, a research among the PSRR State-of-the-Art techniques allowed defining the strategy to improve the overall PSRR of the reference circuit. The proposed architecture includes a pre-regulator in the supply voltage which increases the PSRR performance by $67dB$ at low frequencies. The bandwidth of the error amplifier used in the pre-regulator critically influences the PSRR performance and, above the gain-bandwidth frequency, the error amplifier no longer attenuates the noisy fluctuations in the supply power. Hence, $27pF$ of on-chip capacitors ensure that the PSRR is within the specifications. This approach allows the proposed bandgap voltage reference to present $-110dB@1kHz$ and $-61.3dB@10MHz$, which is high above the primary specifications ($-70dB$ and $-40dB$, respectively).

Power consumption is also a major concern in the BGR design and low power is achieved by using transistors that are used as switches, carefully placed in series with auxiliary branches. Particularly, the reference applied to the pre-regulator during the start-up of the bandgap is made by a resistive divider referenced to the supply voltage; hence it is responsible for most of the total current consumption in this period. The start-up circuit of the current source also represents a bottleneck in the total current consumption, and thereby, it is disabled as soon as the bandgap voltage reaches around 70% of its final value. At this time, the reference of the pre-regulator is switched to the bandgap voltage, making the output bandgap voltage highly independent from the main supply, since the supply voltage of the bandgap core is the output of the pre-regulator. The BGR is a low power consumption IP core with $4.9\mu A$ of total current consumption.

Moreover, the proposed bandgap has the advantages of presenting low temperature dependence and $10\mu A$ of driving current capability without requiring an output buffer (which would increase the area). The temperature curvature of the bandgap voltage has to be trimmed at the time the IP core is being tested, so that the deviation between the full temperature range reaches the minimum value of $3ppm/°C$. The occupied area of the proposed bandgap voltage was a primary specification, so the design always took into consideration the area-consumption trade-off; thus it was possible to reach $0.04mm^2$.

Finally, foundry recommendations for the layout design of the proposed BGR were taken into account, especially regarding matching of resistors, mosfet and bipolar transistors. The BGR was designed and implemented in $TSMC$® 65 nm CMOS technology at Chipidea®.

7.1 Future Work

The proposed bandgap reference circuit represents an improvement on the primary specifications, although there is always margin for additional improvements. The inclusion of the bandgap

circuit in a modern sub-micron Power Management Unit may raise concerns of start-up timing, higher PSRR levels, better performance in power dissipation both in *on* and *off* mode and temperature curvature. However, improvements in these characteristics commonly have an associated area cost.

Likewise, the master bias cell presents a maximum reference current deviation of $+92\%$ from typical and, eventually, the next analog blocks (a low dropout regulator, for instance) require about $\pm 5\%$ to ensure stability within different operation modes and current loads. A possible design to solve this matter is to generate the reference current based on the bandgap voltage, making the current deviation only imposed by the value of the resistor. Meanwhile, the resistor can be designed to guarantee trimming; thereby allowing the adjustment of the reference current during the test of the IP core. The disadvantages of this structure are that an output buffer is needed; more current consumption is inserted into the system and the area of the bandgap circuit increases.

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A

Testbenches

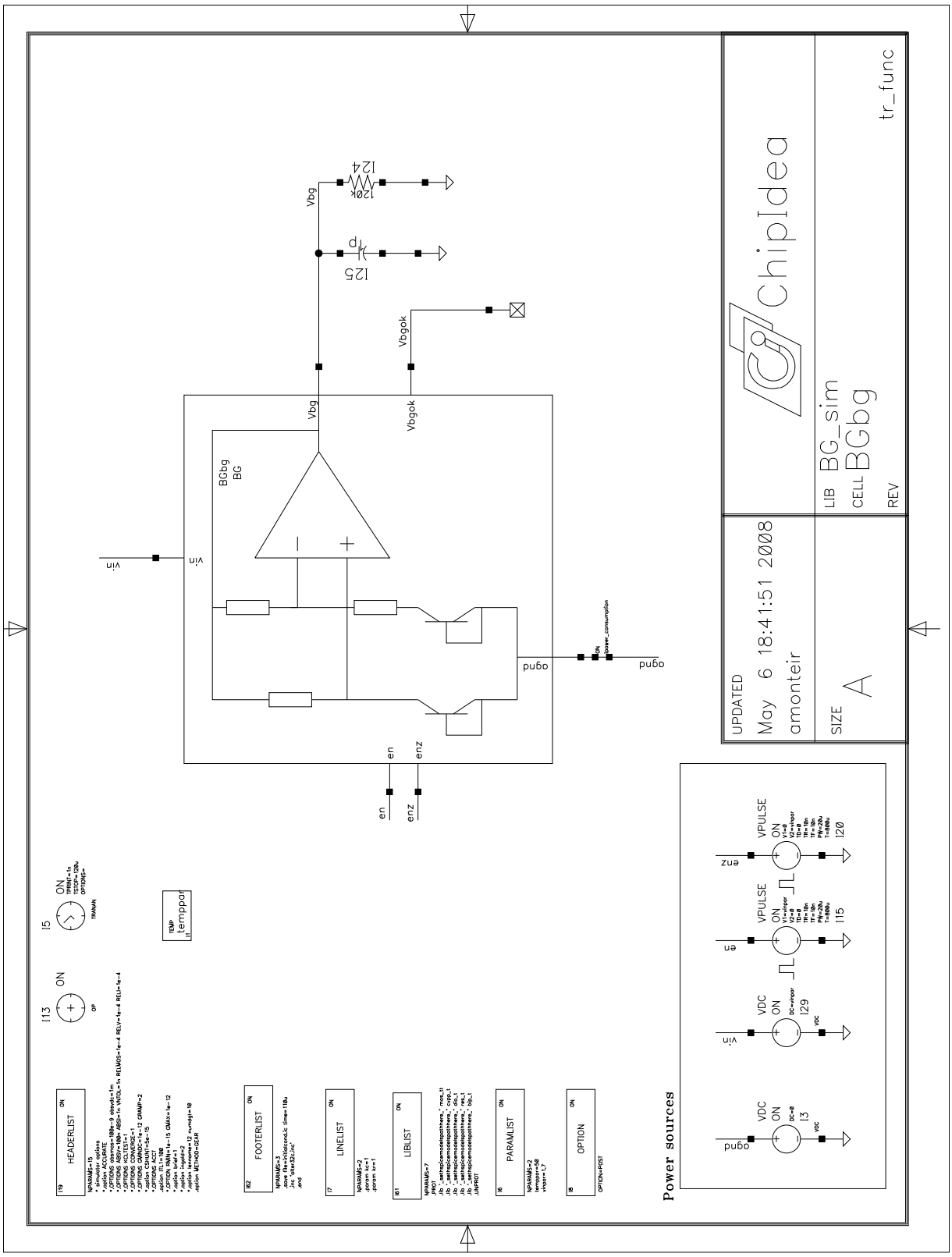

Figure A.1: Testbench used in the transient response of the BGR.

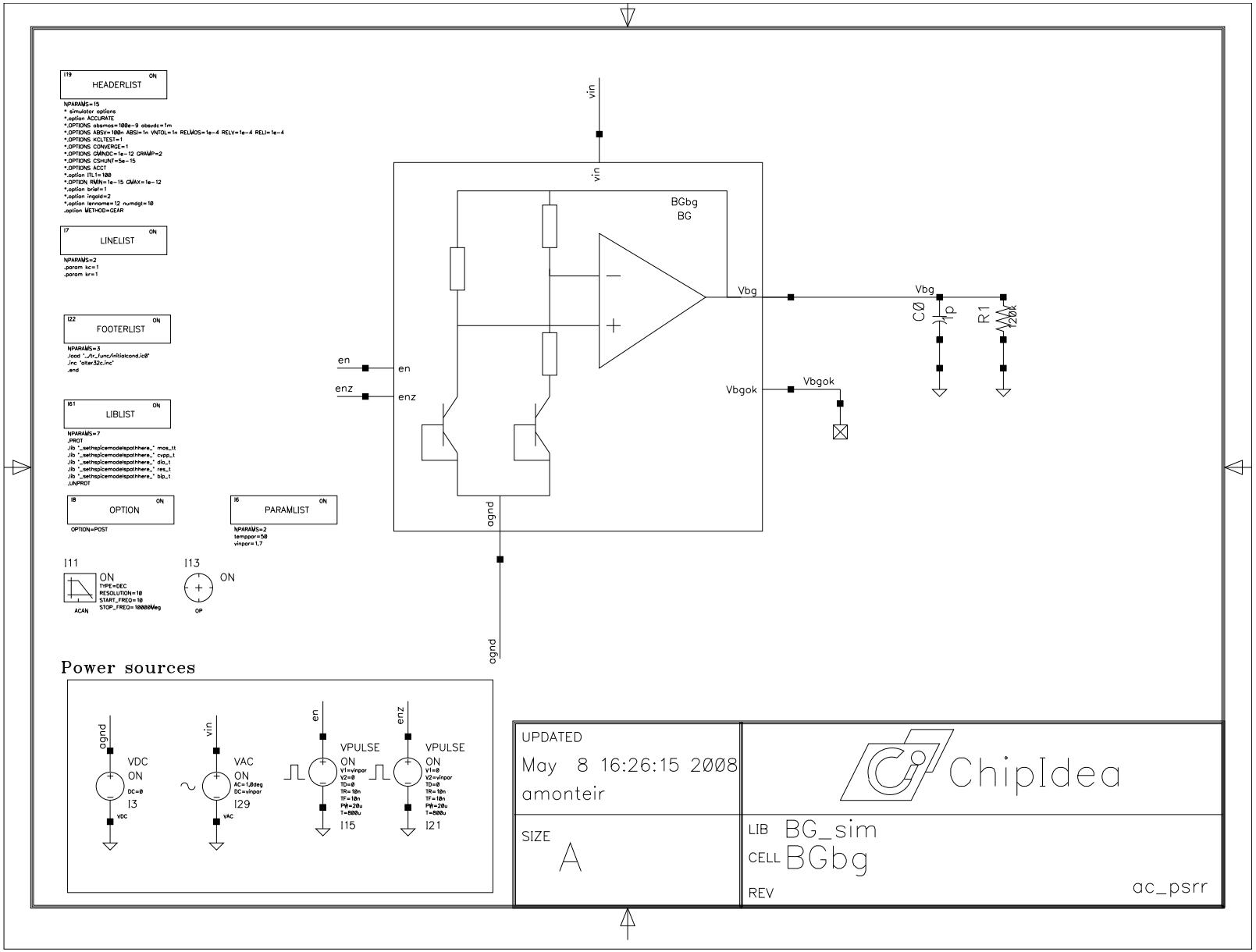

Figure A.2: Testbench used to evaluate the psrr performance of the BGR.

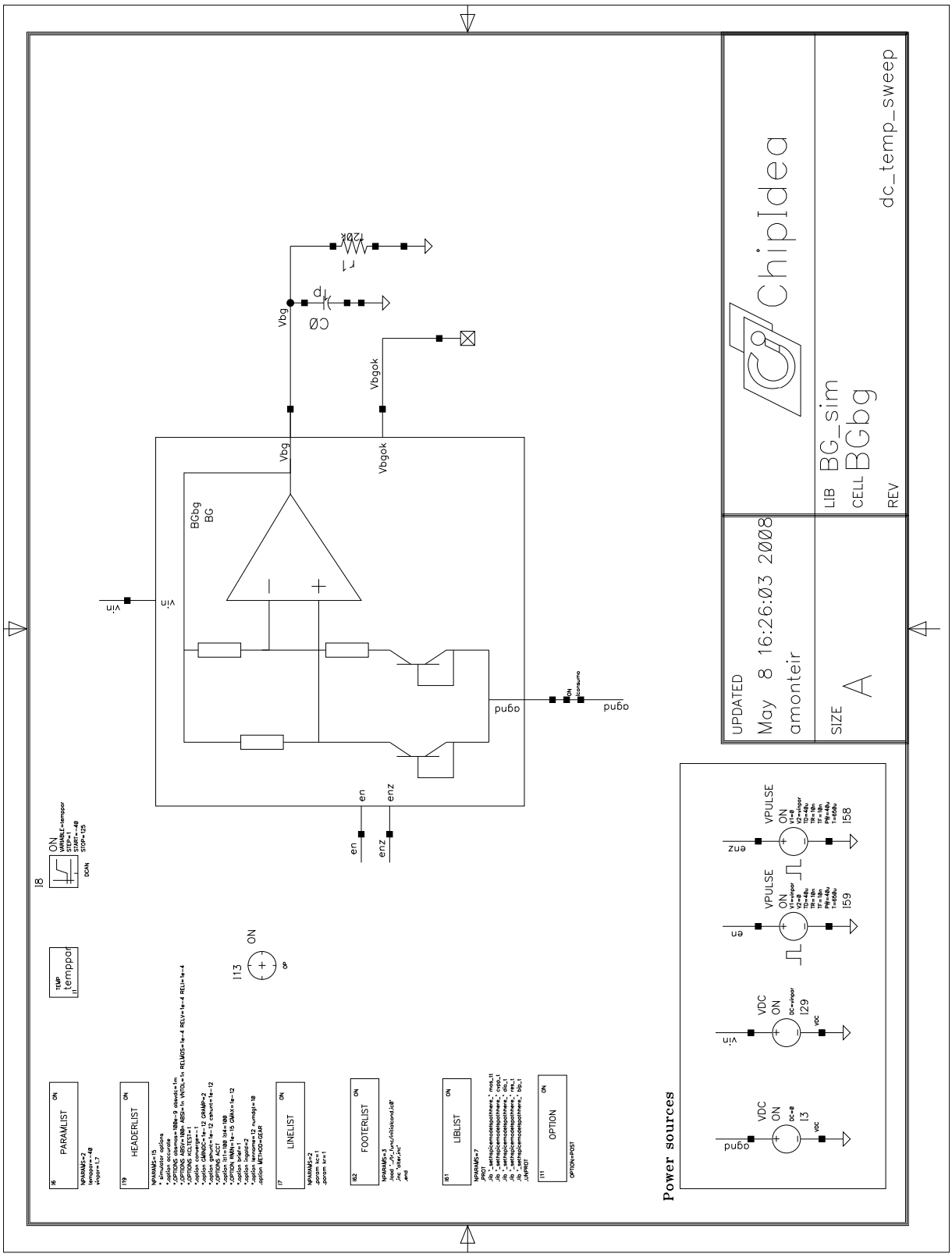

Figure A.3: Testbench used to evaluate the temperature curvature of the BGR.

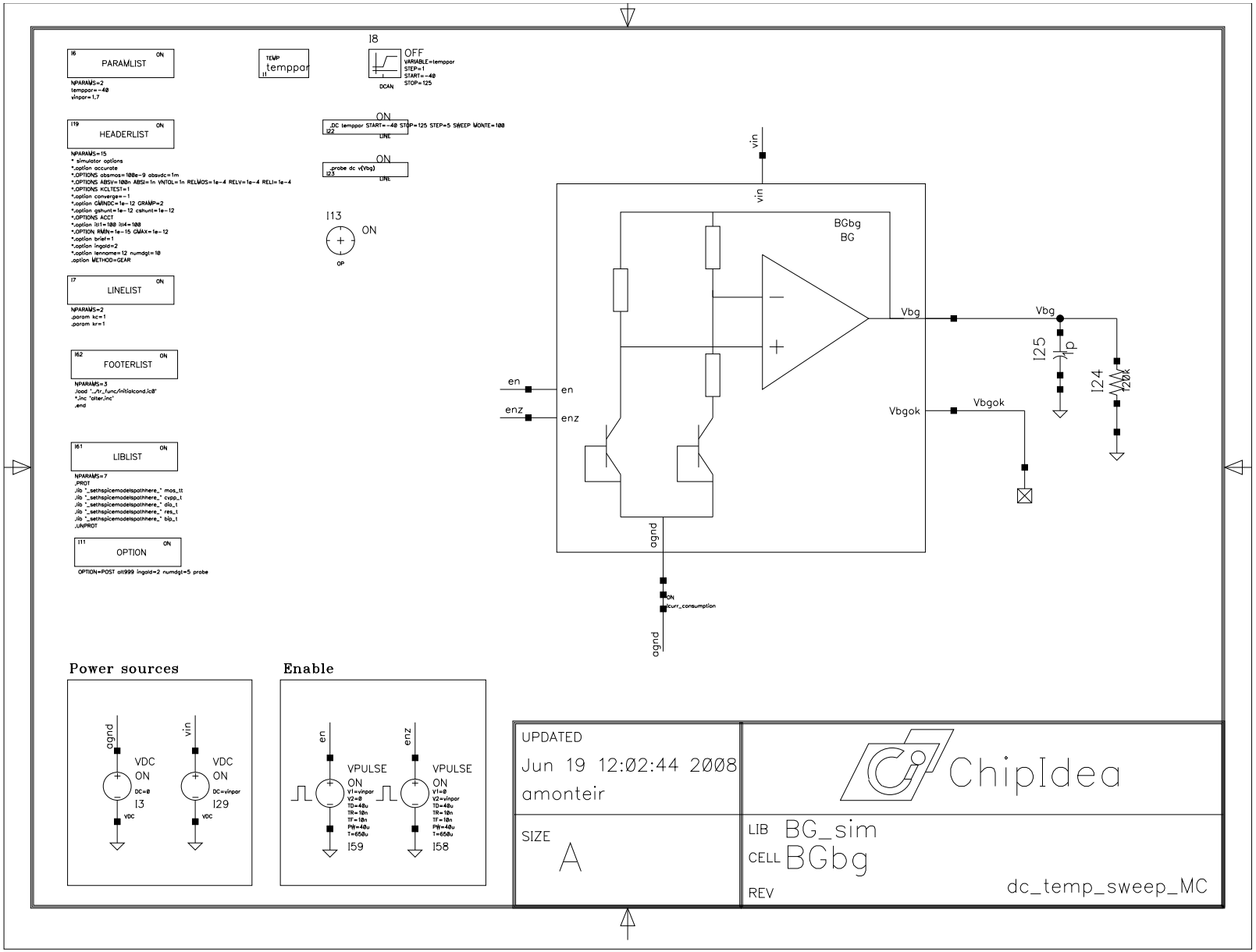

Figure A.4: Testbench used to evaluate the temperature curvature of the BGR using Montecarlo run.

B

Schematics

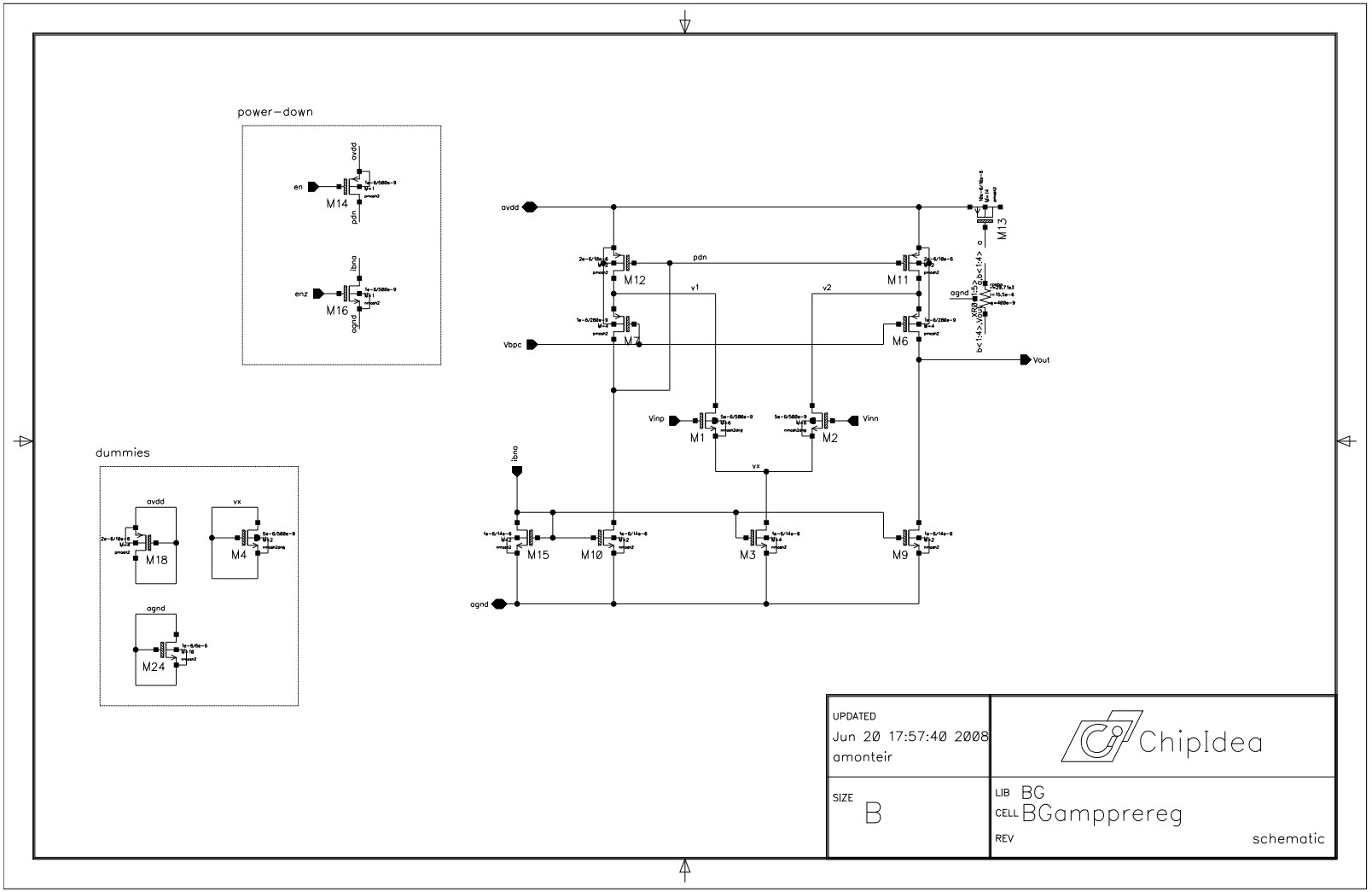

Figure B.1: Schematic of the pre-regulator's error amplifier.

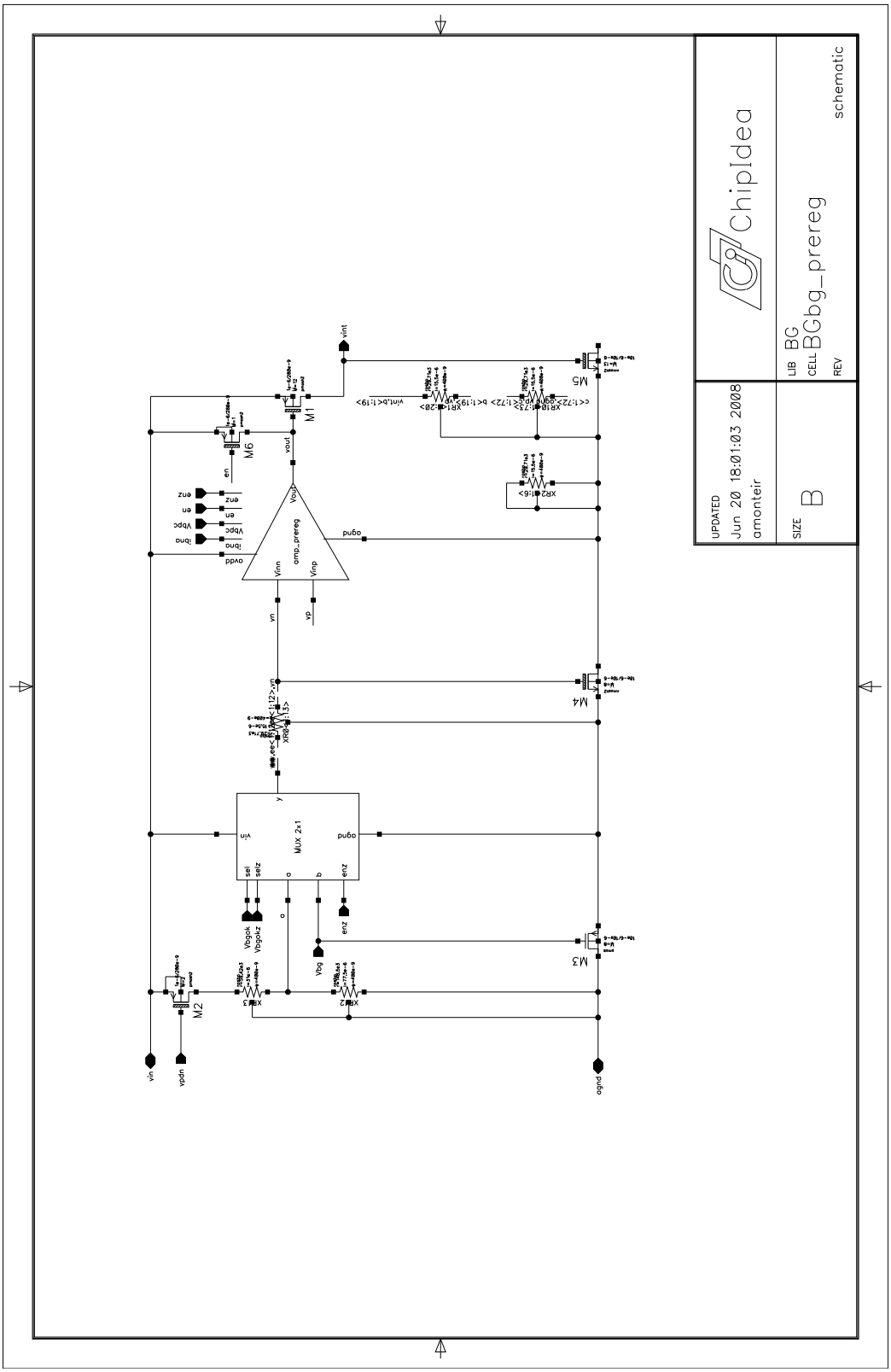

Figure B.2: Schematic of the pre-regulator.

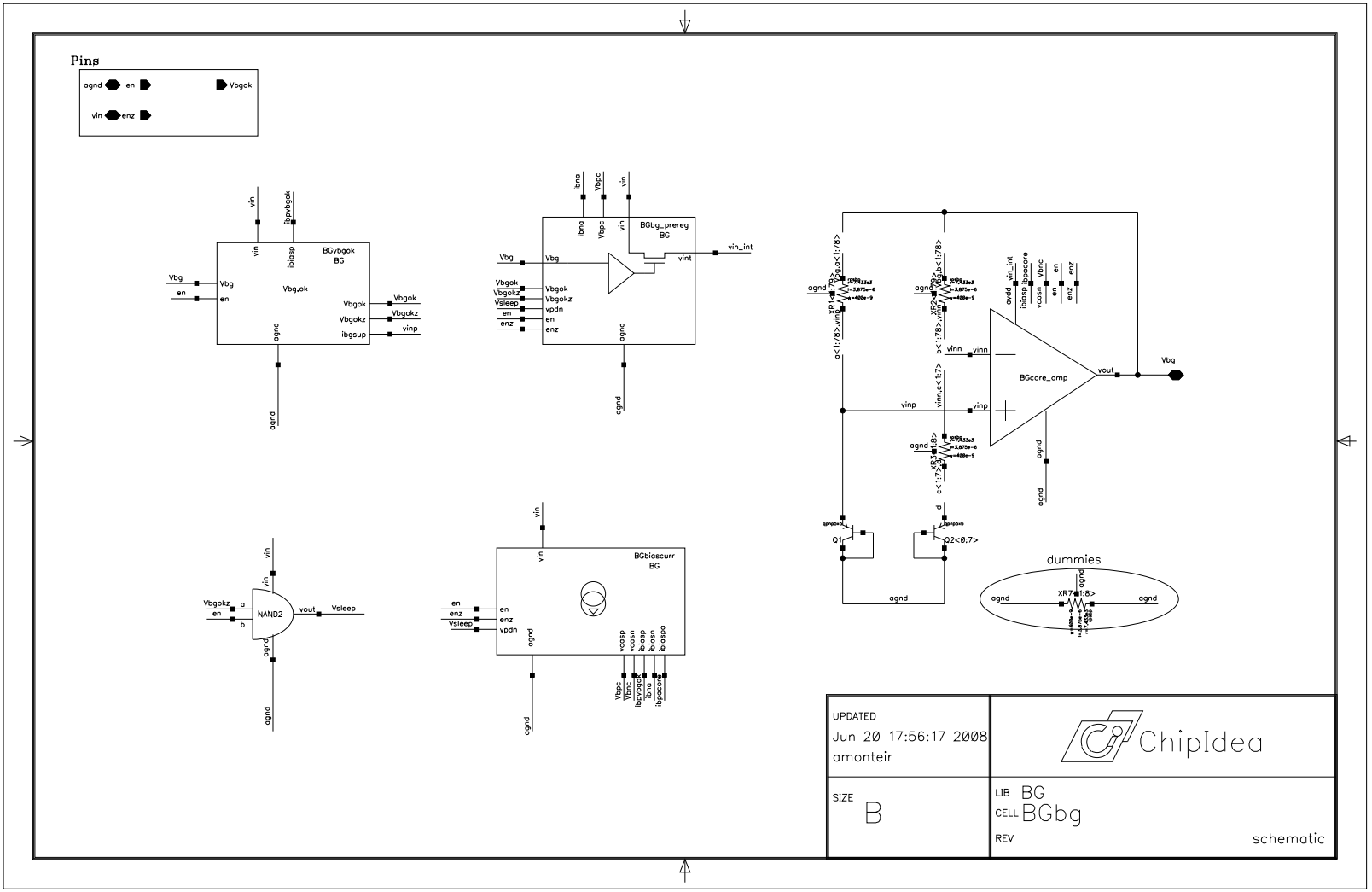

Figure B.3: Schematic of the BGR circuit.

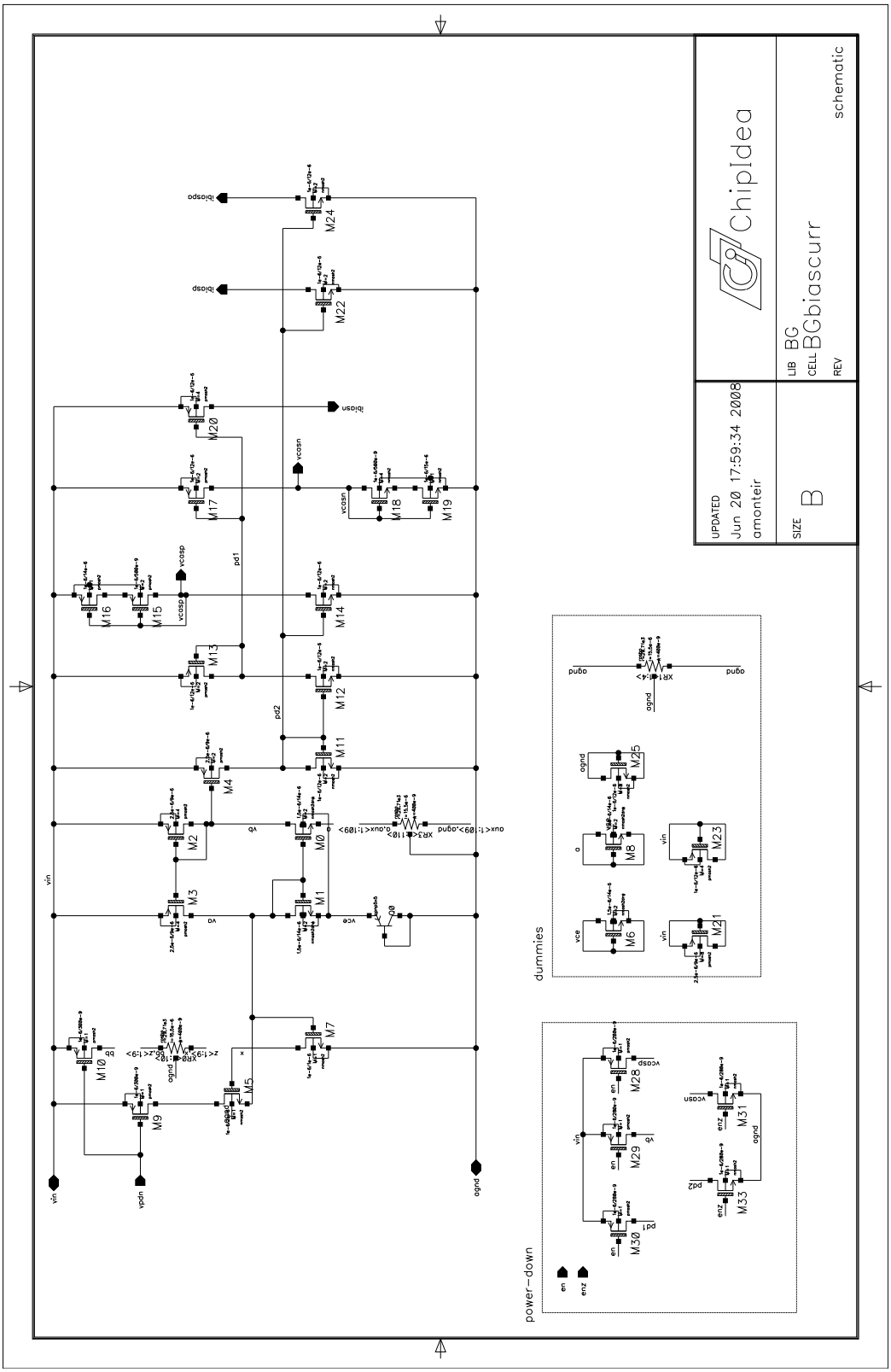

Figure B.4: Schematic of the master bias cell.

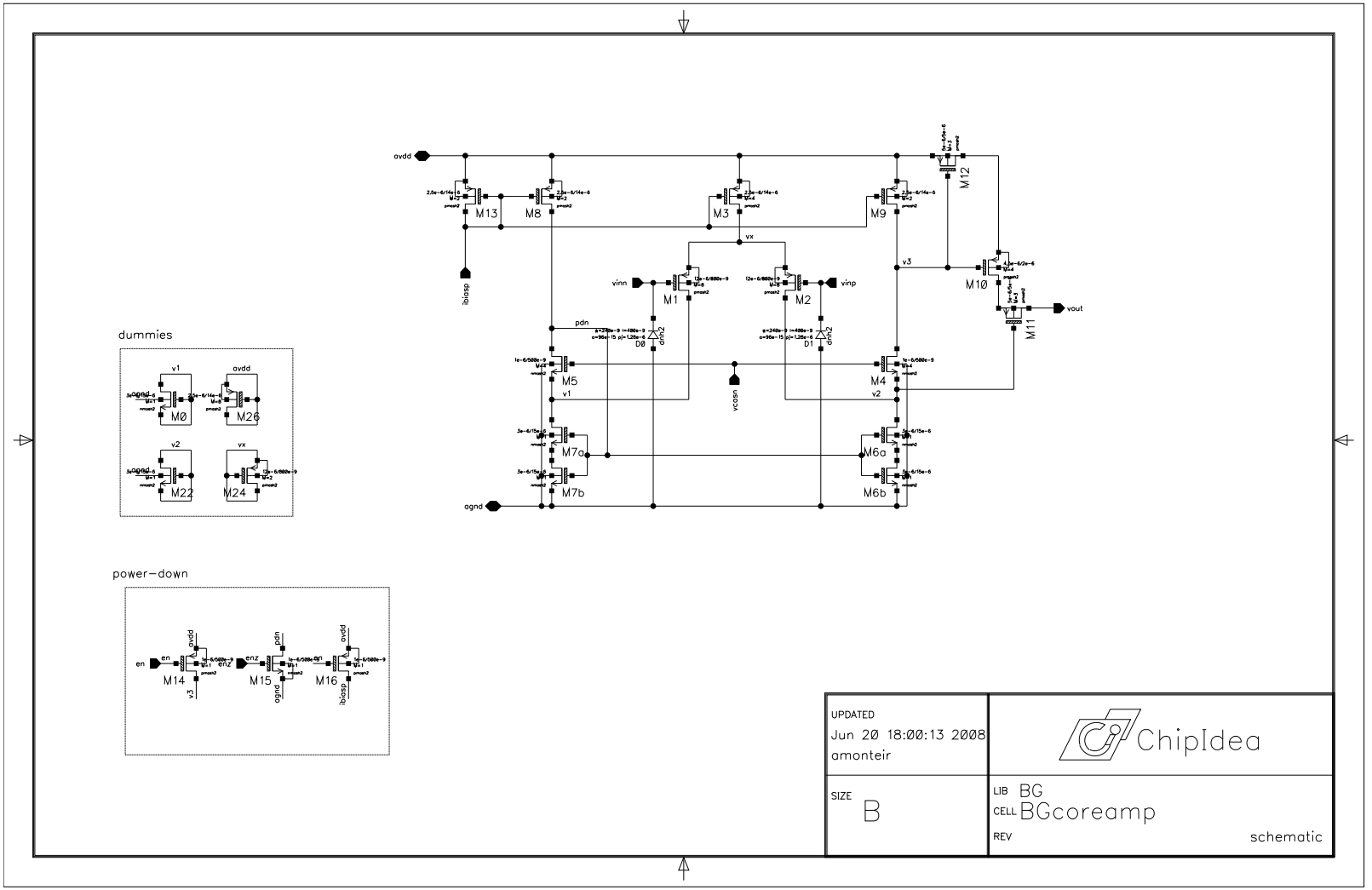

Figure B.5: Schematic of the BGR core's error amplifier.

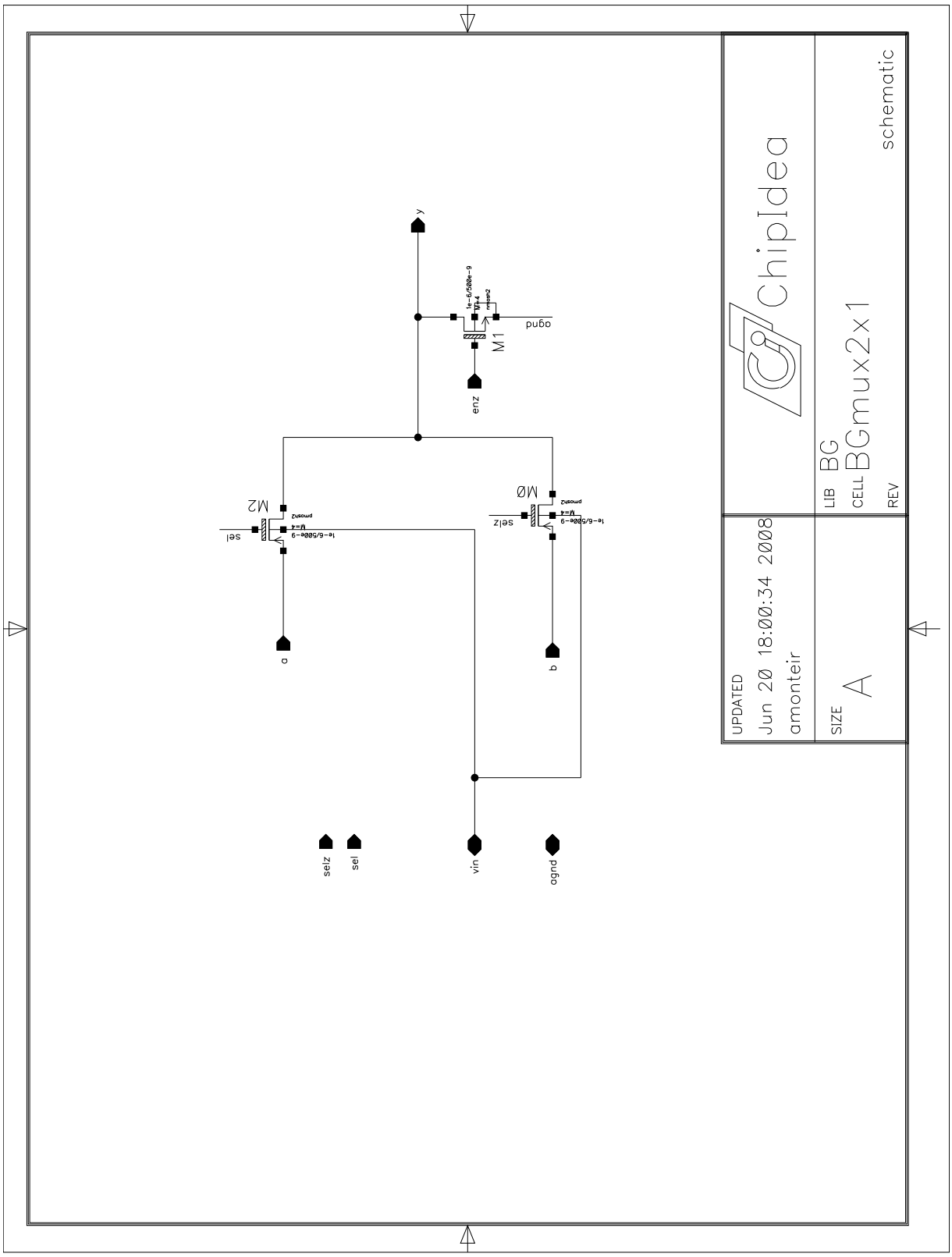

Figure B.6: Schematic of the multiplexer.

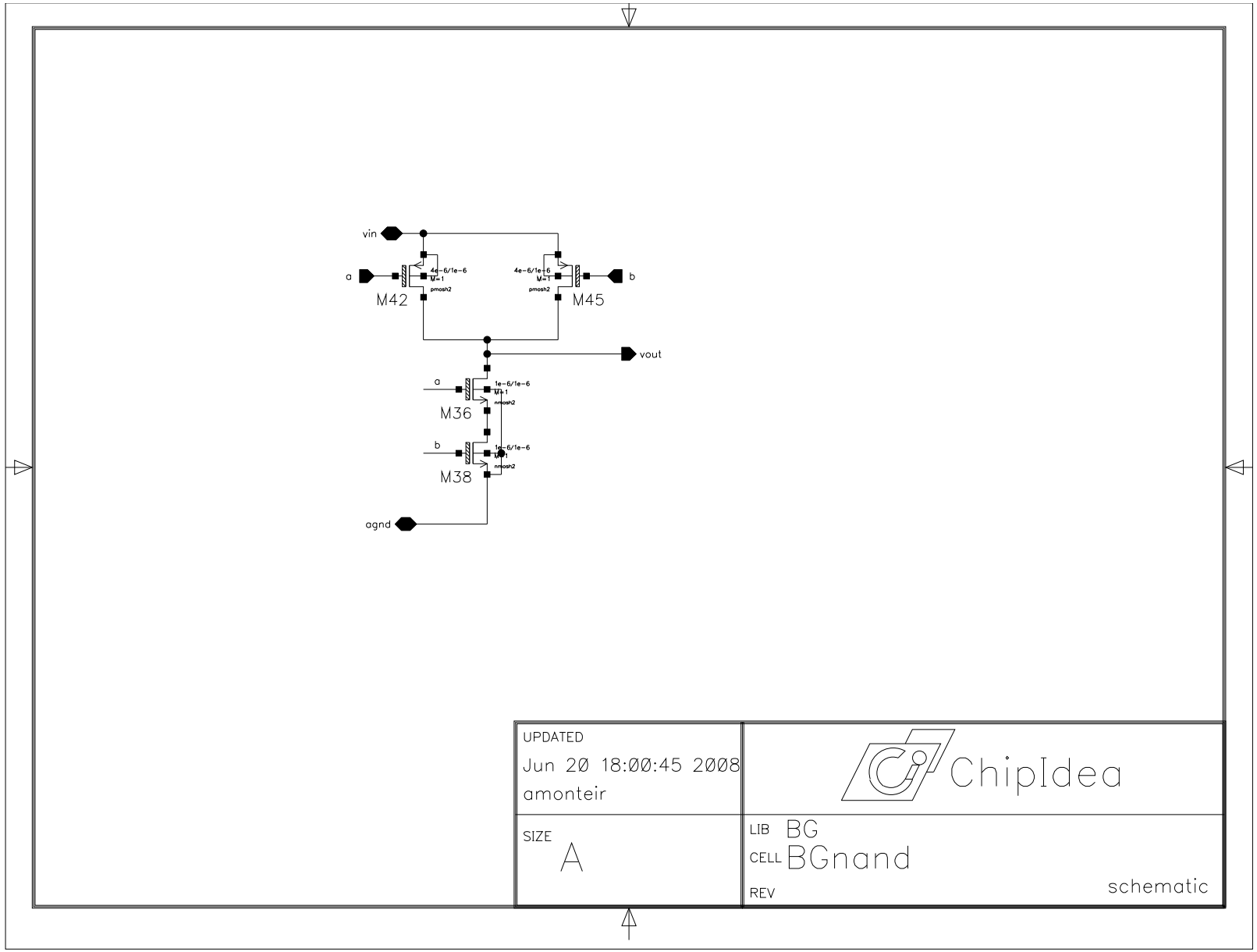

Figure B.7: Schematic of the nand.

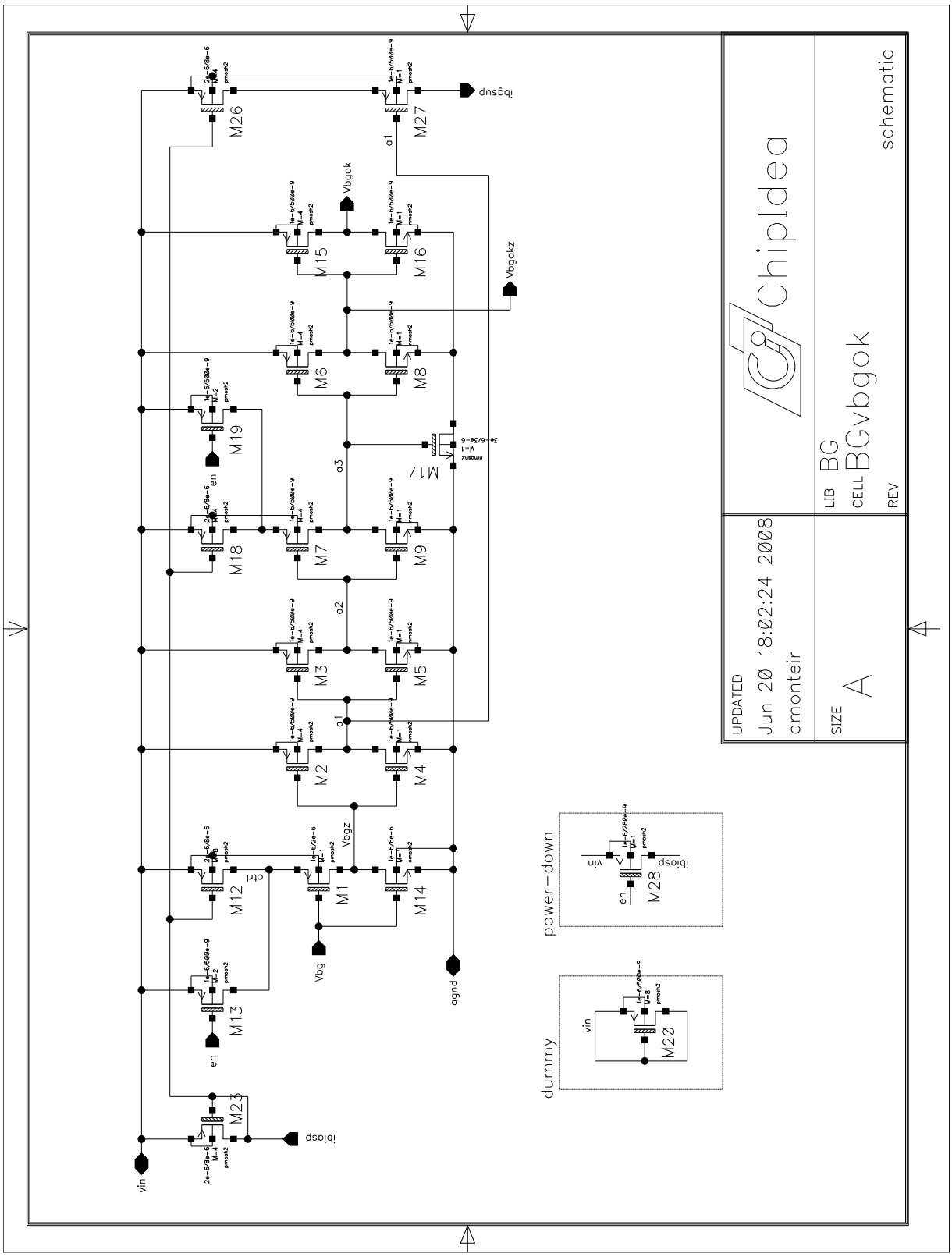

Figure B.8: Schematic of the validation block - vbgok.