UNIVERSIDADE DE LISBOA

INSTITUTO SUPERIOR TÉCNICO

A MATRIX CONVERTER BASED SOLID STATE TRANSFORMER FOR FUTURE ELECTRICAL GRIDS

Pedro Miguel Batista de Sousa Correia da Costa

Supervisor: Prof. Sónia Maria Nunes dos Santos Paulo Ferreira Pinto
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Thesis approved in public session to obtain the PhD Degree in

Electrical and Computer Engineering

Jury final classification: Pass with Distinction

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Abstract

The imminent threats of global warming demand new paradigms across various sectors. Among them are the electrical, industrial and transportation sectors. Decarbonising these sectors demands high penetration of renewable energies in the grid and a massive reduction of fossil fuels. These changes demand new concepts, such as Smart Grids, to tackle challenges in the stability and operation of these future industrial/residential grids, as well as microgrids in aeroplanes and large vessels.

Solid State Transformers are a key technology for future grids. Reeling in power electronic converters can increase controllability (paramount for grids with high decentralised renewable energy penetration), increase power density (extremely relevant in large vessels and aeroplanes) and increase overall net efficiency. Among different power converter topologies, matrix converters can perform AC/AC conversion without any intermediate energy storage and consequently benefit from higher power density and increased converter lifetime.

This work proposes a matrix converter-based SST tackling the technical challenges that arise from the use of matrix converters at the front and back end of SSTs. A novel topology is proposed, and a suitable modulation method is designed to minimise the transformer flux while allowing for the SST to be controlled as a traditional matrix converter, enabling the use of well-established control methods. The leakage of the medium/high-frequency transformer in SST demands new commutation methods for the front-end matrix converter; in this work, a leakage-tolerant commutation method was formulated for a generic number of input and output phases with multiphase transformers. An optimization-based method to size high-order grid-connected filters was designed to further increase the SST power density, and a model predictive controller was designed to control the converter currents.

Simulations of the proposed topology and controllers show prominent results that validate the design methodology.

Keywords: Power Electronics; Solid State Transformers; Matrix Converters; High Power Density Converters; Power Converter Control.

Resumo

Para mitigar os efeitos adversos do aquecimento global é necessária uma descarbonização em massa dos mais relevantes sectores da sociedade. Para tal é necessário aumentar a injeção de energias renováveis na rede assim como um abandono significativo da utilização de combustíveis fosseis. Estas necessidades catalisam novos conceitos como o *Smart Grids* que visam enfrentar os desafios de futuras redes industriais e residenciais assim como micro redes em aeronaves e navios.

Considerada uma tecnologia fundamental nesta transição os Transformadores de Estado Sólido (SST) fazem uso de conversores eletrónicos de potência permitindo operar os transformadores em elevadas frequências. Consequentemente permitem maior flexibilidade de controlo (essencial em redes elétricas com alta penetração de energias renováveis), maior densidade de potência (relevante para a penetração desta tecnologias no sector dos transportes) assim como um aumento da eficiência global das redes. De entre as diferentes topologias de conversores eletrónicos de potência, os conversores matriciais permitem a conversão direta AC/AC sem armazenamento intermédio de energia, beneficiando de maiores densidades de potência e um aumento no tempo médio de vida do conversor.

Este trabalho propõe uma nova topologia para um SST baseada em conversores matriciais para a qual é desenhado um método de modelação que não só permite a minimização do fluxo mas também permite controlar o SST como um conversor matricial clássico permitindo assim a utilização de técnicas de controlo destes conversores bem conhecidas. É ainda proposto um método de modelação capaz de comutar os conversores sob a presença do fluxo de fugas de transformadores com múltiplas fases. Com o objetivo de maximizar a densidade de potência é desenvolvido um método de dimensionamento para filtros de ligação à rede de elevada ordem. É também desenvolvido um mecanismo de controlo para o SST baseado controladores preditivos para as correntes e controladores não lineares para as tensões.

O funcionamento do SST é demonstrado em simulação com resultados que validam tanto a topologia como o seu controlo e mecanismo de comutação.

Palavras-Chave: Eletrónica de Potencia; Transformadores de Estado Sólido; Conversores Matriciais; Conversores de elevada densidade de potência; Controlo de conversores eletrónicos de potência.

Acknowledgements

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I would firstly like to extend my gratitude to my supervisor Prof. Sónia Pinto, whose work and knowledge in Matrix Converters fuelled my pursuit to develop high power density Solid State Transformers. I can only appreciate the availability, advise and support that translated in many hours devoted to this work.

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SYMBOL TABLE

Symbols

a_k	Filter denominator coefficients
A_e	Magnetic material core cross-section
A_p	Transformer area product
A_w	Core window area
b_k	Filter numerator coefficients
B_m	Transformer core's saturation flux density
$BFOM$	Baliga figure of merit
C_i	Capacitance of capacitor i
$\boldsymbol{c}$	Set of capacitors in the filter optimisation problem
$\mathbf{C}$	Concordia transform matrix
e_v	Errors between the reference voltages and output voltages
E_g	Semiconductor energy bandgap
f_s	Transformer operating frequency for the evaluation of the transformer power density
f_p	Function that calculates the set of state variables x at instant time instant t_{k+1} based on the state variables at instant t and the converter vector
f_{sw}	Switching frequency
g	General notation for a cost function or functional
g_f	Cost function of the flux minimisation SST modulation
g_{fn}	Normalised cost function of the flux minimisation SST modulation
g_g	Cost function for the STT model predictive controller
G_n	Filter gain response
H_n	Filter transfer function
h_w	Planar magnetic core window height
i_k	Current at line $k.d$
$\mathbf{i}_k$	Vector notation for a set of currents
J_{co}	Transformer cooper winding current density
k_b	Core staking factor
k_{cu}	Transformer winding filling factor
k_f	Waveform factor
K_v	Non-linear voltage controller gain

$\mathbf{K}$	Transition constrain matrix of the leakage tolerant commutation method
L_i	Inductance of inductor i
l_w	Planar magnetic core window width
$\boldsymbol{l}$	Set of inductors in the filter optimisation problem
m_{kj}	Modulation index of the switch connecting the output phase k to the input phase j
n_k	Number of turns of coil k
PF	Power factor
P_{cu}	Transformer winding joule effect power losses.
P_{fe}	Transformer core material losses
P_t	Total transformer losses
$\mathbf{D}$	$dq0$ transform matrix
Q_g	Grid reactive power
R_i	Resistance of resistor i
R_{ON-SP}	Specific on-state resistance
r_t	Transformer turns ratio
r_i	Parasitic resistance of inductor i
$\boldsymbol{r}$	Set of resistors in the filter optimisation problem
S_j	Transformer winding j apparent power
S_p	Primary winding transformer apparent power
S_{Si}	ith secondary winding transformer apparent power
S_k	With $k = \{1, .., n\}$, converter vector number k based on vector tables.
S_{kj}	State of the switch connecting the output phase k to the input phase j
S'_{kj}	State of the switch connecting the output phase k to the input phase j for the 3x4 DMC
t	Time in SI units unless stated so.
T_s	Discretisation time period
$\mathbf{T}$	State transition matrix of the leakage tolerant commutation method
v_{gi}	Line i to neutral input grid voltage
v_k	Voltage between node k and a reference neutral voltage
v_{kj}	Voltage between node k and node j
V_{BK}	Semiconductor breakdown voltage
$\mathbf{v}_k$	Vector notation for a set of voltages
V_t	Transformer volume

V_v	Lyapunov functions for the output voltage non-linear control
W	Energy stored in the filter for the filter optimisation problem
w_k	Weight factor for cost functions, $k = \{1,2, \dots n\}$
α	Material-dependent constant for magnetic losses
β	Material-dependent constant for magnetic losses
ε_s	Permittivity
ρ_w	Winding material resistivity
μ_n	Electron mobility
γ	Component value scaling factor for the filter sensitivity analysis
ω_n	Low pass filter cut-off frequency
ω_k	Angular frequency of the relevant voltage, current or flux k
ϕ_i	Input grid voltage and current displacement angle
ϕ_o	Output grid voltage and current displacement angle
ϕ_{fk}	Magnetic flux per turn at coil k
ϕ_{fik}	Magnetic flux per turn at coil k at the beginning of the integration period
χ	Equivalent converter matrix of the association of two series matrix converters
χ_{kj}	State of the equivalent SST switch connecting the output phase k to the input phase j
χ_k	With $k = \{1, .., n\}$, equivalent SST converter vector number k based on vector tables.

Additional subscripts and superscripts

d	Direct axis component in a $dq0$ reference frame
q	Quadrature axis component in a $dq0$ reference frame
0	Zero-axis component in a $dq0$ reference frame
α	Alpha component in an $\alpha\beta\gamma$ reference frame
β	Beta component in an $\alpha\beta\gamma$ reference frame
γ	Gamma component in an $\alpha\beta\gamma$ reference frame
k	Acquisition of the relevant unit at instant k, normally corresponding to the current time instant
$k-1$	Acquisition of the relevant unit at instant $k-1$
$k+1$	Acquisition of the relevant unit at instant $k+1$
$k+2$	Acquisition of the relevant unit at instant $k+2$
T	Denotes the transpose of the relevant matrix

$*$ Denotes a reference value for the relevant unit

ABBREVIATIONS

AC – Alternated Current

CO_2 – Carbon Dioxide

DC – Direct Current

ESD – Energy Storage Devices

EU – European Union

EV – Electric Vehicles

FACTS – Flexible AC Transmission Systems

FEM – Finite Elements Model

GaN – Gallium Nitride

PHEV – Plug-In Hybrid Electric Vehicles

HF – High Frequency

HMET – High Electron Mobility Transistor

HV – High Voltage

MF – Medium Frequency

IGBT – Insulated Gate Bipolar Transistor

IT – Information Technology

IV – Intermediate Vector

LF – Low Frequency

LV – Low Voltage

MOSFET – Metal Oxide Semiconductor Field Effect Transistor

MVDC - Medium Voltage Direct Current

PQ – Power Quality

PQI – Power Quality Indicators

RB-IGBT – Reverse Blocking IGBT

RER – Renewable Energy Resources

RMS – Root Mean Square

SG – Smart Grids

SiC – Silicon Carbide

SST – Solid State Transformer

THD – Total Harmonic Distortion

V2G – Vehicle to Grid

V2V – Vehicle to Vehicle

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Chapter 1

INTRODUCTION

This chapter presents the motivation and objectives that guided this work in the search for direct AC-AC conversion solid state transformers (SST), which will be shown to be a key technology for the future of the electrical distribution systems and the electrification of the transportation sector. Besides defining the objectives, this chapter introduces this work's original contributions and outline.

1.1 Motivation

Global reduction of carbon dioxide, CO_2, and emissions is currently viewed as the most effective mechanism to reduce the greenhouse effect. Sources of carbon emissions spread across multiple sectors where the combination of energy used in Industry (24.2%), Buildings (17.5%) and transportation (16.2%) account for around 58% of the more than 5.8 billion tons of CO_2 emitted yearly [1].

European Union (EU) outlined several climate strategies and targets with short-term, mid-term and long-term objectives and frameworks to reduce greenhouse effect gasses, increase overall energy efficiency and increase the share of renewable energy in the energy production mix [2–4]. As of July 2021, the EU Climate Law has been approved by the member states, and it envisions carbon neutrality by the year 2050, imposing intermediate targets in 2030 and 2040 [5].

Several paradigm changes must happen to fulfil the ambitious CO2 neutrality targets successfully. Among them are the transition to renewable energies and the electrification of transportation.

The renewable energy transition requires a new paradigm on the distribution and transportation grids. Unlike most non-renewable energy sources (nuclear and thermal power stations), renewable energy production is inherently distributed. To fully decarbonise the electrical grid, there must be nearly 100% penetration of renewable energy [6]. Renewable

Energy Resources (RER) like wind and solar energy are already competing in the energy market against more traditional non-RER [7]. Yet, to achieve net zero emissions, Energy Storage Devices (ESD) are required due to the intermittence, low duty cycle, and variability of RER.

In such a paradigm, with near 100% penetration of RER, the grid will be mainly dominated by power electronic inverters with completely decentralised energy generation. The two most direct implications are bidirectional power flows and the near absence of mechanical inertia. Consequently, several challenges arise in the electrical grid's stability [8]. Legacy power transformers and grid planning were designed under the principles of unidirectional power flow with sufficient inertia provided by the synchronous machines used in nuclear and thermal power plants.

Despite all the concerns, the share of renewable energy is increasing rapidly, forcing new paradigms in electrical energy distribution that require technological leaps, such as the massification of power electronics across electrical power systems.

With a contribution of 16.2% of the total CO_2 emissions worldwide, the transportation sector's electrification is also a vast challenge. In the past few years, most car manufacturers have started mass production of electric vehicles (EVs) and plug-in hybrid electric vehicles (PHEVs), with some manufacturers completely shutting down the development of combustion-only powertrains. An increase in market share in EVs and PHEVs ultimately means the demand for electrical grid energy will dramatically increase. This transition is only beneficial if RER can locally accommodate the increase in demand since, otherwise, the impact on CO2 can be undesirable (e.g. if the primary energy source is coal).

The usage of the energy stored in EVs and PHEV when connected to the grid enables concepts such as vehicle-to-grid (V2G) or vehicle-to-vehicle (V2V), where energy from the EVs or PHEV is shared with the grid or with other vehicles [9].

Still, in the topic of transportation, the reduction of emissions in the aviation sector is also a prominent topic. Solutions range from the use of sustainable aviation fuels, known as SAF, increased electrification of the aviation auxiliary systems (More Electric Aircraft [10]) to fully electric planes [11].

The generalised use of power electronics is the common factor in enabling the energy paradigm transition in the sectors mentioned above. Power electronics allow the interconnection of variable-speed electric machines, photovoltaic panels, and fuel cells, among other energy sources, to the grid. Power electronics provide grid resiliency and stabilisation solutions coupled with increased net efficiencies. Notably, power converters enable a key

technology for the future of grids and the transportation sector: the empowerment of transformers.

Solid State Transformers (SST) technologies enable the use of medium and high frequency (MF- tens of kHz and HF - hundreds of kHz) transformers that allow significant reductions in size and height of the MF/HF transformer (compared to the 60Hz/50Hz transformers for the same rated power) resulting in increased power densities. Power converters allow the grid interconnection of the MF/HF AC power transformers, as depicted in Figure 1.1, while gaining several control capabilities that are not attainable with traditional legacy transformers. Extra capabilities include power flow control, reactive power compensation, variable voltage gains and the capacity to compensate for transient voltage disturbances [12].

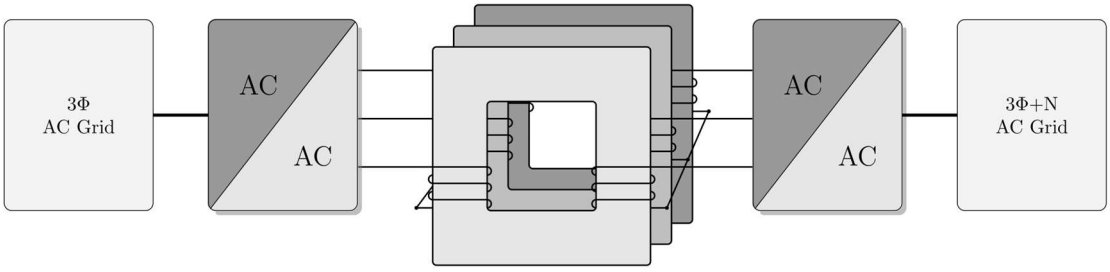
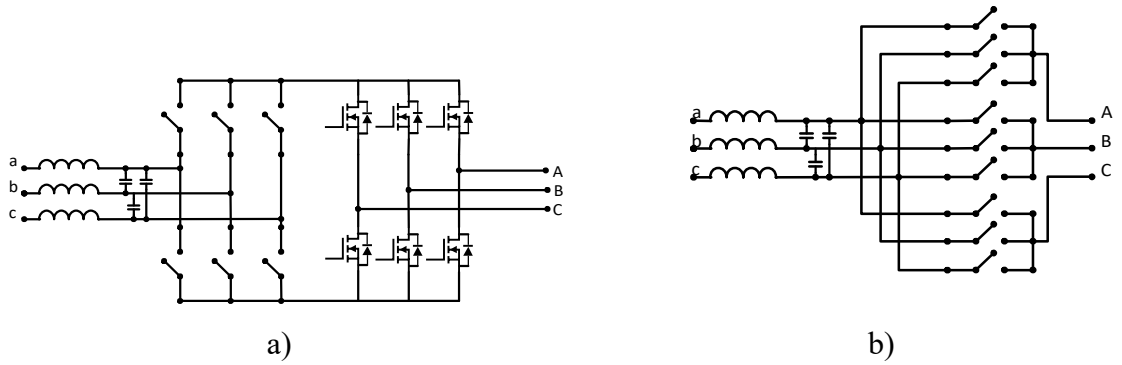


Figure 1.1 Depiction of a SST interfacing a 3 phase AC grid with a 3 phase grid with neutral using a MF/HF transformer and AC/AC power converters.

The increased power density makes SSTs an attractive replacement in transformers operating in volume and weight-sensitive applications (e.g. aviation, maritime transport, high population density areas, high rise buildings, etc…) while the SSTs controllability provides significant advantages over legacy distribution transformers, that can ultimately offer Distributed System Operators (DSOs) means to optimise efficiency, improve Power Quality (PQ) Indicators (PQI), increase grid resiliency, manage microgrids and facilitate the integration of RER [13].

Among AC/AC converters, Matrix Converters, shown in Figure 1.2, are power electronic AC/AC direct converters mainly characterised by using no intermediate storage. Detailed advantages of this converter will be covered in Section 2.2. It is important to note that today's industry penetration of matrix converters is reduced due to the many challenges that arise from using these converters [14]. Still, some industrial applications can be found for industrial motor drives [15] and marine systems [16]. Nonetheless, Matrix Converters can provide significant advantages in several power electronics fields [17], including SSTs. When implemented using new prominent semiconductor technologies such as reverse blocking transistors [18] and dual

gate transistors [19], the matrix converter might be just around the corner of a massive industry penetration, as detailed in section 2.3.



a) b)

Figure 1.2 Typical matrix converter topologies: a) Indirect Matrix Converter (IMC); b) Direct Matrix Converter (DMC).

SST technologies are an ideal fit in the Smart Grids (SG) concept, where controllability and resiliency are paramount [20,21]. These SG, also known as intelligent grids, use modern Information Technology (IT) and information infrastructure combined with grid-level controllability that allows management of bidirectional power flows in an automated manner capable of maximising efficiency, mitigating and minimising disturbances in a coordinated and fast manner. Furthermore, an SG is expected to accommodate events such as new power sources, loads and even new transmission paths while adapting the control strategies to attain the desired maximisation of efficiency [21,22].

Subjects such as SST topologies, analysis, control, modelling, and economic impact are trending research topics for all the above motives. Therefore, this work starts by providing a state-of-the-art in SSTs and then aims to propose a new SST topology using prominent semiconductor technologies and high-power density converters.

1.2 Thesis Proposal Outline

Chapter II presents a state-of-the-art on SSTs followed by a description of matrix converters and modern available power semiconductors.

In Chapter III, a new high-power density SST topology is proposed along with a modulation methodology that transforms the control action of a single matrix converter to the control action of the proposed SST while maintaining the isolation MF transformer outside of the saturation region. A new commutation method is developed and proposed that recirculates the energy

stored in the leakage inductance of the transformer, avoiding its interruption during the commutation process.

Chapter IV details the sizing of the input grid-connected filter, the MF transformer and the current and voltage control of the SST.

A set of simulation results and experimental results are shown in Chapter V, which focuses on validating the proposed original contributions of modulation and commutation methods.

Chapter VI draws a conclusion on the developed work and proposes future work to be built on the foundations laid by this work.

1.3 Thesis Objectives

This PhD aims to develop design methodologies, control and operation techniques for a new high-power density solid-state transformer topology operating in the MF and HF ranges. To achieve the proposed goals, this work is branched in the following objectives:

- To study different SST topologies;
- To propose a new SST topology, including converters to provide AC/AC and AC/DC with HF/MF galvanic isolation;
- To size an MF/HF transformer;
- To select new technologies of power semiconductors for the power converter design;
- To develop controllers that enable the use of the SST in SG by providing system controllability and resilience;
- To simulate the SST in different operation modes with balanced and unbalanced loads in grids with and without power quality issues;
- Design and build a scaled laboratory prototype to validate the topology and controllers and obtain efficiency and quality index metrics.

1.3.1 Thesis Original Contributions

During the development of this PhD thesis proposal, several challenges were faced related to the objective of obtaining an SST operating at MF/HF using matrix converters. Solutions for some of these challenges have led to some original contributions, which will be detailed in this document.

Summarily, the original contributions include:

a) A commutation method that enables using a matrix converter in the secondary of MF/HF transformers, where non-negligible leakage energy must be recirculated in a way that is not accommodated by traditional commutation methods. Even though this topic has been a target of some research by various authors, a particular implementation for three-phase systems was, to the best of the author's knowledge, published by the author of this proposal during his pursuit of a PhD.
b) A modulation method for a direct matrix converter-based SST that minimises the flux of the transformer and enables the immediate use of control methodologies designed for traditional 3×4 direct matrix converters to be employed in the proposed SST system.
c) An automated filter sizing mechanism using optimisation algorithms that obtains a desired attenuation profile while minimising the filter energy for 4th-order or higher filters.a
d) A control method for the SST input and output currents and the output grid voltages considering the dynamics of the optimised filter that resulted from the optimisation process.

These original contributions enable two particular innovations. First is the complete absence of intermediate energy storage in an SST with multi-phase transformers. Secondly, the SST converter can be controlled as if it were a single converter, enabling the use of well-known and tested control techniques to be directly applied to the proposed SST.

1.4 Publications

Hereafter follows a list of publications developed during this PhD thesis.

P. Costa, J. F. Silva, and S. F. Pinto, 'Experimental evaluation of SiC MOSFET and GaN HEMT losses in inverter operation', in IECON 2019-45th Annual Conference of the IEEE Industrial Electronics Society, 2019, vol. 1, pp. 6595–6600.

E. Youssef, P. Costa, S. F. Pinto, A. Amin, and A. A. El Samahy, 'Direct Power Control of a Single Stage Current Source Inverter Grid-Tied PV System', Energies, vol. 13, no. 12, p. 3165, 2020.

A. Pimenta, P. Costa, G. M. Paraíso, S. F. Pinto, and J. F. Silva, 'Active Voltage Regulation Transformer for AC Microgrids', in 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), 2020, pp. 2012–2017.

A. Bento, P. Costa et al., 'On the Potential Contributions of Matrix Converters for the Future Grid Operation, Sustainable Transportation and Electrical Drives Innovation', Applied Sciences, vol. 11, no. 10, p. 4597, 2021.

P. Lopes, P. Costa, and S. Pinto, 'Wireless Power Transfer System For Electric Vehicle Charging', in 2021 International Young Engineers Forum (YEF-ECE), 2021, pp. 132–137.

P. Costa, S. F. Pinto, and J. F. Silva, 'Breadth-First Search Leakage Tolerant Commutation Method for Matrix Converters in Three-Phase Solid State Transformers', in IECON 2021--47th Annual Conference of the IEEE Industrial Electronics Society, 2021, pp. 1–6.

L. Zhang, A. Bento, G. Paraíso, P. Costa, S. Pinto, and J. F. Silva, 'Novel Topology of Modular-Matrix-Converter-Based Smart Transformer for Hybrid Microgrid', in IECON 2021--47th Annual Conference of the IEEE Industrial Electronics Society, 2021, pp. 1–6.

P. Costa, G. Paraíso, S. F. Pinto, and J. F. Silva, 'A four-leg matrix converter based hybrid distribution transformer for smart and resilient grids', Electric Power Systems Research, vol. 203, p. 107650, 2022.

S. Javadi, P. Costa, et al., 'Grid current unbalance compensation using a fuzzy controlled smart transformer', Electric Power Systems Research, vol. 209, p. 108041, 2022.

L. Zhang et al., 'Multiple modularity topology for smart transformers based on matrix converters', IET Electric Power Applications, vol. 16, no. 8, pp. 926–940, 2022.

P. Costa, S. F. Pinto, and J. F. Silva, 'Multi-objective optimization of high order input filters for grid connected converters using Genetic Algorithms', in IECON 2022--48th Annual Conference of the IEEE Industrial Electronics Society, 2022, pp. 1–6.

P. Costa, S. Pinto, and J. F. Silva, 'A Novel Analytical Formulation of SiC-MOSFET Losses to Size High-Efficiency Three-Phase Inverters', Energies, vol. 16, no. 2, p. 818, 2023.

L. Zhang, P. Costa et al., 'Capacitor voltage balancing with switching sequence strategy for series-connected matrix-converter-based smart transformer', Electric Power Systems Research, vol. 225, p. 109857, 2023.

P. Costa, S. F. Pinto, and J. F. Silva, "Finite set predictive control of a boost matrix converter with a 3rd order output filter", in IECON 2023--49th Annual Conference of the IEEE Industrial Electronics Society, 2022, pp. 1–6.

Chapter 2

SOLID STATE TRANSFORMERS: STATE-OF-THE-ART

The development of SSTs encompasses challenges such as control, topologies and topological constraints, MF/HF transformer design, filters and protection circuits, commutation methods and application-specific challenges [23]. Research on these challenges will allow SST to become a disruptive technology, particularly for electrical power distribution grids [13].

This chapter will overview SST technologies, including their types and main applications. As presented in the introduction, building SSTs using matrix converters can provide unprecedented power densities and is an ongoing research topic. Therefore, an overview of matrix converters topologies and control techniques follows the SST state-of-the-art.

Switching power semiconductor devices are the main building blocks of any power electronics converter. Silicon semiconductors are the de facto standard for most power converter designs. However, semiconductors with a higher bandgap than Silicon, called wideband-gap semiconductors, are rapidly penetrating the industry, and, as such, a section is dedicated to them at the end of this chapter.

2.1 Solid State Transformers

2.1.1 The Concept of Solid-State Transformers

In general terms, an SST is composed of a transformer operating at a frequency much higher than the grid frequency of 50-60 Hz. This transformer, operated either at a medium frequency (MF- tens of kHz) or at high frequency (HF - hundreds of kHz), interfaces with two or multiple low-frequency LF (50-60 Hz) grids or DC systems using power converters (hence the name solid state)[1]. There are two striking differences between SST and classical transformers: 1) the

[1] Some authors have a wider definition for SST where they also classify as SST transformers with only a front-end converter where the transformer is operating at low frequency [35]. In this work these transformers with a front-end converter are named Hybrid Transformers which fall outside of the proposed work scope.

use of MF and HF in the transformer allows for higher power densities in the transformer; 2) the use of power converters provides several degrees of controllability whereas a classical transformer has very few (e.g., electronic tap changers);

The power handling capability of transformers is well known to be a function of the product between the transformer window area and the transformer core cross-section [24]. This product, often called Area Product, A_p, can be given by (2.1).

$$A_P = \frac{S_p(1+\sum_i S_{Si}/S_P)}{k_f B_m f_s J_{Co} k_{co}} \tag{2.1}$$

S_P and S_{Si} are the primary winding apparent power and the apparent power of the ith secondary winding, respectively, B_m is the core's saturation flux density, J_{Co} and k_{co} are the current density and winding filling factor, respectively, k_f is the waveform factor and f_s is the frequency. In this area product rule lays the essence of several transformer design methods. With some basic assumptions on the transformer dimensions, it is fair to say that the transformer volume and weight are roughly proportional to $A_p^{3/4}$. Further inspection allows the relation in (2.2) where V_t is the transformer volume.

$$\frac{S_P}{V_t} \propto \frac{A_p}{A_p^{3/4}} f_s = A_p^{1/4} f_s \Big|_{J_{Co},k_{Co},B_m,k_f=\text{const}} \tag{2.2}$$

The relation in (2.2) states that the power density of the transformer is proportional to the frequency and to the fourth root of the area product, when the current density, filling factor, waveform factor and the magnetic flux density saturation remain constant. Even though it is somewhat apparent that the transformer design for HF and MF involves different magnetic materials and perhaps even different design methodologies depending on the application, the relation in (2.2) reveals that increasing the operating frequency has a more significant impact on power density than increasing the transformer size.

Combined with modern power converter power densities of tenths of kW per dm^3 [25], it becomes clear that the use of MF or HF SSTs will lead to higher power densities. With modern power converters being able to efficiently process power while switching at frequencies around several tens of kHz, the power density of SST can be improved by two orders of magnitude [26].

The second highlighted advantage of SST is brought by the use of controlled power converters. Power converters allow new degrees of controllability, such as voltage level control, dynamic voltage restoration, and power flow control, to name a few. This new paradigm of

providing controllability to a transformer promises increased flexibility and enabling features in the power distribution grid [27], airborne applications [28], in EV charging stations [29], subsea power grid [30], marine vessels [31], DC grids [32] and renewable energy generation [33]. The concept of a smart transformer is roughly defined as a transformer capable of handling tasks that were once "difficult or even impossible" to traditional bulky transformers [34]. This topic will be further extended in section 2.1.2, where more details will be given on the advantages of controllability in SST.

As is the case with power converters, SSTs can be obtained with a multitude of different topologies and configurations. To better frame the topology proposal provided in this work, a brief discussion of SSTs AC front and back-ends is enclosed hereafter.

SST types depend on the type of converter used at the primary and secondary of the HF/MF transformer. For most topologies, we can group these SSTs according to Figure 2.1. The MF/HF transformer can be interfaced by an AC/AC converter without intermediate energy storage, such as matrix converters, and an AC/AC converter with intermediate energy storage, such as an association of rectifier and inverter. The combinations of these converters across the primary and secondary of the transformer led to the four possible configurations depicted in Figure 2.1.

Each solution has merits and demerits; the most power-dense topology is the one in Figure 2.1 b) since no intermediate storage is required. The use of intermediate storage (be it on the primary or secondary side converter) enables the decoupling of the input and output dynamics, which might be helpful to optimise each converter better [35]. Even though on the primary side, single boxes are used to depict AC/AC and AC/DC converters, it does not necessarily mean a single converter and can be an association of series and parallel converters, as it will be approached later in this section.

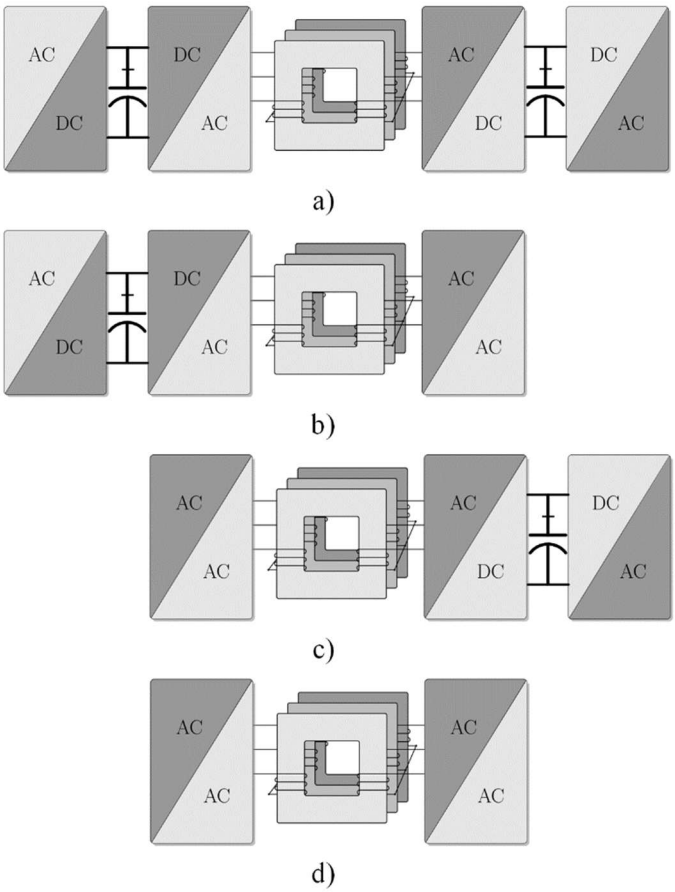


Figure 2.1 Arrangements of SST reagarding the use of intermediate storage: a) Direct conversion at the primary and indirect conversion with energy storage at the secondary; b) Direct conversion at both the primary and secondary; c) Indirect conversion with intermediate energy storage at both the primary and secondary. d) Indirect conversion with intermediate energy storage at the primary and direct conversion at the secondary.

SST configurations also depend on their MF/HF transformer configuration. A three-phase to three-phase system can be interconnected using a single-phase transformer, a three-phase transformer or even multiple transformers that have, or don´t have, magnetic coupling among each other. Though not depicting every possible solution, Figure 2.2 shows configurations for a single-phase transformer, a three-phase transformer, a multiport transformer and three single-phase transformers (for simplicity, all the converters are depicted as AC/AC converters).

Figure 2.2 a) depicts an SST using a single-phase transformer interfacing two three-phase AC systems. Figure 2.2 b) makes use of a three-phase transformer. Figure 2.2 c) interleaves three three-phase converters on the primary side for a single three-phase converter on the secondary side. Finally, Figure d) shows the interface of two three-phase AC grids by three single-phase transformers with six single-phase converters. The depicted configurations offer the numerous arrangements possible without entering deeply into the details of HF/MF

transformer designs, which need to account for power density, efficiency, and cooling requirements and are often the result of optimisation processes such as in [36].

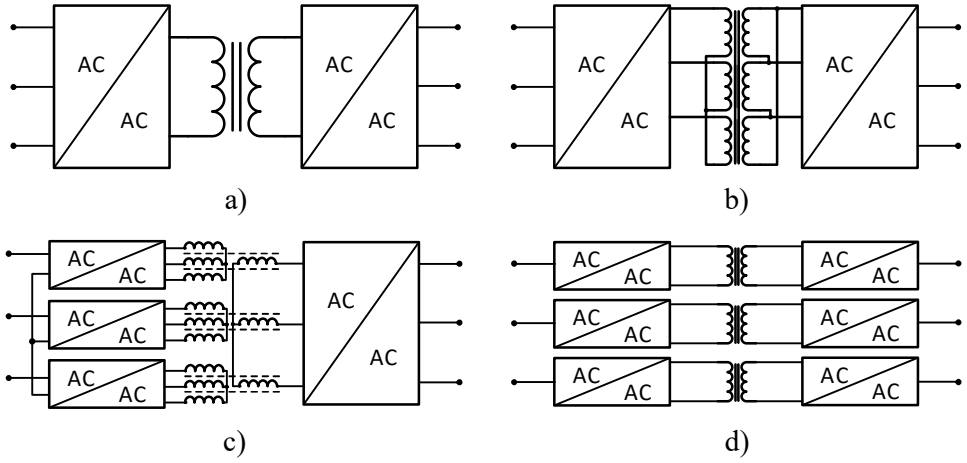


Figure 2.2 Arrangements of SST regarding number of phases and modularity of the MF/HF transformer: a) Single phase transformer; b) Three phase transformer. c) Three three-phase to single-phase transformers; d) Three single-phase transformers.

SST types can further be grouped based on their modularity regarding the power converters. Series associations of power converters on the input side are commonly made so that the SST can withstand typical Medium Voltage (MV) levels (6kV~40kV) [37]. Modern power wideband-gap semiconductor technologies might allow the use of full-scale converters (not modular) connected to the MV in the near future. Nonetheless, numerous modular and cascaded converter topologies have been proposed [38]. It is advantageous to have some modularity on the secondary side of the converter, where the converters are generally placed in parallel.

As an illustrative example, a modular topology using a single-phase matrix converter at the secondary and modular bidirectional half-bridges at the input can be found in [39]. One of the main concerns of modular topologies (which mostly divide the MV grid voltages across multiple capacitors) is to ensure that the capacitor's voltage remains balanced, thus requiring specific modulation methods or controllers that provide such equilibrium.

Studies dedicated to this group of SSTs and further comparisons can be found in [35], [40], [41] and [42], where concepts such as converter cells are introduced to study different modular solutions.

The selection of topology will obviously vary according to the application. Different topologies will have different possible power densities, efficiencies, and particular commutation requirements. Despite all the differences, one common goal for all these topologies is to provide new unattainable degrees of controllability with a traditional

transformer. This is precisely the topic covered in the following section, which highlights the benefits of the control capabilities of SSTs.

2.1.2 Smart Solid-State Transformers

Smart Solid-State Transformers, hereby referred to as Smart Transformers, usually extend the capabilities of traditional transformers to a point where the controllability advantages will enable prominent future technologies.

Traditional transformer controllability only extends a little beyond electronic tap-changers that enable the change, in a relatively slow and discrete manner, of the turns ratio of the transformer, allowing the control of the output voltage level. This mechanism is essential to satisfactorily control the grid voltage level under different loads, even if the changing of the transformer taps is made at the grid fundamental frequency.

Smart Transformers can benefit from using controlled power converters, allowing them to improve PQI parameters and mitigate disturbances actively. This is particularly important in future grids where a high level of intermittent and decentralised renewable energy must account for the majority of the grid energy production. RER production patterns have low-duty cycles and vary seasonally and daily, which can result in bidirectional power flows across distribution transformers [43] for which traditional transformers were not designed. Furthermore, most renewable energy generation connects to the grid using power converters, and as such, the inertia once provided by the synchronous machines primarily used in non-renewable energy sources' power plants must be emulated in some manner.

To accommodate all these issues, the concept of SG is an imminent reality facilitated by the ever-growing IT infrastructure and decreasing costs of power converters.

Smart Transformers as a key technology for the Smart Grid

The 20th-century power grid is built around the paradigm of a reduced number of centralised power generation plants to produce the electrical energy to be transmitted and distributed across residential areas, industrial parks, illumination systems and many other customers. This centralised paradigm eases the control of production/consumption equilibrium, a problem well characterised and dominated worldwide [44].

However, new paradigms on energy generation from renewable sources have led to significant scientific research, the electrical industry, and governmental efforts to develop SGs (also referred to as future grids or intelligent grids). The vision behind these SGs is to combine modern IT infrastructures that enable the sharing of high payloads of metering information in real-time with almost negligible costs, computational power, artificial intelligence, and modern power electronic converters to empower the transport and distribution grids with unprecedented levels of available information and controllability.

Part of this transition has already begun. As an example, as of 2021 in Portugal, most residential consumers are equipped with "smart" metering devices that report consumption information combined with power quality indicators to the system operator of the distribution electrical grid, allowing for faster issue solving, thus providing a better service to the customer.

In the next few decades, this transition is expected to accelerate until a whole new paradigm of energy production, transport, distribution, and consumption is achieved. In this new paradigm, SGs maximise the entire system efficiency in real-time by locally matching distributed production units to local consumption, minimise the grid carbon footprint, improving overall power quality, providing dynamic resiliency and disturbances mitigation while using predictive maintenance that can avoid faults, easily accommodate new generation units and dynamically control energy storage systems reducing the peak power demand of generation and handle the randomness of renewable energy generation [21].

Extensive surveys have been done on all the technologies required to attain SG [21,45,46] with clear conclusions on the necessity of this evolution and highlighting standards, technologies and regulations dedicated to SG. Smart grids will also impact the energy market operation, as highlighted in [47], and face significant challenges to creating communication systems that efficiently, safely, and securely manage all the required information traffic for this technology [22]. Though extremely relevant, these last two topics fall outside of the scope of this work; as such, little mention of them will be given in detriment of issues that relate closer to this work.

The critical point of having so much information available is to be able to impact the grid with controllable devices. In such a paradigm, these devices are mainly controlled power electronic converters. Power electronic converters are somewhat already and will increasingly be present in most loads, production centres, grid support systems like Flexible AC Transportation Systems (FACTS), protections and transformers across the grid. SSTs, in particular, are key technologies at the distribution level that can directly impact some of the above-mentioned smart grid concepts. SSTs can efficiently accommodate bidirectional power

flows, improve overall PQI, and mitigate upstream and downstream disturbances, resulting in a more resilient grid that ultimately provides a better service to producers and consumers.

SST is now considered the key enabling technology for the modernisation of the electrical grid [47]. In summary, SSTs bring the following advantages (compared to traditional distribution transformers): Reduced installation area and volume of distribution transformers [48]; 2) Capability of input reactive power control for MV grid support [12]. 3) Improvement of PQIs [12,48,49]; 4) Mitigation of very short, short or sustained disturbances[49]; 4) Power flow control [50]; 5) Efficient handling of bidirectional power flow [32,47,51]; 6) Direct integration of renewable energy sources (such as wind turbines [32] or photovoltaic panels [52]), DC outputs for microgrids [33] and energy storage devices [53].

Figure 2.3 depicts some examples of grid disturbances that can be downstream mitigated using SST. Voltage sags and swells as per Figure 2.3 b) and c) fall within the scope of dynamic voltage restorers, which is attainable by most SST topologies suggested in literature with output voltage controllers [35]. Figure 2.3 a), d), e), f), g) and h) depict, respectively, harmonic distortion, voltage flicker, voltage surges, voltage unbalances, short-time interruptions and long-time interruptions.

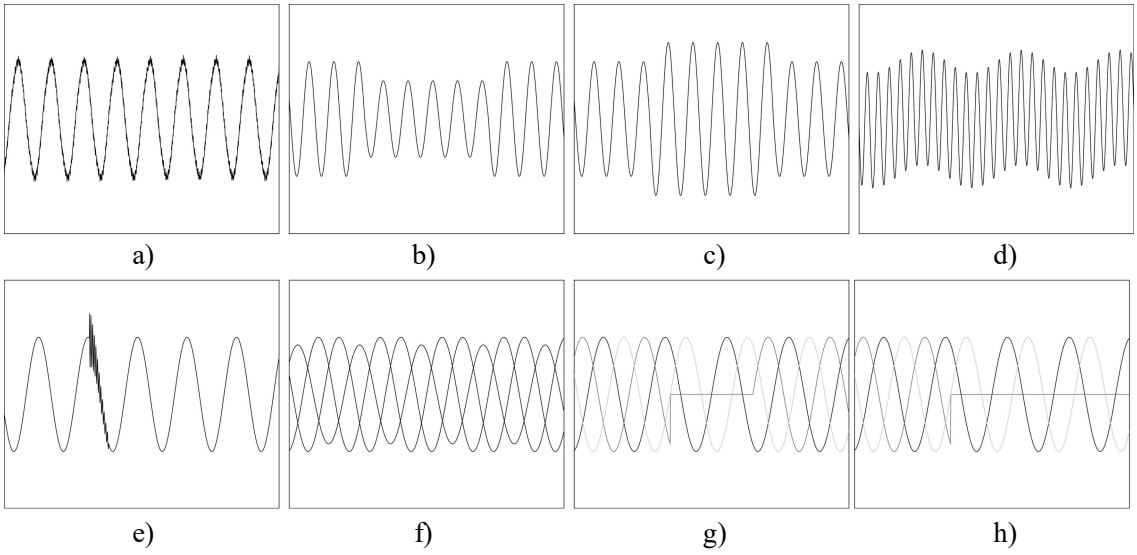


Figure 2.3 Typical grid voltage disturbances a) Harmonic distortion; b) Voltage sag; c) Voltage Swell; d) Flicker; e) Voltage surge; f) Voltage unbalance; g) Single-phase short interruption; h) Single-phase long interruption.

Even if particular examples of SSTs mitigating these issues are not directly found in the literature, there are extensive examples of the use of power converters to mitigate these issues, which can possibly be adapted directly into most SST topologies.

SSTs can also be an excellent solution to accommodate and manage multiple outputs such as microgrids, EV charging stations and renewable energy production. These additional integrated systems make SSTs an attractive investment in the near future. In the typical power range of distribution transformers, SSTs are expected to cost around five times more than traditional transformers and, as such, might not be currently attractive for situations where ancillary services are not necessary, and an LV AC environment already exists [54].

Smart Transformer Application Examples

In [55], a modular SST topology is proposed for ultrafast EV charging stations using a series association of converters to withstand the MV voltage levels, where several batteries can be charged individually for a battery-swap station. The proposed controllers combined with bidirectional power flow capability also allow power transfer from the battery to the grid. However, the topology only outputs DC ports, which are suitable to charge EVs or create DC microgrids and would require an additional power conversion state to obtain an AC grid.

Another proposal for an SST with EV charging capability is proposed in [52], where the authors propose an energy management scheme which includes the support of PV arrays while providing reactive power compensation and frequency regulation. A scaled and experimentally tested multiport transformer SST is presented in [56], managing both an EV charging station and stationary charge for both grid ancillary support and fast vehicle charging. The use of a grid-side Matrix Converter provides additional power density. However, the proposed topology uses three single-phase HF transformers, whereas a three-phase transformer would provide better power density.

An SST topology and model are presented in [57] for an SST that serves as a distribution transformer combined with local energy storage and local energy generation while proposing a control technique that takes into account the cross-coupling between all the transformer windings necessary to accommodate loads, generation storage and MV grid. Similar considerations are made in [33], where the work studied the integration of SSTs in DC microgrids that also support energy generation units and storage. However, for both works, using multiple AC/DC and DC/AC conversion stages requires intermediate energy storage that results in decreased power density and a reduced lifetime of the converters.

A final mention of the potential contributions of SSTs is their ability to emulate inertia, in this case called virtual inertia. This is particularly relevant since most of the grid's inertia is provided by synchronous generators, which are mostly used along with non-renewable power

sources. With solar and wind energy occupying a considerable percentage of the energy mix in Europe (with expected growth in the coming years), alternative methods for frequency regulation must be studied and implemented in the grid.

Virtual inertia research tackles open challenges such as grid integration of virtual inertia systems, inertia estimation, modelling and control method of aggregated virtual inertia systems, energy storage resources and management, as well as market structures for virtual inertia [58].

Smart Transformers in airborne, marine and railway applications

Smart Transformers also play a role in transportation systems. In these applications, besides the already well-stated advantages of extra controllability degrees, specific power and power density are also extremely important, with several researchers considering these applications as the first entry point of SST technology [13,23].

The More Electric Aircraft (MEA) is presented as a transition concept of the aviation sector towards full electrification. MEA concept proposes the transition of hydraulic and pneumatic systems within the aircraft to electrical systems, thereby removing the jet engine's bleed system that powers hydraulics and pneumatics, resulting in increased efficiency [10].

The use of SST systems in the MEA, though at the cost of increased complexity, is seen as a way to improve system reliability with power flow control in multiple DC grids and optimisation of storage systems [59]. The same authors in [60] propose a multiport SST that controls power flow while managing an energy storage device for an MEA, showing efficiencies in the range of 96%.

Shipboard systems also benefit significantly from the SST's increased power density. In [61], it is shown that using an SST-based rectifier reduces the weight by a factor of ten with one-third of the volume of the equivalent 60 Hz transformer. The same work also highlights the benefits of SSTs combined with wideband-gap semiconductors for the (Medium Voltage Direct Current) MVDC grid in future shipboard power systems, as is also discussed in [62].

Proposals for an SST that interfaces ship to shore as an MV to LV transformer are done in [63], using 10kV SiC MOSFET devices installed inside a standard shipping container for easy modularity and mobility.

2.2 AC/AC Conversion with Matrix Converter

Matrix converters are AC/AC converters that do not require intermediate energy storage, unlike the indirect AC/AC Voltage Source Back to Back Converter, VSBBC, which is composed of two stages, one AC/DC rectifier and one DC/AC inverter decoupled by some energy storage device (typically electrolytic capacitors), such as depicted in Figure 2.4 a). Matrix converters only require input filters and can perform a direct AC to AC conversion as per Figure 2.4 b).

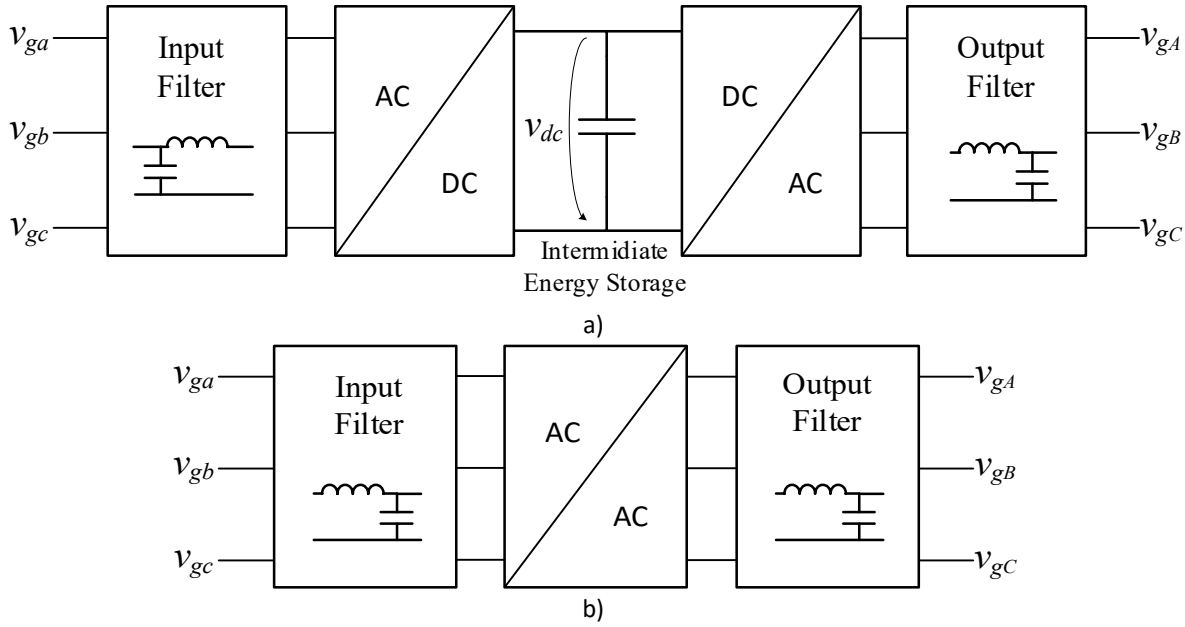


Figure 2.4 Depiction of AC/AC converter topologies – a) with intermediate energy storage, b) without intermediate energy storage.

Throughout this section, a comprehensive review is given on the most common matrix converter topologies, their advantages and drawbacks, how they compare to other AC/AC converters, their modulation and control techniques, as well as filters and protection circuitry sizing.

Compared to other topologies for AC/AC conversion, matrix converters suffer from coupled dynamics between the input and output, which increases control complexity and limits the control envelope (e.g. it is not possible to consume input reactive power when there is no active power). However, matrix converters offer some significant advantages:

- Power density in matrix converters is higher when compared to other AC/AC converters since it is primarily dependent on power semiconductors and does not require intermediate energy storage devices;

- Matrix converter's reliability can be higher given the lack of electrolytic capacitors, which tend to be a common failure point in VSBBC converters [64];
- Efficiency of matrix converters can surpass VSBBC in a wide range of operating conditions due to the lower voltage the semiconductors need to support [65];
- High switching frequencies enabled by recent power semiconductor technologies allow for low filtering requirements, further contributing to increased power densities.

As shown in the following sections, these advantages place Matrix Converters as a front-runner topology for future applications that demand AC/AC and even AC/DC conversion.

2.2.1 Bidirectional Switches

As stated, Matrix Converters are mainly composed of power semiconductors. More specifically, matrix converters use bidirectional switches that can be obtained with a variety of arrangements of forced and natural commutation power semiconductors.

The most straightforward format of a controlled bidirectional switch is depicted in Figure 2.5 a). It comprises a single Insulated Gate Bipolar Transistor (IGBT) and four diodes arranged as a full wave rectifier. When this bidirectional switch conducts (is ON), there are three semiconductors in the current path, and unlike the remaining bidirectional switch topology, this switch does not allow for selecting a particular current path and can only be controlled to be fully open or fully closed.

By far, the most typical bidirectional switch configurations are the common emitter anti-series IGBT switch depicted in Figure 2.5 b) and the common collector IGBT switch configuration Figure 2.5 c). When conducting, these switches have only two semiconductors in the current path (one diode and one IGBT).

Similar configurations as those described above can also be obtained using Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). Figure 2.5 d) and Figure 2.5 e) depict the common source and common drain configurations of the MOSFET bidirectional switches. Since MOSFETs can conduct in both directions when driven ON, the bidirectional switch current crosses both MOSFETs, given that typically, the MOSFET channel offers low resistance, the resulting voltage drop being less than the body diode threshold voltage.

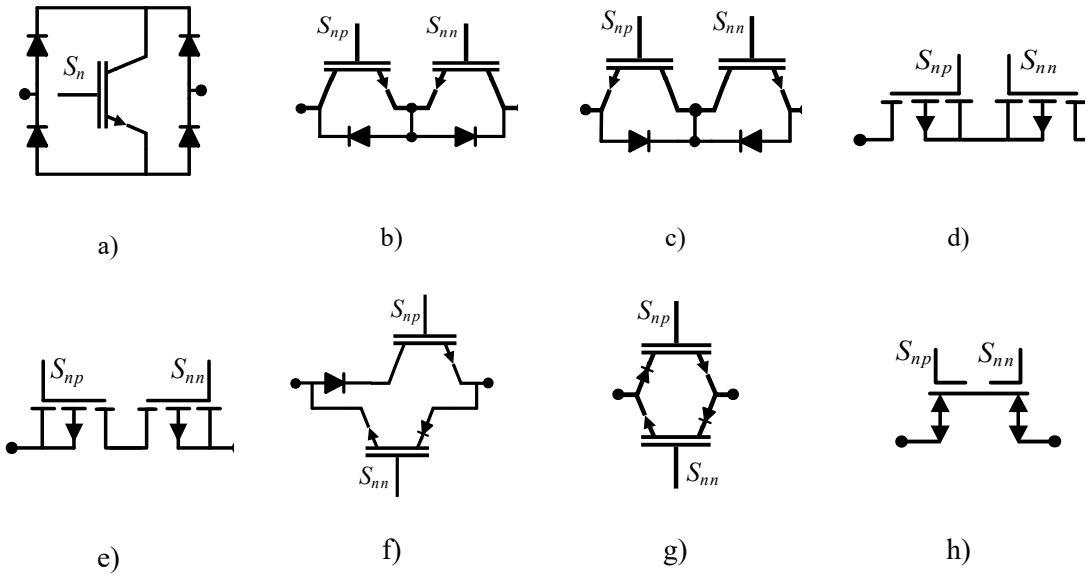


Figure 2.5 Bidireciontal (or four-quadrant) switches configurations: a) Single IGBT with rectifier diodes; b) Common emitter IGBTs; c) common collector IGBTs; d) commong source MOSFETs; e) common drain MOSFETs; f) Reverse-blocking IGBT for forward conduction plus series diode and IGBT for reverse conduction; g) Anti-parallel reverse blocking IGBTs; h) bidirectional (dual gate) JFETs.

Reverse-blocking IGBTs (RB-IGBTs can block reverse voltages, whereas a common IGBT cannot hold off a few tens of volts. The advantage of RB-IGBTs for bidirectional switches is having only one semiconductor in the current path when conducting, resulting in reduced conduction losses. However, RB-IGBTs are usually slower than IGBTs, leading to increased switching losses. Thus, RB-IGBTs could be attractive for switching frequencies in the low tens of kHz.

Figure 2.5 f) shows a bidirectional switch where a single RB-IGBT replaces one diode and one IGBT. Since RB-IGBTs are considerably more expensive and less widely available than typical IGBTs, this hybrid solution can be used in applications where a bidirectional switch is required, but the current has a more preferential direction. Figure 2.5 g) portrays a bidirectional switch using two RB-IGBTs; therefore, despite the current direction, only one semiconductor is crossed.

A significant mention must go to the bidirectional JFETs depicted in Figure 2.5 h). These monolithic devices are capable of blocking in both directions with a single conducting channel and a dual gate that allows for the control of the current flow direction. These devices are relatively recent but can ultimately be the breakthrough that will enable matrix converters to penetrate industrial and other prominent sectors fully. Similarly to the RB-IGBTs, the switch only has one semiconductor in the current path when conducting. Therefore, a single

bidirectional JFET can work as a four-quadrant controlled switch, whereas two RB-IGBT devices are required to accomplish the same function.

A deeper insight into modern wideband-gap semiconductor technologies is given in Section 2.3, whose superior characteristics when compared with silicon semiconductors, are particularly relevant to matrix converters.

2.2.2 Single and Dual Stage Matrix Converters

Single-stage matrix converters, depicted in Figure 2.6, are also known as Direct Matrix Converters (DMC) and are composed of $m \times n$ bidirectional switches, where m is the number of output phases and n is the number of input phases, e.g. a 3×3 DMC is typically composed of 9 bidirectional switches. In comparison, a 4×3 DMC requires 12 bidirectional switches (most controlled bidirectional switches need at least two transistors and two diodes, as shown in section 2.2.1).

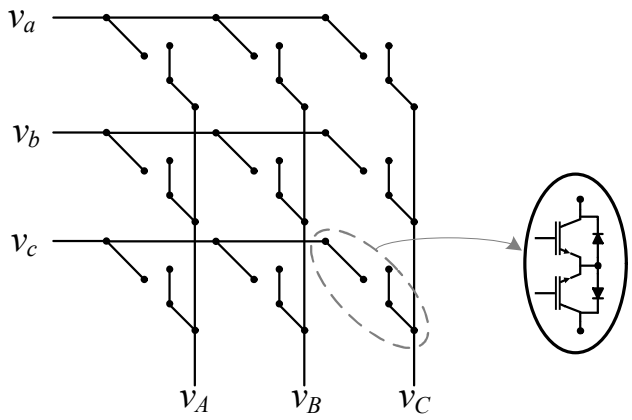


Figure 2.6 Depiction of a 3×3 DMC, where each switch is attained with a common emiter connection of two IGBTs.

Dual-stage Matrix converters, depicted in Figure 2.7, use an input rectifier stage with no energy storage called virtual or soft DC-link, followed by a DC/AC inverter stage. Dual stage Matrix converters are typically referred to as Indirect Matrix Converters (IMCs). The most typical IMC topology uses $2 \times n$ bidirectional switches plus $2 \times m$ switches, as shown in Figure 2.7 b). In an effort to reduce the switch count of the IMC, some authors developed IMC-based topologies that required less controlled switches. The most known IMC topologies are known as Sparse IMC (SIMC), shown in Figure 2.7 c), Very Sparse IMC (VSIMC), shown in Figure 2.7 d), and Ultra Sparse IMC, depicted in Figure 2.7 e).

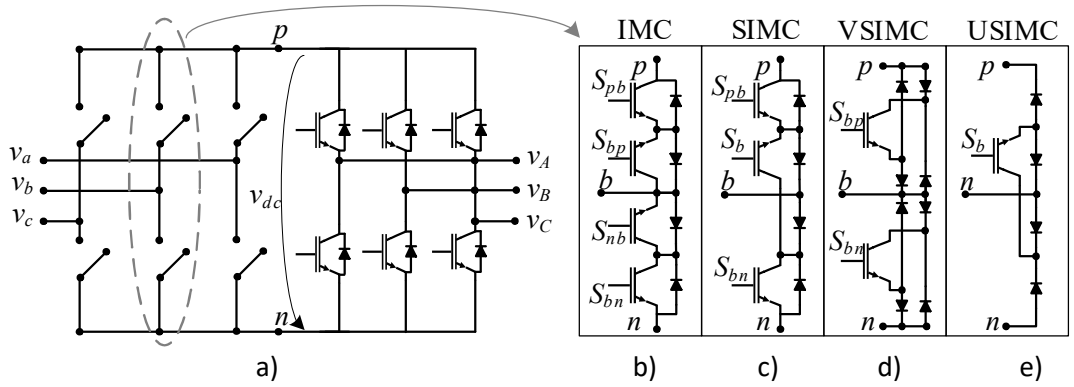


Figure 2.7 Depiction of a 3×3 IMC in it's: a) classical topology; b) Sparse topology; c) Very Sparse topology; d) Ultra Sparse topology.

IMCs are a desirable solution for systems with a high output phase count, e.g. polyphase electric machines, since they will have substantially fewer switches. However, the bidirectional switch count is the same for a system with three input and three output phases.

2.2.3 Commutation Methods of DMC

To change the state of DMC bidirectional switches, dedicated commutation methods have been utilized to ensure that the input capacitor voltages are not short-circuited during the transition, nor are the output inductor currents opened. The commutation methods can be based on either the output current sign, or the input voltage signs, and they can be either two-step or four-step methods; these methods are well-known and extensively detailed in [64]. Therefore, only a brief explanation of the methods is undertaken in this document.

Current sign-based commutation methods use the signs of the output currents to know which semiconductor is forward conducting in the bidirectional switch. In four-step commutation methods, the first step is to drive the non-conducting devices to the OFF state. In the second step, after a short dead-time, the semiconductor devices to be put into conduction (ON state) to carry the output currents are driven to the ON state. After another slight delay, the third step drives open (OFF state) the semiconductor devices that were carrying the output currents in the first step. In the fourth step, the non-conducting semiconductor devices from the conducting bidirectional switches are driven to the ON state. The depiction of this process as a state machine can be seen in Figure 2.8.

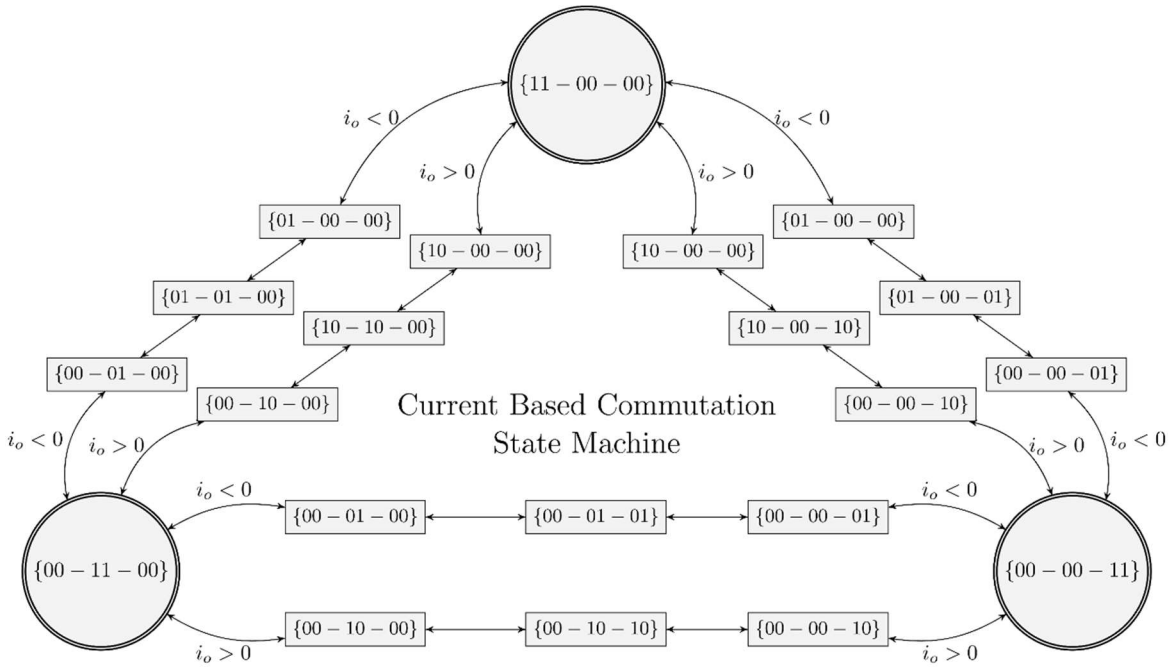


Figure 2.8 State Machine representation of the four-step current based commutation scheme for one direct matrix converter leg. The states are represented as $\{S_{x1p}\ S_{x1n}\text{-}S_{x2p}\ S_{x2n}\text{-}S_{x3p}\ S_{x3n}\}$ where 1 means that the transistor is commanded to the on state and 0 the transistor is commanded to the off state, S_{x1p} represents the transistor that connects the input phase 1 to the output phase x capable of carrying positive biased current, while S_{x1p} represents the transistor that connects the input phase 1 to the output phase x capable of carrying negative biased current.

The two-step method based on the current is similar to the four-step method, where the first and fourth steps are neglected, and as such, only one semiconductor device is driven to the ON state per conducting switch. Consequently, this method must change the conducting device every time the output current sign changes.

The voltage sign-based commutation methods use the signs of the input voltages to know which semiconductor device can be closed without short-circuiting the input capacitors. The commutation process is then similar to the current-based commutation but concerns the short-circuiting of the input capacitors. The depiction of this process as a state machine is shown in Figure 2.9.

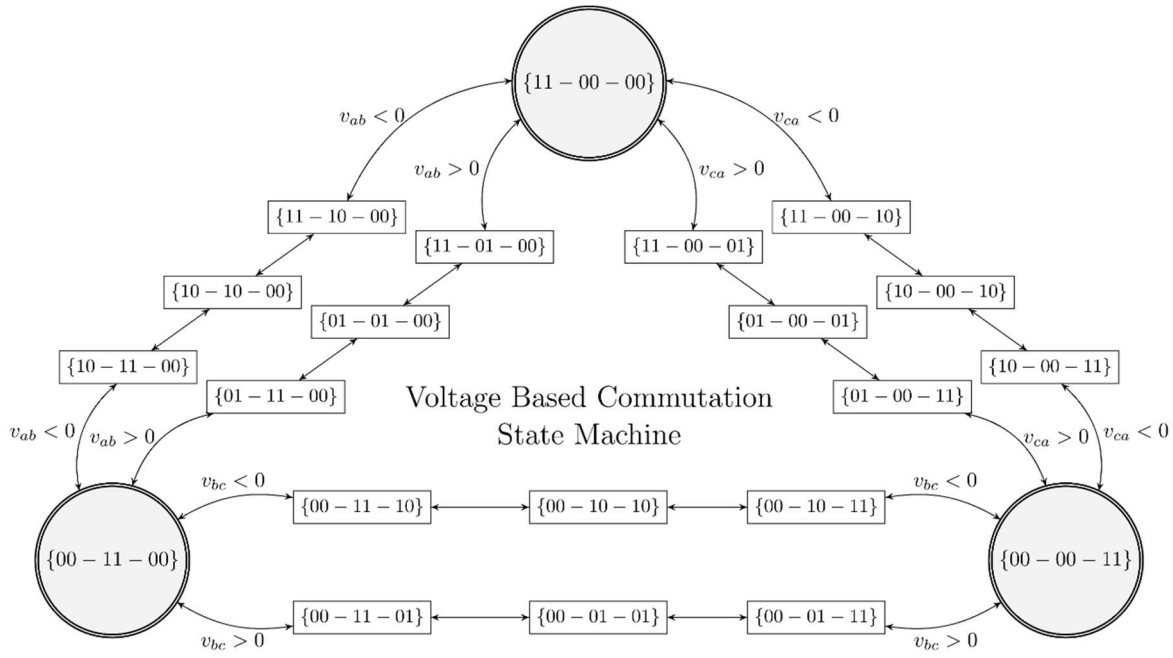


Figure 2.9 State Machine representation of the four-step voltage-based commutation scheme for one direct matrix converter leg. State description is similar to Figure 2.8.

2.2.4 Model of a Multiphase DMC

Consider the $n \times m$ DMC of Figure 2.10, which is composed of n input and m output phases with $n \times m$ switches.

Assuming the bidirectional switches depicted in Figure 2.10 behave as ideal switches, i.e. with zero conduction resistance, zero switching time and no leakage currents, then the state of each bidirectional switch can be represented by the variable S_{kj} (where k and j represent the output and input phase of the switch, respectively). This variable assumes the value of "1" when the switch is closed (ON state) and the value of "0" when the switch is opened (OFF state), as per (2.3).

$$S_{kj} = \begin{cases} 1 \ , \ \text{Switch is in closed state} \\ 0 \ , \ \text{Switch is in open state} \end{cases} \tag{2.3}$$

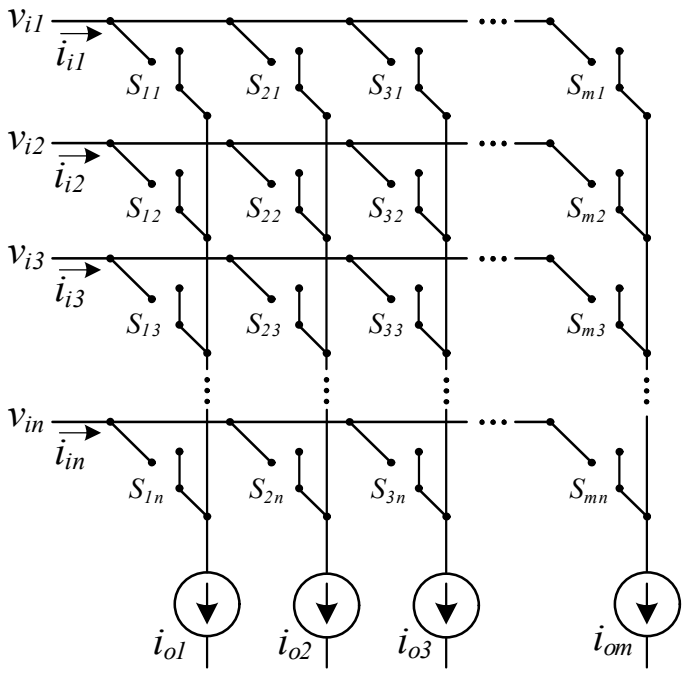


Figure 2.10 Multiphase model of a DMC with n input phases and m output phaes

The matrix $\mathbf{S}$ can then be defined as representing all the switch states of the $n \times m$ DMC according to (2.4).

$$\mathbf{S} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & \cdots & S_{1n} \\ S_{21} & S_{22} & S_{23} & \cdots & S_{2n} \\ S_{31} & S_{32} & S_{33} & \cdots & S_{3n} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ S_{m1} & S_{m2} & S_{m3} & \cdots & S_{mn} \end{bmatrix} \tag{2.4}$$

The set of possible combinations of the matrix $\mathbf{S}$ is $2^{m \times n}$, bounded by the topological constraints of the DMC; namely, the input phases cannot be shorted since they are expected to behave as voltage sources, and the output phases current cannot be interrupted since the output phases are expected to behave as current sources. These restrictions can be summarised in (2.5) , where it is seen that the sum of the switches states across a line of the matrix $\mathbf{S}$ must exactly equal the unity, ensuring that each output phase is connected to one, and only one, input phase using just one bidirectional switch.

$$\sum_{j=1}^{n} S_{kj} = 1 \quad k \in \{1, 2, ..., \mathrm{m}\} \tag{2.5}$$

The matrix allows the input line to be directly related to the neutral voltage of the output and to the line to neutral voltages at the input $\mathbf{v_i} = \begin{bmatrix} v_{i1} & v_{i2} & v_{i3} & ... & v_{in} \end{bmatrix}^{\mathrm{T}}$ as per (2.6).

$$\mathbf{v_o} = \begin{bmatrix} v_{o1} \\ v_{o2} \\ v_{o3} \\ \cdots \\ v_{om} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & \cdots & S_{1n} \\ S_{21} & S_{22} & S_{23} & \cdots & S_{2n} \\ S_{31} & S_{32} & S_{33} & \cdots & S_{3n} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ S_{m1} & S_{m2} & S_{m3} & \cdots & S_{mn} \end{bmatrix} \begin{bmatrix} v_{i1} \\ v_{i2} \\ v_{i3} \\ \cdots \\ v_{in} \end{bmatrix} = \mathbf{S}\mathbf{v_i} \tag{2.6}$$

Similarly, the transposed of the matrix $\mathbf{S}$ can be used to obtain the input currents $\mathbf{i_i} = \begin{bmatrix} i_{i1} & i_{i2} & i_{i3} & \ldots & i_{in} \end{bmatrix}^{\mathrm{T}}$ from the output currents $\mathbf{i_o} = \begin{bmatrix} i_{o1} & i_{o2} & i_{o3} & \ldots & i_{om} \end{bmatrix}^{\mathrm{T}}$ as per (2.7).

$$\mathbf{i_i} = \begin{bmatrix} i_{i1} \\ i_{i2} \\ i_{i3} \\ \cdots \\ i_{in} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{21} & S_{31} & \cdots & S_{m1} \\ S_{12} & S_{22} & S_{32} & \cdots & S_{m2} \\ S_{13} & S_{23} & S_{33} & \cdots & S_{m3} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ S_{1m} & S_{2n} & S_{3n} & \cdots & S_{mn} \end{bmatrix} \begin{bmatrix} i_{o1} \\ i_{o2} \\ i_{o3} \\ \cdots \\ i_{om} \end{bmatrix} = \mathbf{S}^{\mathrm{T}}\mathbf{i_o} \tag{2.7}$$

Simple algebraic manipulations of the matrix $\mathbf{S}$ can be done to obtain line-to-line output voltages from line-to-neutral output voltages or the other way around. These matrices will be used whenever the use of line-to-line voltages is advantageous. In the following sections, these general results will be particularised for the cases of a 3×3 and a 3×4 DMC.

2.2.5 Model of a Three-Phase DMC

Consider the three-phase converter with three output phases of Figure 2.11, where the input filter output has a voltage source characteristic, and the inductive load behaves at a small enough time scale as a current source. The resultant DMC converter uses nine bidirectional switches allowing a total of $3^3 = 27$ possible converter states.

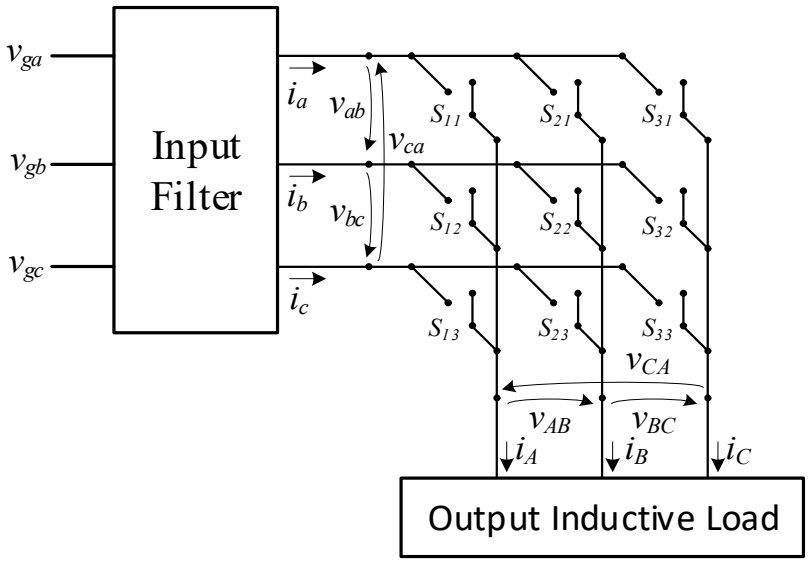


Figure 2.11 Model of a DMC with an input filter and an output inductive load with three input phases and three output phases

For this particular case, the matrix $\mathbf{S}$ is of size 3×3 and assumes the values shown in (2.8) with the restrictions of (2.9).

$$\mathbf{S} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \tag{2.8}$$

$$\sum_{j=1}^{3} S_{kj} = 1 \quad k \in \{1,2,3\} \tag{2.9}$$

To obtain the output line to neutral voltages from the input line to neutral voltages and the input converter currents from the output converter currents equations (2.6) and (2.7) can be used taking into consideration the matrix $\mathbf{S}$ from (2.8) and that $\mathbf{v_o}, \mathbf{v_i}, \mathbf{i_o}$ and $\mathbf{i_i}$ are vector matrices of size $[1 \times 3]$.

The switch combinations of all possible states (2^9) of (2.8) are constrained by (2.9) resulting in 27 possible combinations represented in Table 2.1. These combinations can be divided into three groups:

- combinations 1 to 6 use all three input voltages on the output and are characterised by imposing a null common mode voltage on the output;
- Combinations 7 to 24 use two different input voltages at the output, and for each combination in this group, there is another one that is symmetrical in the resultant output voltages and input currents. Furthermore, the first six combinations circulate

only the output current of phase A in the input, the second set of six only the current of phase B and the final six only the current of phase C;

- combinations 25 to 27 use only one input voltage applied to the output, resulting in zero amplitude input currents and zero amplitude output voltages.

Table 2.1 Possible combinations of a 3×3 DMC converter regarding to the states of the switches and resulting output voltages and input currents.

№	S_{11}	S_{12}	S_{13}	S_{21}	S_{22}	S_{23}	S_{31}	S_{32}	S_{33}	$v_A(t)$	$v_B(t)$	$v_C(t)$	$i_a(t)$	$i_b(t)$	$i_c(t)$
1	1	0	0	0	1	0	0	0	1	$v_a(t)$	$v_b(t)$	$v_c(t)$	$i_A(t)$	$i_B(t)$	$i_C(t)$
2	0	1	0	0	0	1	1	0	0	$v_b(t)$	$v_c(t)$	$v_a(t)$	$i_C(t)$	$i_A(t)$	$i_B(t)$
3	0	0	1	1	0	0	0	1	0	$v_c(t)$	$v_a(t)$	$v_b(t)$	$i_B(t)$	$i_C(t)$	$i_A(t)$
4	1	0	0	0	0	1	0	1	0	$v_a(t)$	$v_c(t)$	$v_b(t)$	$i_A(t)$	$i_C(t)$	$i_B(t)$
5	0	1	0	1	0	0	0	0	1	$v_b(t)$	$v_a(t)$	$v_c(t)$	$i_B(t)$	$i_A(t)$	$i_C(t)$
6	0	0	1	0	1	0	1	0	0	$v_c(t)$	$v_b(t)$	$v_a(t)$	$i_C(t)$	$i_B(t)$	$i_A(t)$
7	1	0	0	0	1	0	0	1	0	$v_a(t)$	$v_b(t)$	$v_b(t)$	$i_A(t)$	$-i_A(t)$	0
8	0	1	0	1	0	0	1	0	0	$v_b(t)$	$v_a(t)$	$v_a(t)$	$-i_A(t)$	$i_A(t)$	0
9	0	1	0	0	0	1	0	0	1	$v_b(t)$	$v_c(t)$	$v_c(t)$	0	$i_A(t)$	$-i_A(t)$
10	0	0	1	0	1	0	0	1	0	$v_c(t)$	$v_b(t)$	$v_b(t)$	0	$-i_A(t)$	$i_A(t)$
11	0	0	1	1	0	0	1	0	0	$v_c(t)$	$v_a(t)$	$v_a(t)$	$-i_A(t)$	0	$i_A(t)$
12	1	0	0	0	0	1	0	0	1	$v_a(t)$	$v_c(t)$	$v_c(t)$	$i_A(t)$	0	$-i_A(t)$
13	0	1	0	1	0	0	0	1	0	$v_b(t)$	$v_a(t)$	$v_b(t)$	$i_B(t)$	$-i_B(t)$	0
14	1	0	0	0	1	0	1	0	0	$v_a(t)$	$v_b(t)$	$v_a(t)$	$-i_B(t)$	$i_B(t)$	0
15	0	0	1	0	1	0	0	0	1	$v_c(t)$	$v_b(t)$	$v_c(t)$	0	$i_B(t)$	$-i_B(t)$
16	0	1	0	0	0	1	0	1	0	$v_b(t)$	$v_c(t)$	$v_b(t)$	0	$-i_B(t)$	$i_B(t)$
17	1	0	0	0	0	1	1	0	0	$v_a(t)$	$v_c(t)$	$v_a(t)$	$-i_B(t)$	0	$i_B(t)$
18	0	0	1	1	0	0	0	0	1	$v_c(t)$	$v_a(t)$	$v_c(t)$	$i_B(t)$	0	$-i_B(t)$
19	0	1	0	0	1	0	1	0	0	$v_b(t)$	$v_b(t)$	$v_a(t)$	$i_C(t)$	$-i_C(t)$	0
20	1	0	0	1	0	0	0	1	0	$v_a(t)$	$v_a(t)$	$v_b(t)$	$-i_C(t)$	$i_C(t)$	0
21	0	0	1	0	0	1	0	1	0	$v_c(t)$	$v_c(t)$	$v_b(t)$	0	$i_C(t)$	$-i_C(t)$
22	0	1	0	0	1	0	0	0	1	$v_b(t)$	$v_b(t)$	$v_c(t)$	0	$-i_C(t)$	$i_C(t)$
23	1	0	0	1	0	0	0	0	1	$v_a(t)$	$v_a(t)$	$v_c(t)$	$-i_C(t)$	0	$i_C(t)$
24	0	0	1	0	0	1	1	0	0	$v_c(t)$	$v_c(t)$	$v_a(t)$	$i_C(t)$	0	$-i_C(t)$
25	1	0	0	1	0	0	1	0	0	$v_a(t)$	$v_a(t)$	$v_a(t)$	0	0	0
26	0	1	0	0	1	0	0	1	0	$v_b(t)$	$v_b(t)$	$v_b(t)$	0	0	0
27	0	0	1	0	0	1	0	0	1	$v_c(t)$	$v_c(t)$	$v_c(t)$	0	0	0

For the particular case of 3×3 DMC, it is sometimes helpful to obtain the output line-to-line voltages as opposed to the line-to-neutral output voltages (since the neutral is virtual). For these cases, the output line-to-line voltages can be computed from the input line-to-neutral voltages, as per (2.10).

$$\begin{bmatrix} v_{AB} \\ v_{BC} \\ v_{CA} \end{bmatrix} = \begin{bmatrix} S_{11}-S_{21} & S_{12}-S_{22} & S_{13}-S_{23} \\ S_{21}-S_{31} & S_{22}-S_{32} & S_{23}-S_{33} \\ S_{31}-S_{11} & S_{32}-S_{12} & S_{33}-S_{13} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \mathbf{S}_{\ln} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.10}$$

It is also sometimes useful to define the line-to-line output voltages as a function of the line-to-line input voltages. The line-to-line input voltages relate to the line-to-neutral input voltages

according to (2.11). The resulting matrix is non-invertible; however, when considering that the sum of both the line-to-neutral and line-to-line voltages must be equal to zero, then the relation can be obtained.

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.11}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} \frac{1}{3} & 0 & -\frac{1}{3} \\ -\frac{1}{3} & \frac{1}{3} & 0 \\ 0 & -\frac{1}{3} & \frac{1}{3} \end{bmatrix} \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} \tag{2.12}$$

The relation between the input line-to-line voltages and the output line-to-line voltages can then be obtained by (2.14) while the relation between input line-to-line voltage and the output line-to-neutral voltage is given by (2.13).

$$\begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = \frac{1}{3} \begin{bmatrix} S_{11}-S_{12} & S_{12}-S_{13} & S_{13}-S_{11} \\ S_{21}-S_{22} & S_{22}-S_{23} & S_{23}-S_{21} \\ S_{31}-S_{32} & S_{32}-S_{33} & S_{33}-S_{31} \end{bmatrix} \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \mathbf{S}_{nl} \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} \tag{2.13}$$

$$\begin{bmatrix} v_{AB} \\ v_{BC} \\ v_{CA} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} S_{11}-S_{12}-S_{21}+S_{22} & S_{12}-S_{13}-S_{22}+S_{23} & S_{13}-S_{11}+S_{21}-S_{23} \\ S_{21}-S_{22}-S_{31}+S_{32} & S_{22}-S_{23}-S_{32}+S_{33} & S_{23}-S_{21}+S_{31}-S_{33} \\ S_{12}-S_{11}+S_{31}-S_{32} & S_{13}-S_{12}+S_{32}-S_{33} & S_{11}-S_{13}-S_{31}+S_{33} \end{bmatrix} \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \mathbf{S}_{ll} \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} \tag{2.14}$$

The resulting matrices $\mathbf{S}$, $\mathbf{s}_{\ln}$, $\mathbf{s}_{nl}$ and $\mathbf{s}_{ll}$ will be used to relate the input line to neutral voltages to the output line to neutral voltages, the input line to neutral voltages to the output line to line voltages, the input line to neutral voltages to the output line to line voltages and the input line to line voltages to the output line to line voltages, respectively.

2.2.6 Model of a Four-Phase DMC

Consider now the DMC from Figure 2.12 with three input phases and four output phases, and the same filter characteristics as the one stated in the above section. This converter is then composed of 12 bidirectional switches that allow 81 (3^4) different feasible combinations.

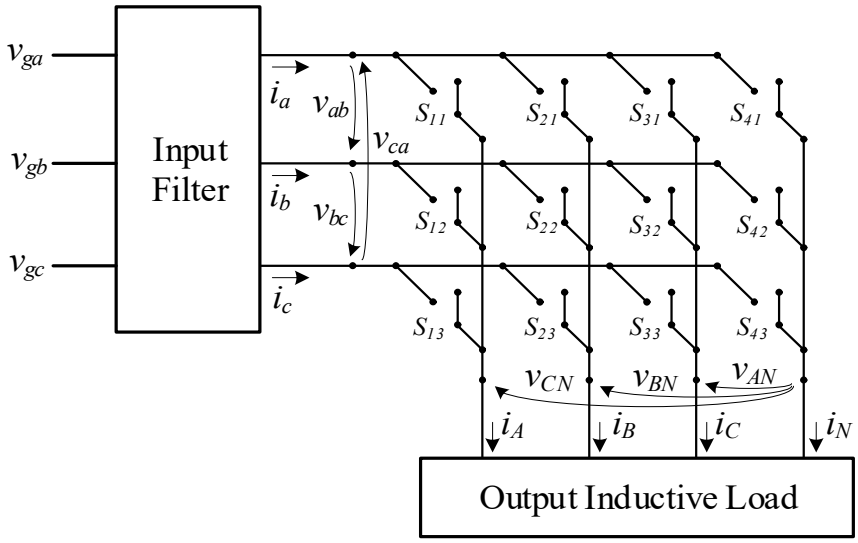


Figure 2.12 Direct Matrix Converter with three input phases and four output phases

The matrix $\mathbf{S}'$ [2] that defines the switches' states is now given by (2.15) with the constraints imposed by (2.16). Once again, this matrix relates the line to neutral input voltages $\mathbf{v_i} = \begin{bmatrix} v_a & v_b & v_c \end{bmatrix}$ with the line to neutral output voltages $\mathbf{v_o} = \begin{bmatrix} v_A & v_B & v_C & v_N \end{bmatrix}$ as well as the input and output converter currents of the converter $\mathbf{i_i} = \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}$ and through its transposed form. Notice that the line to neutral voltages represented are relative to a virtual neutral from the input side, which should not be confused with the output voltage v_N.

$$\mathbf{S}' = \begin{bmatrix} S'_{11} & S'_{12} & S'_{13} \\ S'_{21} & S'_{22} & S'_{23} \\ S'_{31} & S'_{32} & S'_{33} \\ S'_{41} & S'_{42} & S'_{43} \end{bmatrix} \tag{2.15}$$

$$\sum_{j=1}^{3} S'_{kj} = 1 \quad k \in \{1,2,3,4\} \tag{2.16}$$

As in most applications, the four output phases of the DMC converter will represent a three-phase system where the 4th leg is the neutral point of the output three-phase system. It is more intuitive to reduce the matrix $\mathbf{S}'$ to define the line to neutral voltages, $\mathbf{v_{oN}}$ (where this time the neutral refers to v_n) in function of the line to neutral input voltages (where this neutral refers to the input virtual neutral), which is represented in (2.17).

[2] Throughout the document the switch state matrix will be referred as $\mathbf{S}$ for the 3 × 3 DMC converter and as $\mathbf{S}'$ for the 3 × 4 DMC converter. Unless otherwise noted this added symbology is used for the same purpose in all other matrices derived from $\mathbf{S}$ or $\mathbf{S}'$.

$$\mathbf{v_{oN}} = \begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} = \begin{bmatrix} S'_{11} - S'_{41} & S'_{12} - S'_{42} & S'_{13} - S'_{43} \\ S'_{21} - S'_{41} & S'_{22} - S'_{42} & S'_{23} - S'_{43} \\ S'_{31} - S'_{41} & S'_{32} - S'_{42} & S'_{33} - S'_{43} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \mathbf{S'_n v_i} \quad (2.17)$$

The 81 different possible states regarding the output voltages and input currents are detailed in the two tables of Appendix A. The combinations present in Table A.1 are characterised by using only two of the possible three input voltages, and similarly to the 3×3 DMC, for each of these combinations, there is always a symmetrical state regarding the output voltages and input currents. The combinations numbered 43 to 78 present in Table A.2 are characterised by using all three input voltages; however, unlike the 3×3DMC, these vectors do not have zero common mode voltage. The last three states of Table A.2 are the zero states where only one of the input voltages is used, resulting in a zero-amplitude output voltage and zero amplitude input currents.

2.2.7 Matrix Converter Modulation and Control Techniques

In a summarised manner, this section will describe the main modulation and control techniques used to drive matrix converters with a particular emphasis on the DMC.

Two main modulation methods will be detailed: The first is the Venturini-Alesina modulation method proposed in 1981 [66] and further extended in 1989 [67]; this method was a major breakthrough in matrix converter research since it allowed for the simultaneous control of the output voltages and input currents [68]; The second modulation/control technique is Model Predictive Control (MPC), the current trend for the control of both DMCs and IMCs. This technique can be used with either a finite control set (where the output of the controller is directly the state of each switch) or with an infinite control set where the output of the controller is a voltage reference that is posteriorly applied at the input of a modulator [69].

An additional modulation technique and an additional control method are mentioned in this paragraph since they are typically used in matrix converters. However, they are not thoroughly detailed here for the sake of brevity, and they are Space Vector Modulation (SVM), commonly used in three-phase inverters, is also used in both 3x3 and 3x4 matrix converters to modulate references obtained from a variety of controllers [70]; Sliding Mode Control (SMC) which is a non-linear control technique successfully used to control a variety of switched power converters [71,72] since the late 80's.

Venturini-Alesina modulation

The Venturini-Alesina modulation (VAM) eased the practical usage of matrix converters. Besides its historical significance, VAM is still widely used, and some results of this work are extracted using this modulation method.

A brief overview of this modulation technique is provided in this section. The objective of the VAM is to obtain modulation indexes $m_{jk}(t)$, that when compared against carrier waves provide the state for each S_{jk} semiconductor of matrix (2.8) for the 3×3 DMC and of matrix (2.15) for the 3×4 DMC. These modulation indexes are time functions which are compared to triangular or sawtooth carrier waves to generate the driving signals that define the state of each semiconductor S_{jk}.

Venturini-Alesina Modulation in 3×3 DMC

To obtain the desired modulation indexes, the Venturini-Alesina method starts by defining the shape of the input voltages and output currents as per (2.18) and (2.19), respectively, where V_I and I_o are the input voltage and output current amplitudes, ω_i and ω_o are the angular frequencies of the input voltages and output currents, ϕ_o is the phase difference between the output current and the target output voltage and t is time.

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} V_I \cos(\omega_i t) \\ V_I \cos(\omega_i t - 2\pi/3) \\ V_I \cos(\omega_i t - 4\pi/3) \end{bmatrix} \tag{2.18}$$

$$\begin{bmatrix} i_A(\mathrm{t}) \\ i_B(\mathrm{t}) \\ i_C(\mathrm{t}) \end{bmatrix} = \begin{bmatrix} I_o \cos(\omega_o t - \phi_o) \\ I_o \cos(\omega_o t - 2\pi/3 - \phi_o) \\ I_o \cos(\omega_o t - 4\pi/3 - \phi_o) \end{bmatrix} \tag{2.19}$$

The modulation indexes m_{kj} represent the duty cycle of each switch within a switching period, such that the relations in (2.20) and (2.21) are fulfilled.

$$\begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} = \begin{bmatrix} m_{11}(t) & m_{12}(t) & m_{13}(t) \\ m_{21}(t) & m_{22}(t) & m_{23}(t) \\ m_{31}(t) & m_{32}(t) & m_{33}(t) \end{bmatrix} \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \tag{2.20}$$

$$\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} = \begin{bmatrix} m_{11}(t) & m_{21}(t) & m_{31}(t) \\ m_{12}(t) & m_{22}(t) & m_{32}(t) \\ m_{13}(t) & m_{23}(t) & m_{33}(t) \end{bmatrix} \begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} \tag{2.21}$$

Assuming a balanced load, the matrix converter input currents can be defined as per (2.22), where I_i is the input current amplitude and ϕ_i is the phase difference between the input voltage and current.

$$\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} = \begin{bmatrix} I_i \cos(\omega_i t - \phi_i) \\ I_i \cos(\omega_i t - 2\pi/3 - \phi_i) \\ I_i \cos(\omega_i t - 4\pi/3 - \phi_i) \end{bmatrix} \tag{2.22}$$

The optimal Venturini-Alesina modulation method in [67] defined the target output voltages, $\begin{bmatrix} v_A(t) & v_B(t) & v_C(t) \end{bmatrix}$, as a combination of a sinusoidal at the fundamental output angular frequency, ω_o, with contributions of the third harmonics from the fundamental input frequency, ω_i, and the third harmonic of the output fundamental frequency as per (2.23) where V_o is the target output voltage amplitude. Defining the target output voltages, including third-order harmonics, allows for a converter gain of $\sqrt{3}/2$, whereas the definition of the output voltages considering only the fundamental lead to a maximum voltage gain of $1/2$.

$$\begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} = \begin{bmatrix} V_o \cos(\omega_o t) + \frac{1}{4} V_I \cos(3\omega_i t) - \frac{1}{6} V_o \cos(3\omega_o t) \\ V_o \cos(\omega_o t - 2\pi/3) + \frac{1}{4} V_I \cos(3\omega_i t) - \frac{1}{6} V_o \cos(3\omega_o t) \\ V_o \cos(\omega_o t - 4\pi/3) + \frac{1}{4} V_I \cos(3\omega_i t) - \frac{1}{6} V_o \cos(3\omega_o t) \end{bmatrix} \tag{2.23}$$

Under these conditions, the modulation indexes for each S_{jk} switch can be given by (2.24) implemented as suggested in [73].

$$m_{kj}(t)=\frac{1}{3}+\frac{1}{3}\frac{V_o}{V_i}\left\{\begin{array}{l}\left(1-\frac{\tan\phi_i}{\tan\phi_o}\right)\cos\left(\omega_o t+\omega_i t-\frac{\left(2(k+j)-4\right)\pi}{3}\right)+\\+\left(1+\frac{\tan\phi_i}{\tan\phi_o}\right)\cos\left(\omega_o t-\omega_i t-\frac{2(k+j)\pi}{3}\right)+\\-\frac{1}{6}\left(1-\left|\frac{\tan\phi_i}{\tan\phi_o}\right|\right)\cos\left(3\omega_o t+\omega_i t-\frac{2(j-1)\pi}{3}\right)+\\-\frac{1}{6}\left(1-\left|\frac{\tan\phi_i}{\tan\phi_o}\right|\right)\cos\left(3\omega_o t-\omega_i t-\frac{2(1-j)\pi}{3}\right)+\\-\frac{1}{6\sqrt{3}}\left|\left(1-\left|\frac{\tan\phi_i}{\tan\phi_o}\right|\right)\right|\cos\left(4\omega_i t-\frac{2(j-1)\pi}{3}\right)+\\+\frac{7}{6\sqrt{3}}\left|\left(1-\left|\frac{\tan\phi_i}{\tan\phi_o}\right|\right)\right|\cos\left(2\omega_i t-\frac{2(1-j)\pi}{3}\right)\end{array}\right\} \tag{2.24}$$

Venturini-Alesina Modulation in 3×4 DMC

When using a 3×4 DMC, the target output voltages also need to account for the target voltage for the neutral line as per (2.25).

$$\begin{bmatrix}v_A(t)\\v_B(t)\\v_C(t)\\v_N(t)\end{bmatrix}=\begin{bmatrix}V_o\cos(\omega_o t)+\frac{1}{4}V_I\cos(3\omega_i t)-\frac{1}{6}V_o\cos(3\omega_o t)\\V_o\cos(\omega_o t-2\pi/3)+\frac{1}{4}V_I\cos(3\omega_i t)-\frac{1}{6}V_o\cos(3\omega_o t)\\V_o\cos(\omega_o t-4\pi/3)+\frac{1}{4}V_I\cos(3\omega_i t)-\frac{1}{6}V_o\cos(3\omega_o t)\\\frac{1}{4}V_I\cos(3\omega_i t)-\frac{1}{6}V_o\cos(3\omega_o t)\end{bmatrix} \tag{2.25}$$

Unlike the assumptions taken for the 3×3 DMC modulation, the input and output currents can be unbalanced. A set of simplified modulation indexes, assuming unity power factor and using the instantaneous measurement of the input and output filtered voltages of the converter, is written in (2.26), where $v_k(t)$ is the input filtered voltage in phase *k* and $v_j(t)$ is the output filtered voltage in phase *j* [74].

$$m_{kj}(t)=\frac{1}{3}\left[1+\frac{2v_k(t)v_j(t)}{V_i^2}+\frac{4\sqrt{3}}{9}\frac{V_o}{V_i}\sin\left(\omega_i t+(j-1)\frac{2\pi}{3}\right)\sin(3\omega_i t)\right] \tag{2.26}$$

Assuming a sufficiently small imbalance in the currents, the results obtained for the 3×3 DMC modulation can be adapted to allow the control of the input power factor and handle

unbalanced output currents at the cost of harmonic distortion in the input currents. Therefore, the modulation indexes of switches with index $j \in \{1,2,3\}$, $k \in \{1,2,3\}$ can still be given by (2.24), while the neutral branch switches modulation indexes m_{41}, m_{42} and m_{43}, are given by (2.27).

$$m_{4j}(t) = \frac{1}{3} + \frac{1}{3}\frac{V_o}{V_i}\left\{\begin{array}{l} -\frac{1}{6}\left(1-\left|\frac{\tan\phi_i}{\tan\phi_o}\right|\right)\cos\left(3\omega_o t + \omega_i t - \frac{2(j-1)\pi}{3}\right) + \\ -\frac{1}{6}\left(1-\left|\frac{\tan\phi_i}{\tan\phi_o}\right|\right)\cos\left(3\omega_o t - \omega_i t - \frac{2(1-j)\pi}{3}\right) + \\ -\frac{1}{6\sqrt{3}}\left|\left(1-\left|\frac{\tan\phi_i}{\tan\phi_o}\right|\right)\right|\cos\left(4\omega_i t - \frac{2(j-1)\pi}{3}\right) + \\ +\frac{7}{6\sqrt{3}}\left|\left(1-\left|\frac{\tan\phi_i}{\tan\phi_o}\right|\right)\right|\cos\left(2\omega_i t - \frac{2(1-j)\pi}{3}\right) \end{array}\right\} \quad (2.27)$$

Finite Control Set Model Predictive Control

MPC is considered one of the most prominent techniques for controlling matrix converters. Even though this control technique has been used since the late 1970s [75], its applications on power converters only started to mainstream at the turn of the century. The basis of the MPC technique uses a dynamic model of the system to predict the future states of the controlled plant. Such predictions are then evaluated to select the control action, minimising a suitable cost function.

One of the significant drawbacks of MPC is the required computation power [76]. Complex discretised model dynamics combined with multiple predictions to be computed in real time can easily lead to unfeasible computation times. However, with increasing computation power available at exponentially decreasing cost has somewhat shadowed this problem.

Despite the abovementioned drawbacks, MPC presents significant advantages when compared to linear controllers. Since the system dynamics are predicted, the errors are minimised even before they arise; ultimately, if all system dynamics were perfectly modelled, the MPC controller would yield the optimum control law.

For the control of switching power converters, it is typical to consider a finite control set; this is, predictions are made for all the available converter states [69]. A different technique is to consider a continuous control set and then use a modulation method to emulate such continuity. The second method yields a constant switching frequency, while the first method does not. Even though similar results can be attained with either method, the use of the finite

control set can result in slightly better dynamic performance [77] and lower THDs [78]. Therefore, the hereafter description will focus on the finite control set predictive control.

Assuming the set of possible control actions as S_i where $i = 1, \dots, n$ are the n available converter states (control set) and a system dynamics describing function f_p that based on the current system state variables, $x(t_k)$, and the current converter state (control action), S_i, allows to predict the next system state variables $x(t_{k+1})_i$ the relation (2.28) can be obtained. [3]

$$x\left(t_{k+1}\right)_i = f_p\left(x\left(t_k\right), S_i\right) \tag{2.28}$$

It is then possible, for n finite control set, to predict the future system state variables for all the available control actions. To select the best control action S_i of the control set, a cost functional, g, must be defined and evaluated for all control actions. The function g can tackle multiple control objectives. In the case of matrix converters, the objectives are usually the tracking of both the output and input current references. Generally, g will be a functional of the reference state and the system state but can also include more complex dynamics that can be directly a functional of the control action, f_s (e.g. minimising switching losses).

$$\min g\left(x(t), f_p\left(x\left(t_k\right), S_i\right), f_s(S_i), \dots\right) \quad i \in \{1, \dots, \mathrm{n}\} \tag{2.29}$$

At a first glance it might look like we can directly compute each state at t_{k+1}, however in practice both acquisitions and computations take non negligible time. To overcome this issue the horizon of the prediction is advanced by one sampling period. To illustrate this strategy take as an example the situation in Figure 2.13, where the current measurements $x(t_k)$ combined with the current control action S_2 are used to estimate $x(t_{k+1})$. The control action selects state S_2 at t_{k-1} and as such the control action that minimizes $g(t_{k+2})$ is selected at t_k which will be applied in the converter at t_{k+1}.

[3] When the "next" system state variables are mentioned, they assume that the system model dynamics has been discretized with a given time sample T_s therefore to ease the nomenclature $x(t_{k+1})$ refers in reality to $x(t + T_s)$

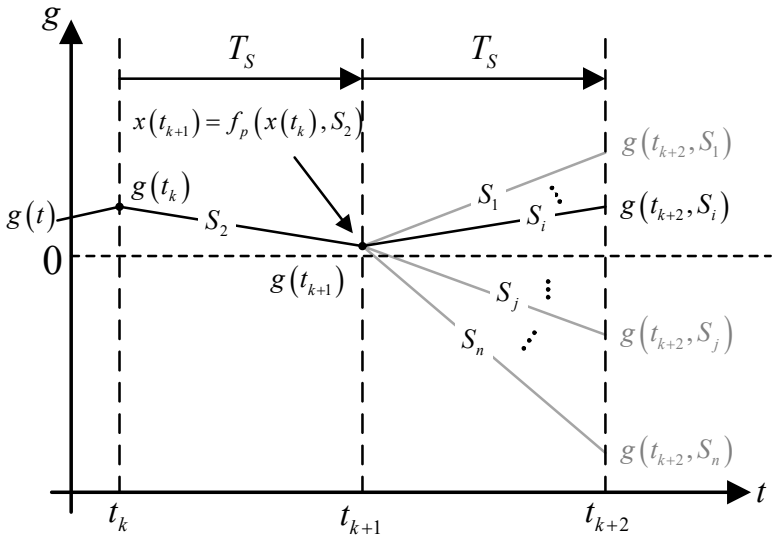


Figure 2.13 Depiction of MPC cost function behaviour over time, with a representation of the computation of all possible control actions at t_{k+1} with their respective predicted impact on the cost function.

The calculation horizon can be further extended beyond t_{k+2} by computing the cost function for all possible combinations up to the event horizon. For the case of a 3×4 matrix converter (which has 79 possible different states), the prediction, f_p, must be computed 80 times to predict until t_{k+2} and it must be computed 6242 times to predict until t_{k+3}. Generally, f_p must be computed n^{t_p} times, where n is the number of different control actions, and t_p is the number of time steps beyond t_{k+1} the MPC will compute. In practice, this leads to unbearable computation times and as such, for most applications $t_p = 1$.

To facilitate comprehension of the method hereafter follows an example of an MPC controller which controls simultaneously the output currents and the input power factor for a 3×4 matrix converter with a second order input filter and an inductive RL load, as per Figure 2.14

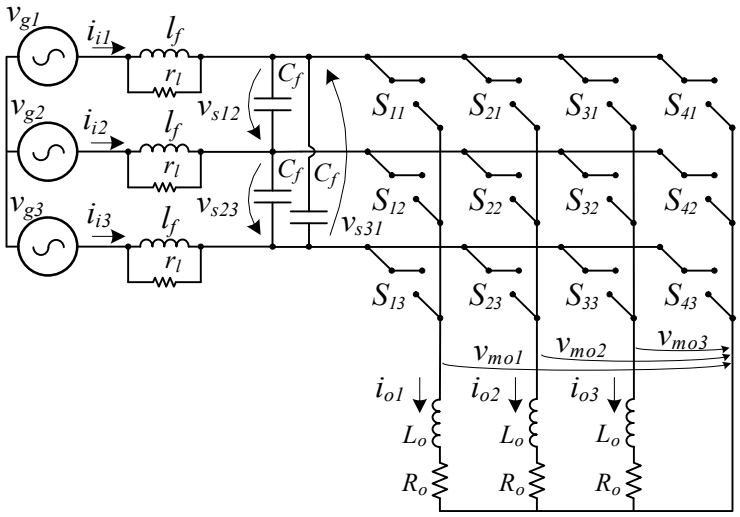


Figure 2.14 Depiction of a 3×4 DMC with a second order input filter supplying an RL load.

The first step to implement the MPC controller is to describe the system dynamics at the input filter and at the output load. Suppose the input and output frequencies are assumed to be equal. In that case, it is beneficial to describe the system dynamics in a *dq0* reference frame synchronous with the input grid voltage (a description of the necessary transforms can be found in Appendix B). The dynamics of the input filter inductor currents can be obtained by the voltage law across the loop formed with the grid voltage and the inductor and capacitor voltages and is given by (2.30).

$$\begin{bmatrix} \frac{di_{Lfd}}{dt} \\ \frac{di_{Lfq}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix} \begin{bmatrix} i_{Lfd} \\ i_{Lfq} \end{bmatrix} + \begin{bmatrix} -\frac{1}{2L_f} & -\frac{\sqrt{3}}{6L_f} \\ \frac{\sqrt{3}}{6L_f} & -\frac{1}{2L_f} \end{bmatrix} \begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} + \frac{1}{L_f} \begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix} \tag{2.30}$$

Notice that the *0* component is omitted since the input is a three-phase system without neutral this component is equal to zero.

The grid currents i_{id} and i_{iq} differ from the inductor currents since the damping resistor of the filter is placed in parallel with the inductor, this is detailed in (2.31).

$$\begin{bmatrix} \frac{di_{Lfd}}{dt} \\ \frac{di_{Lfq}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix} \begin{bmatrix} i_{Lfd} \\ i_{Lfq} \end{bmatrix} + -\frac{r_l}{L_f} \begin{bmatrix} i_{Lfd} \\ i_{Lfq} \end{bmatrix} + \frac{r_l}{L_f} \begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix} \tag{2.31}$$

The summation of the currents at the input of the matrix converter node yields the dynamics of the input filter capacitor voltages v_{sd} and v_{sq}, as per (2.32).

$$\begin{bmatrix} \frac{dv_{sd}}{dt} \\ \frac{dv_{sq}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix} \begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} + \begin{bmatrix} \frac{1}{2C_f} & -\frac{\sqrt{3}}{6C_f} \\ \frac{\sqrt{3}}{6C_f} & \frac{1}{2C_f} \end{bmatrix} \begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix} + \begin{bmatrix} -\frac{1}{2C_f} & \frac{\sqrt{3}}{6C_f} \\ -\frac{\sqrt{3}}{6C_f} & -\frac{1}{2C_f} \end{bmatrix} \begin{bmatrix} i_{mid} \\ i_{miq} \end{bmatrix} \quad (2.32)$$

With a simple RL load at the output, the dynamics of the output current can be obtained by applying the voltage laws across each output phase and neutral, as is shown in (2.33).

$$\begin{bmatrix} \frac{di_{od}}{dt} \\ \frac{di_{oq}}{dt} \\ \frac{di_{o0}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_o}{L_o} & \omega & 0 \\ -\omega & -\frac{r_o}{L_o} & 0 \\ 0 & 0 & -\frac{r_o}{L_o} \end{bmatrix} \begin{bmatrix} i_{od} \\ i_{oq} \\ i_{o0} \end{bmatrix} + \frac{1}{L_o} \begin{bmatrix} v_{md} \\ v_{mq} \\ v_{m0} \end{bmatrix} \quad (2.33)$$

To compute the predictions in real-time, it is necessary to discretise the obtained continuous dynamics. Naturally, there are multiple methods to obtain a discretised set of equations. Euler's forward and backwards methods are two of the most common discretisation methods. The Euler forward method is an explicit method, while the Euler backwards is an implicit method (which results in higher computation effort). Euler's backward method offers unconditional stability [79] and is therefore chosen for this example. Assuming a discretisation time sample T_s the prediction for the input currents i_d and i_q can be obtained (after some algebraic manipulation) via (2.34). Notice that this prediction depends on the state of the grid voltages at t_{k+1}, which for sufficiently small T_s and considering they are represented in a *dq* frame can be assumed to be approximately equal to the current grid voltages $v_{gd}(k+1) \approx v_{gd}(k)$.

$$\begin{aligned} \begin{bmatrix} i_{id}(k+1) \\ i_{iq}(k+1) \end{bmatrix} = & \frac{3L_fC_fR_f}{3L_fC_fR_f + L_fT_s + R_fT_s^2} \begin{bmatrix} i_{id}(k) \\ i_{iq}(k) \end{bmatrix} + \frac{(L_f + R_fT_s)T_s}{3L_fC_fR_f + L_fT_s + R_fT_s^2} \begin{bmatrix} i_{mid}(k+1) \\ i_{miq}(k+1) \end{bmatrix} + \\ & + \frac{3C_f(L_f + R_fT_s)}{3L_fC_fR_f + L_fT_s + R_fT_s^2} \begin{bmatrix} v_{gd}(k+1) \\ v_{gq}(k+1) \end{bmatrix} - \frac{3L_fC_f}{3L_fC_fR_f + L_fT_s + R_fT_s^2} \begin{bmatrix} v_{gd}(k) \\ v_{gq}(k) \end{bmatrix} + \\ & - \begin{bmatrix} -\frac{3C_fR_fT_s}{6L_fC_fR_f + 2L_fT_s + 2R_fT_s^2} & -\frac{\sqrt{3}C_fR_fT_s}{6L_fC_fR_f + 2L_fT_s + 2R_fT_s^2} \\ \frac{\sqrt{3}C_fR_fT_s}{6L_fC_fR_f + 2L_fT_s + 2R_fT_s^2} & -\frac{3C_fR_fT_s}{6L_fC_fR_f + 2L_fT_s + 2R_fT_s^2} \end{bmatrix} \begin{bmatrix} v_{sd}(k) \\ v_{sq}(k) \end{bmatrix} \end{aligned} \quad (2.34)$$

A similar approach yields the prediction equations for the output current as shown in (2.35).

$$\begin{bmatrix} i_{od}(k+1) \\ i_{oq}(k+1) \\ i_{o0}(k+1) \end{bmatrix} = \frac{L_o}{L_o + T_s R_o} \begin{bmatrix} i_{od}(k) \\ i_{oq}(k) \\ i_{o0}(k) \end{bmatrix} + \frac{1}{L_o + T_s R_o} \begin{bmatrix} v_{md}(k+1) \\ v_{mq}(k+1) \\ v_{m0}(k+1) \end{bmatrix} \quad (2.35)$$

The prediction of the output currents i_{od}, i_{oq} and i_{o0} combined with reference values for these currents i_{od}^*, i_{oq}^* and i_{o0}^* will serve to track the output currents. Since the power at the input and output of the matrix converter must be equal[4], the only degree of freedom left to control the input currents is the reactive power that can be computed from (2.36).

$$Q_g = v_{gd} i_{iq} - v_{gq} i_{id} \quad (2.36)$$

Notice that in each prediction equation there is a term that depends on the matrix converter instantaneous state: the currents in (2.34), $i_{mid}(k+1)$ and $i_{miq}(k+1)$; and the voltages in (2.35), $v_{md}(k+1)$, $v_{mq}(k+1)$, $v_{m0}(k+1)$. Both equations can now be computed for each possible state of the matrix converter (shown in tables A.1 and A.2 of the Appendix A) and for each outcome the cost function of (2.37) is evaluated to select the state that minimizes this function after all control actions have been predicted.

$$g = \frac{w_1}{S_{nom}^2}(Q^* - Q)^2 + \frac{1}{I_{nom}^2}\left[w_2 \left(i_{od}^* - i_{od}\right)^2 + w_3 \left(i_{oq}^* - i_{oq}\right)^2 + w_4 \left(i_{o0}^* - i_{o0}\right)^2 \right] \quad (2.37)$$

2.3 Modern Power Semiconductor Technologies

Power semiconductor devices are the building blocks of power converters. For efficiency reasons, power semiconductor devices are operated as switches, connecting (*on* state) or disconnecting (off state) converter sub-circuits at switching frequencies in the range of kHz to MHz. The control of this *on* or *off* state can be driven by the circuit main voltages/currents, as in diodes, or it can be forced, as it happens on field effect or bipolar transistors, or it can even be a combination of both, such as in thyristors which can be triggered to a conducting state but can only return to a non-conducting state after the voltage across the device is reversed or the anode current is zeroed.

[4] It is usual to disregard the converter power losses in order to establish the control equations, this obviously implies that the converter efficiencies are sufficiently high for such approximation to hold.

With the invention of the Isolated Gate Bipolar Transistors (IGBTs) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET), there was a significant revolution in power electronics which powered innovations across a wide range of sectors, from the automotive sector to industry automation and even telecommunications. They allowed the implementation of DC/DC, DC/AC, AC/DC and AC/AC converters with higher efficiencies and desirable power densities [80].

For most of the time, these devices were manufactured using Silicon (Si). However, increasing demands of power density, operating temperature, and blocking voltage of the semiconductors have motivated investment in producing transistors with different materials such as Silicon Carbide (SiC), Gallium Nitride (GaN) and Gallium Oxide (Ga_2O_3). Hereafter, the reader will find a comparison between these materials that highlights their relevant differences for the development of power transistors and diodes.

2.3.1 Modern Power Semiconductor Materials

The performance of power semiconductor devices is directly related to their physical properties. The Baliga figure-of-merit *BFOM* [81], proposed in 1982, defines according to the material properties a figure-of-merit that relates to the conduction losses of a given semiconductor:

$$BFOM = \varepsilon_S \mu_n E_G^3 \tag{2.38}$$

Where ε_S, μ_n and E_G are the permittivity, the electron mobility and the bandgap of the semiconductor material. Wideband-gap semiconductors use materials with bandgaps (>3 eV) higher than that of Si (typically in the range of 1-1.5 eV) that, as a result, have higher critical electrical fields, which, according to (2.38) would lead to lower conduction losses compared to a power device built with Si for the same breakdown voltage. This result is somewhat intuitive since the wideband-gap semiconductor can be built with a lower thickness (assuming a vertically built semiconductor) to withstand the same voltage.

Baliga also concluded in a later work that, in high-frequency applications, the higher the critical electrical field and the electron mobility of the semiconductor, the lower the switching losses for the same operating voltage [81].

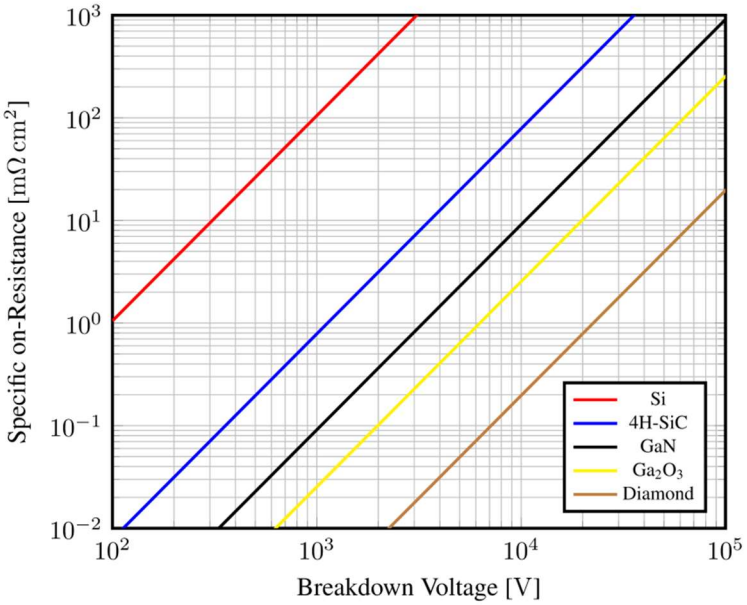


Figure 2.15 Relation between the breakdown voltage and the specific on-Resistance for semiconductors made with Si, 4H-SiC, GaN, GA_2O_3 and Diamond.

Figure 2.15 shows the contours of the relation between the breakdown voltage and the specific on-state resistance considering (2.39) where R_{on-} is the specific on-state resistance and V_{BK} is the breakdown voltage.

$$BFOM = V_{BK}^2 / R_{ON-SP} \tag{2.39}$$

Furthermore, some wide-band materials show considerably higher thermal conductivity. This is particularly advantageous since it allows operating with higher admissible losses without exceeding temperature limits or even at the same power point with a lower operating temperature.

Table 2.2 Properties of Si and wide-bandgap materials.

Material/Property	Si	4H-SiC	GaN	Ga_2O_3	Diamond
Band Gap [eV]	1.1	3.2	3.4	4.9	5.5
Critical Field [10^6 V·cm^{-1}]	0.3	2	3.3	8	10
Relative Electric Permittivity	11.8	10	8.9	16.3	5.5
Majority carrier Mobility [cm^{2}V^{-1}s^{-1}]	1350	720	370	1300	1900
Thermal Conductivity [W·m^{-1}·K^{-1}]	149	370	130	15	2290

Table 2.2 shows a set of properties of different materials used to develop semiconductors. Notice that the bandgap and the critical electrical field of the represented materials are substantially higher than those of Si. The thermal conductivity of SiC and Diamond is also significantly higher than Si, facilitating the thermal management design. Lastly, notice that the electron mobility of GaN is higher than that of both Si and SiC. In the future, diamond properties may turn it into the material of choice for high-voltage, high-power semiconductors.

2.3.2 Modern Power Semiconductor Devices

Even though most of the commercially available semiconductor devices for power electronics are still manufactured using Si, some particular devices are already being manufactured on a large scale using wide-bandgap materials.

The first wide-bandgap devices produced on a large scale were SiC Schottky diodes, widely used to replace the anti-parallel Si diode in Si IGBT modules. SiC MOSFETs, fuelled by the increasing demand in the EV sector, also began large-scale production in around 2015 and are currently widespread across a wide range of applications. The development of SiC IGBT promises unprecedented blocking voltages for a single device. Some manufacturers, such as Hitachi, claim mass production of SiC IGBTs will start in late 2024.

Gallium Nitride power semiconductor devices are also widely available as of 2021; the first available devices were depletion-mode devices, which are inherently “normally-on” devices. They were sold with a cascaded LV Si MOSFET to form a “normally-off” device at the added cost of a second semiconductor in the current path. More recently, manufacturers have begun the mass production of enhancement mode GaN devices, which are inherently “normally-off” devices as is desired in most applications [82].

The following subsections will provide some details on the above-described devices concerning operating voltages and power ranges.

Silicon Carbide Diodes

SiC Diodes for power electronics applications are mostly manufactured as Schottky diodes and PiN diodes. SiC Schottky diodes are currently manufactured and commercially available with a maximum blocking voltage of 3300 V, while SiC PiN diodes are manufactured for up to 15 kV of maximum blocking voltage. The blocking voltage of SiC Schottky devices tested in academia goes as high as 10kV [83] and as high as 30 kV for SiC Pin Diodes [84,85].

Despite the commercial availability of PiN diodes, the most common SiC diodes by far are Schottky barrier diodes (SBD), which are now widely used as anti-parallel diodes to IGBT modules. Si SBD was used in power applications up to 200 V mainly due to their fast recovery time compared to other diodes; SiC enabled the same fast recovery time, but in voltages up to 3300 V. Still, SiC SBDs with blocking voltages of up to 1700 V are more common.

Silicon Carbide Metal Oxide Semiconductor Field Effect Transistor

For the same voltage level, MOSFETs offer lower switching losses than IGBT counterparts; this means they enable the use of converters at a higher switching frequency, reducing filtering requirements and, therefore, increasing power density.

Despite the advantages in switching losses, Si MOSFETs are only advantageous for ratings up to 600 V. Therefore, applications that require higher blocking voltages would default to Si IGBTs. With the now widespread commercial availability of 1700 V SiC MOSFETs, several applications ranging from motor drives to grid-connected converters are now using these devices [86,87].

Besides the higher blocking voltages, SiC MOSFETs also have the additional benefit of high thermal conductivity, which eases the cooling requirements.

Silicon Carbide Insulated Gate Bipolar Transistor

IGBTs share the high current density of bipolar transistors with the high input impedance of MOSFETs, which made them, for the past years, the reigning power semiconductor for high-power converters. The first SiC IGBT was fabricated in 1996 [88], but as of yet, commercially available devices have yet to be manufactured.

With the increasing interest in MV and HV converters for applications such as FACTs or HVDCs, so is increasing the interest in semiconductor devices that can withstand higher voltages. SiC IGBT devices promise such breakthroughs, with 20kV devices already being laboratory-tested in switched power converters [89].

The mass fabrication of SiC IGBTs is still immature and expected to improve over the next few years. Nonetheless, the current reported devices show excellent performance for switched power converters with prospects of challenging SiC MOSFETs for higher voltage levels (>3.3kV) and enabling new paradigms in MV and HV converters [90].

Gallium Nitride High Electron Mobility Transistor (HEMT)

Instead of a doped region, HEMT uses a junction composed of materials with different band gaps, hence the also common name of HFET (Heterojunction Field Effect Transistor). This junction forms a 2-dimensional electron gas, which results in high electron mobility [91].

GaN HEMT normally-off devices are already available in the market with breakdown voltages up to 650V. The main advantage of these devices is the reduced switching losses, even when compared with SiC MOSFET [92]. The main drawback comes from the reduced thermal conductivity of GaN, which might involve more challenging cooling designs.

In 2019, researchers at Panasonic presented a dual gate bidirectional GaN HMET whose channel can conduct and block in both directions in a controlled way. These devices can switch extremely fast with low switching losses and the benefit of only having one channel conducting all the current, thus achieving a single-device bidirectional switch [19,93]. The characteristics of such devices are particularly attractive for matrix converters and can potentially be the required breakthrough for the industrial penetration of matrix converters [94].

Gallium Oxide Field Effect Transistor

As apparent by Figure 2.15, Ga_2O_3, more specifically β-Ga_2O_3, is a promising material to make semiconductor devices that can switch under high voltages given its attainable critical field strength of 8 MV/cm [95]. Consequently, Ga_2O_3 devices could highly increase the voltage capabilities of matrix converters.

Power device structures for Ga_2O_3 MOSFETs have been demonstrated to be feasible [96], with several authors classifying them as one of the most promising wide-bandgap semiconductor technologies. Nonetheless, several challenges need to be met before commercial devices are available.

The major downside of Ga_2O_3 is the reduced thermal conductivity of this material, which is even lower than that of Si, which in turn results in more demanding cooling requirements, which can decrease the overall power density of the power converter.

Chapter 3

MATRIX CONVERTER BASED SOLID STATE TRANSFORMER

The proposed SST topology aims to replace a traditional distribution transformer, offering higher degrees of controllability along with an increase in specific power and power density. Consider the novel SST topology of Figure 3.1, which is composed of two DMCs interfacing an MFT between an MV three-phase grid and an LV three-phase grid with neutral.

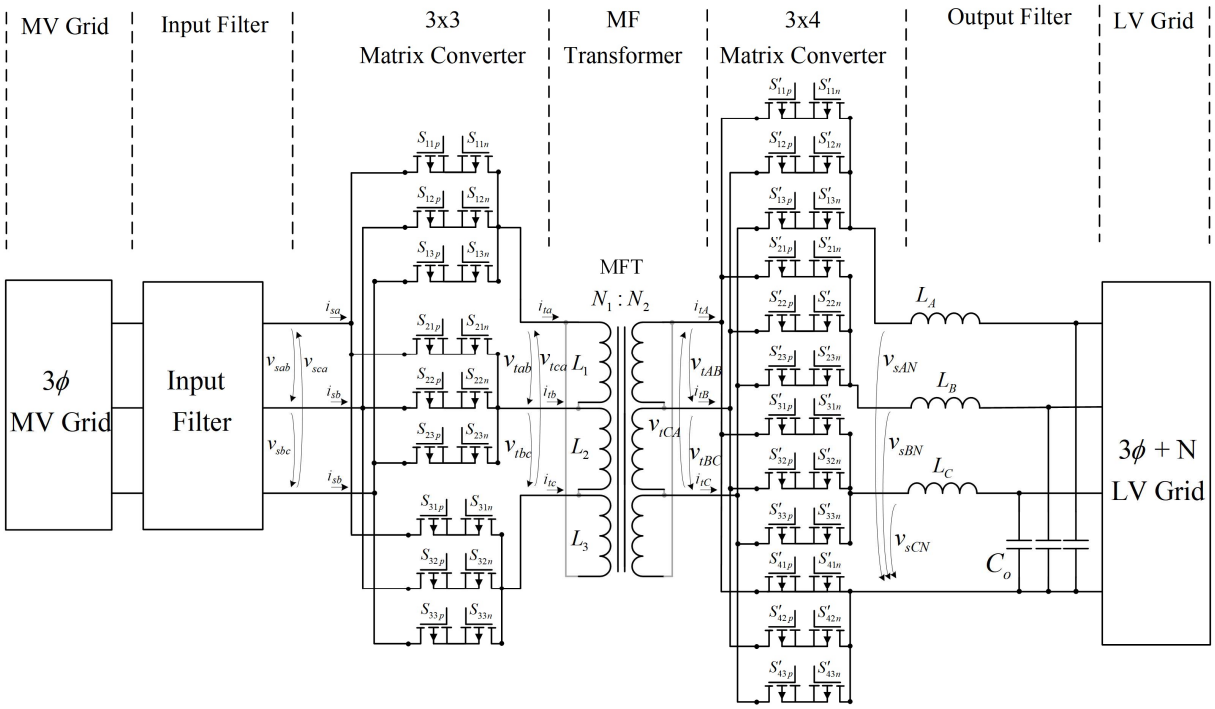


Figure 3.1 Schematization of the proposed SST topology composed of a MF transformer that interface a three-phase grid whitout neutral with a three-phase grid with neutral via DMCs.

This topology combines the power density advantages of matrix converters and a single three-phase MF transformer. As a consequence of the expected future developments in power semiconductors, the primary side converter can use switches that can withstand voltages in the range of MV levels used in distribution grids [97]. The secondary side converter is to be operated in grid-forming mode, where the converter controls the grid voltage, while the primary side converter works in grid-connected mode, where the converter consumes/injects currents from/into the grid by synchronising with the grid voltages.

This chapter focuses on three main novel contributions: First is the proposal of the above-shown high-power density topology; Second is a modulation method that considers the input 3x3 DMC, the output 3x4 DMC and the isolation transformer as a single 3x4 DMC. By doing so, the control action of traditional control methodologies can be unfolded into both converters while the flux on the transformer remains outside of the saturation region. Ultimately, this means that the SST can be abstracted as a single converter for the controller design, enabling previously established control methodologies to be directly employed in the SST. Third is a commutation method that deals with the leakage inductance of the transformer. Without it, the traditional commutation methods would not recirculate the leakage energies, leading to severe overvoltages that can potentially damage the semiconductors.

3.1 A Novel Modulation Method for Transformer Flux Minimization

3.1.1 SST Modelling as a single matrix converter

The matrix converters of Figure 3.1 can be modeled by the matrices $\mathbf{S}$ and $\mathbf{S}'$ from (2.8) and (2.15) for the primary side and secondary side matrix converters, respectively. Assuming that the MF transformer is ideal and characterized by the turns ratio $r_t = N_1/N_2$ where N_1 and N_2 are the number of turns of the primary and secondary coils, the relation between the input phase voltages of the primary side matrix converter, $\boldsymbol{V_s}$ and the output phase voltages of the secondary matrix converter, $\boldsymbol{V_m}$, is given by (3.1)

$$\mathbf{v_m} = r_t(\mathbf{S}' \cdot \mathbf{S})\mathbf{v_s} \tag{3.1}$$

Where $\mathbf{v_m} = \begin{bmatrix} v_{mA} & v_{mB} & v_{mC} & v_{mN} \end{bmatrix}^T$ and $\mathbf{v_s} = \begin{bmatrix} v_{sa} & v_{sb} & v_{sc} \end{bmatrix}^T$ are the phase voltages referenced to the virtual input neutral. The product of matrices $\mathbf{S}'$ and $\mathbf{S}$ is given by (3.2) and is hereby referred as $\boldsymbol{\chi}$.

$$\boldsymbol{\chi} = \mathbf{S}' \cdot \mathbf{S} = \begin{pmatrix} s_{11}s'_{11} + s_{21}s'_{12} + s_{31}s'_{13} & s_{12}s'_{11} + s_{22}s'_{12} + s_{32}s'_{13} & s_{13}s'_{11} + s_{23}s'_{12} + s_{33}s'_{13} \\ s_{11}s'_{21} + s_{21}s'_{22} + s_{31}s'_{23} & s_{12}s'_{21} + s_{22}s'_{22} + s_{32}s'_{23} & s_{13}s'_{21} + s_{23}s'_{22} + s_{33}s'_{23} \\ s_{11}s'_{31} + s_{21}s'_{32} + s_{31}s'_{33} & s_{12}s'_{31} + s_{22}s'_{32} + s_{32}s'_{33} & s_{13}s'_{31} + s_{23}s'_{32} + s_{33}s'_{33} \\ s_{11}s'_{41} + s_{21}s'_{42} + s_{31}s'_{43} & s_{12}s'_{41} + s_{22}s'_{42} + s_{32}s'_{43} & s_{13}s'_{41} + s_{23}s'_{42} + s_{33}s'_{43} \end{pmatrix} \tag{3.2}$$

Considering the topological constraints imposed by (2.9) and (2.16) in matrices $\mathbf{S}$ and $\mathbf{S}'$ while inspecting (3.2) it can be shown that $\boldsymbol{\chi}$ follows a similar set of constraints.

$$\sum_{j=1}^{3} \chi_{kj} = 1 \quad k \in \{1,2,3,4\} \tag{3.3}$$

The relation in (3.3) dictates that $\boldsymbol{\chi}$ has 81 different possible states similar to the number of possible states of $\mathbf{S}'$. That means that the 2187 possible combinations of the association of both matrix converters (27 states from the 3×3 DMC and 81 states of the 3×4 DMC) always result in one of the 81 possible states described in Tables A.1 and A.2 of Appendix A.

The proposed controller/modulator will make use of this property to enable the control of the SST as a single 3×4 DMC converter. As a consequence of this property, any 3×4 DMC converter state, obtained, for example, by the Venturini-Alesina modulation described in section 2.2.7, can then be unfolded into two states for each one of the primary and secondary matrix converters. Therefore, as depicted in Figure 3.2, these two matrix converters and the MF Transformer can be modelled by a single matrix converter as long as the transformer is considered ideal, with an additional voltage gain given by the turns ratio r_t.

The reason to consider the MF Transformer ideal is the main advantage brought by the simplicity of describing the system. The downside in the practical world will be the influence of parasitic elements, namely leakage and magnetising inductances, in the converter's currents. The main idea is that the influence of these elements can be mitigated by minimising the said parasitic components in the transformer design stage.

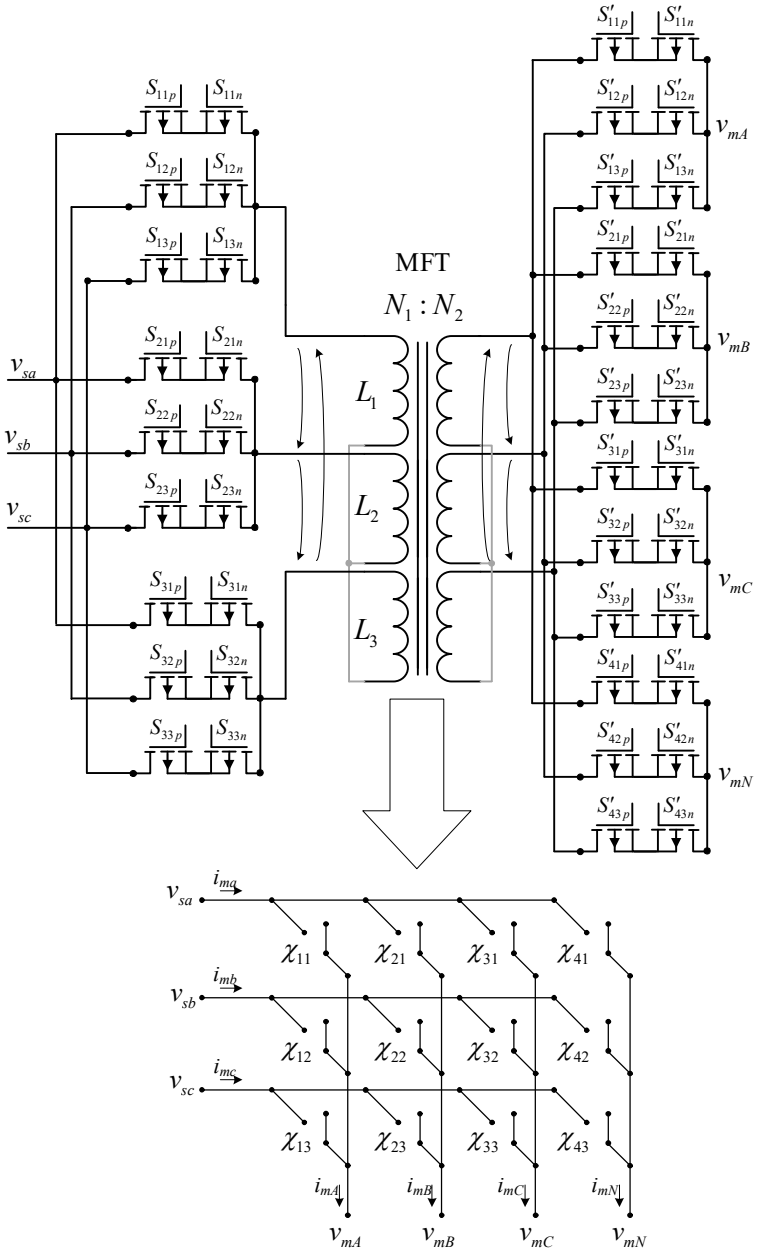


Figure 3.2 Depiction of the equivelant $\boldsymbol{\chi}$ DMC that models both primary and secondary converters along with an ideal transformer.

The input-output behaviour of both matrix converters and the MF Transformer can then be modelled by the matrix $\boldsymbol{\chi}$ according to the relation in (3.4) and (3.5), where $i_{mi} = \begin{bmatrix} i_{ma} & i_{mb} & i_{mc} \end{bmatrix}$ and $i_{mo} = \begin{bmatrix} i_{mA} & i_{mB} & i_{mC} & i_{mN} \end{bmatrix}$.

$$\mathbf{v}_m = \boldsymbol{\chi} r_t \mathbf{v}_s \tag{3.4}$$

$$\mathbf{i_{mi}} = \boldsymbol{\chi}^T r_t \mathbf{i_{mo}} \tag{3.5}$$

Figure 3.3 shows the number of possible combinations of matrices $\mathbf{S}'$ and $\mathbf{S}$ that can be used to achieve each of the 81 possible states of $\boldsymbol{\chi}$. Vectors 1 to 18 and 37 to 42 can each be obtained with 36 possible combinations of the states of $\mathbf{S}'$ and $\mathbf{S}$. Vectors 19 up to 36 can each be obtained with 30 possible combinations, while vectors 43 to 78 can be obtained by only 6 different possible combinations each. Finally, vectors 79 to 81, also called zero vectors since they have zero output voltage and zero amplitude input currents, can each be attained in 189 different possible ways.

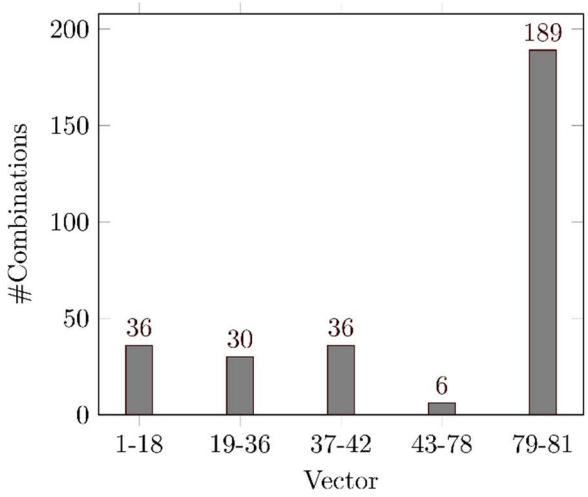


Figure 3.3 Representation of the number of possible combinations of the vectors of S and S' that result in a particular vector of the $\boldsymbol{\chi}$ equivalent converter. For example, vectors 1 to 18 and vectors 43 to 78 of $\boldsymbol{\chi}$ can each be attained in 36 combinations of S and S'.

With the considered assumptions for the MF Transformer, the SST can be represented by an input filter followed by a 3×4 DMC followed by an output filter. This model enables the use of any controller or modulation technique that is suitable for a 3×4 DMC to be used directly in the SST as long as the selected converter state can be appropriately unfolded for both matrix converters.

3.1.2 A Model Predictive Controller to minimise the transformer flux

The challenge now becomes how to unfold the state of the equivalent converter. The most straightforward approach to obtain the desired $\boldsymbol{\chi}$ state would be to set $\mathbf{S}$ to the identity matrix resulting in $\mathbf{S}'$ being identical to $\boldsymbol{\chi}$, (3.6).

$$\boldsymbol{\chi} = \mathbf{S}' \cdot \mathbf{S} = \mathbf{S}' \cdot \mathbf{I} = \mathbf{S}' \tag{3.6}$$

It is, however, unfortunate and evident that such an approach is not a suitable solution since LF voltages would be applied to the transformer, which would result in a transformer designed for MF to the saturation of the core's material. It becomes clear then that this approach requires unfolding each desired state so that the core saturation is avoided.

The electromotive force for the path formed by the coil k, neglecting resistive voltage drops, is simply the voltage across the coil k, v_k. Considering the flux per turn across coil k, ϕ_{fk}, and the number of turns n_k then the voltage v_k can be obtained by (3.7).

$$v_k = n_k \frac{d\phi_{fk}}{dx} \tag{3.7}$$

The resulting flux per turn for a given voltage over a period T can then be obtained by (3.8) where ϕ_{fik} is the flux at the beginning of period T of coil k.

$$\phi_{fk} = \frac{1}{n_k}\int_T v_k dt + \phi_{fik} \tag{3.8}$$

It is important to note that (3.8) is only valid as long as some linearity of the magnetic material is assumed (i.e. the material is operating in the linear region of the BH curve and no saturation is considered).

Under this set of circumstances, (3.8) provides a suitable criteria to unfold the vectors of $\boldsymbol{\chi}$ by minimising the integral of the voltages across the coils. In the case of single-phase transformers, the problem becomes the minimisation of each transformer's flux. However, for a three-phase transformer, where the sum of the three fluxes equates to almost zero, minimising three fluxes is redundant. It then becomes helpful to use an $\alpha\beta$ reference frame.

The voltages applied to the three-phase MF transformer can be obtained from the voltages of the input capacitors voltages $[v_{ab}\ v_{bc}\ v_{ca}]$ and the state of the primary side matrix converter using matrix $\mathbf{S}_{nl}$ from (2.13) given by (3.9) using Concordia's transform, as per Appendix B.1.1 (Notice that $\mathbf{S}_{ll}$ derives directly from $\mathbf{S}$ according to (2.14)).

$$\begin{bmatrix} v_{tab} \\ v_{tbc} \\ v_{tca} \end{bmatrix} = \mathbf{S}_{ll} \begin{bmatrix} v_{sab} \\ v_{sbc} \\ v_{sca} \end{bmatrix} \Rightarrow \mathbf{C}^T \begin{bmatrix} v_{tab} \\ v_{tbc} \\ v_{tca} \end{bmatrix} = \left(\mathbf{C}^T \mathbf{S}_{ll} \mathbf{C}\right) \mathbf{C}^T \begin{bmatrix} v_{sab} \\ v_{sbc} \\ v_{sca} \end{bmatrix} \Rightarrow \begin{bmatrix} v_{t\alpha} \\ v_{t\beta} \end{bmatrix} = \left(\mathbf{C}^T \mathbf{S}_{ll} \mathbf{C}\right) \begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} \tag{3.9}$$

The flux in an $\alpha\beta$ reference is then given by (3.10).

$$\begin{cases} \phi_{f\alpha} = \dfrac{1}{n_k}\int_T v_{t\alpha}dt + \phi_{\alpha i} \\ \phi_{f\beta} = \dfrac{1}{n_k}\int_T v_{t\beta}dt + \phi_{\beta i} \end{cases} \tag{3.10}$$

Assuming that the input capacitor's voltage dynamics is slow compared to a given sampling period T_S (i.e., $v_{s\alpha}(t_k) \approx v_{s\alpha}(t_{k+1})$ and $v_{s\beta}(t_k) \approx v_{s\beta}(t_{k+1})$), then the transformer voltages can be written as per (3.11).

$$\begin{bmatrix} v_{t\alpha}(t_{k+1}) \\ v_{t\beta}(t_{k+1}) \end{bmatrix} = \left(\mathbf{C}^T\mathbf{S}_{ll}(t_{k+1})\mathbf{C}\right)\begin{bmatrix} v_{s\alpha}(t_k) \\ v_{s\beta}(t_k) \end{bmatrix} \tag{3.11}$$

Discretizing (3.10) with the sampling period T_s yields (3.12). Replacing the transformer's voltages of (3.11) in (3.12) the relation in (3.13) is obtained.

$$\begin{bmatrix} \phi_{f\alpha}(t_{k+1}) \\ \phi_{f\beta}(t_{k+1}) \end{bmatrix} = \begin{bmatrix} \phi_{fi\alpha} \\ \phi_{fi\beta} \end{bmatrix} + \frac{1}{n_k}T_s\begin{bmatrix} v_{t\alpha}(t_{k+1}) \\ v_{t\beta}(t_{k+1}) \end{bmatrix} \tag{3.12}$$

$$\begin{bmatrix} \phi_{f\alpha}(t_{k+1}) \\ \phi_{f\beta}(t_{k+1}) \end{bmatrix} = \begin{bmatrix} \phi_{fi\alpha} \\ \phi_{fi\beta} \end{bmatrix} + \frac{1}{n_k}T_s\left(\mathbf{C}^T\mathbf{S}_{ll}(t_{k+1})\mathbf{C}\right)\begin{bmatrix} v_{s\alpha}(t_k) \\ v_{s\beta}(t_k) \end{bmatrix} \tag{3.13}$$

The unfolding of the matrix $\boldsymbol{\chi}$ can then be stated as a minimisation problem of the $\alpha\beta$ components of the MF transformer's magnetic flux. This is stated in (3.14) by minimising the cost function g_f where $\boldsymbol{\chi}^*$ is the reference state for the equivalent converter which must be unfolded.

$$\begin{aligned} &\text{minimize } g_f = \phi_\alpha(t_{k+1})^2 + \phi_\beta(t_{k+1})^2 \\ &\text{subject to } \mathbf{S}'\cdot\mathbf{S} = \boldsymbol{\chi}^* \\ &\qquad\qquad \mathbf{S}' \in \{\mathbf{S}'_1, \mathbf{S}'_2 \cdots, \mathbf{S}'_{81}\} \\ &\qquad\qquad \mathbf{S} \in \{\mathbf{S}_1, \mathbf{S}_2 \cdots, \mathbf{S}_{27}\} \end{aligned} \tag{3.14}$$

Given that the subset of possible combinations of matrixes $\mathbf{S}'$ and $\mathbf{S}$ that satisfy $\boldsymbol{\chi}^*$ is sufficiently small, as is depicted in Figure 3.3, each outcome of the function g_f can be computed for each possible combination.

One of the advantages of this approach is that the function g_f can be adapted to include other objectives, e.g. reducing switching losses. However, to accommodate other objectives, it is helpful to normalise the objective function. Considering the magnetic core material cross-

section, A_c, and the core's magnetic flux density saturation, B_{max} a normalised version of g_{fn} is given by (3.15) where the term $\sqrt{6}/2$ derives from using a power invariant transformation on the $\alpha\beta$ components.

$$g_{fn} = \left(\frac{\sqrt{6}}{2B_{max}A_c} \phi_{f\alpha}\left(t_{k+1}\right) \right)^2 + \left(\frac{\sqrt{6}}{2B_{max}A_c} \phi_{f\beta}\left(t_{k+1}\right) \right)^2 \tag{3.15}$$

It is important to remark that $\phi_{f\alpha}\left(t_{k+1}\right)$ and $\phi_{f\beta}\left(t_{k+1}\right)$ depend on $\phi_{fi\alpha}$ and $\phi_{fi\beta}$. One possible way to obtain these fluxes is to integrate the transformer's voltage as per (3.16) assuming that the core's material, throughout the integration period, remains inside the linear region of the BH curve.

$$\begin{cases} \phi_{fi\alpha} = \dfrac{1}{n_k}\displaystyle\int_0^t v_{t\alpha}\left(t\right)dt \\ \phi_{fi\beta} = \dfrac{1}{n_k}\displaystyle\int_0^t v_{t\beta}\left(t\right)dt \end{cases} \tag{3.16}$$

The above approach suffers from errors that will inevitably be integrated over time and, thus, is unsuitable for practical application. As such, the transformer flux can be estimated or measured in different ways. A common method, as shown in [98], is to use an additional coil in the core, also called a magnetic ear, and measure its inductance using an HF signal. Then, by taking advantage of the relation between permeability and inductance, it is possible to estimate $\phi_{i\alpha}$ and $\phi_{i\beta}$. It is also possible to use the magnetostriction properties of the core's material to measure the transformer flux bias indirectly with a strain gauge. Another possible method is to use a lossy integrator that will act as a low pass filter in the measurements of the transformer voltages to obtain an approximation of the transformer flux in each leg.

3.1.3 Simulation Results

In an effort to obtain numerical simulation validation for the proposed modulation method, a Matlab/Simulink implementation of both the converter and modulation method was performed. The simulation was done using SimPowerSystems switched models of the semiconductors and a linear transformer model, an input 2nd order input filter with a $4mH$ inductor, a $3.3\mu F$ capacitor and a damping resistor of 19Ω was used along with an RL load of $10mH$ and 10Ω.

To obtain the reference values of $\boldsymbol{\chi}^*$ a Venturini-Alesina method for the 3×4 equivalent DMC was used. The transformer was considered to be ideal, and for the sake of results presentation, a reference core area of 540 mm^2 was considered so that the results could be presented in magnetic field density units for a reference material with 0.3 T of characteristic magnetic flux density. The reference value and the core dimensions were extracted considering a reference ferrite core[5].

As detailed in (3.14) for each reference vector for the equivalent converter, the states of the primary and secondary converter sides are unfolded in a way that minimises the cost function g_f. As an illustrated example, depicted in Figure 3.4, the simulation values of the computed values for g_f were obtained at $t = 1.2s$.

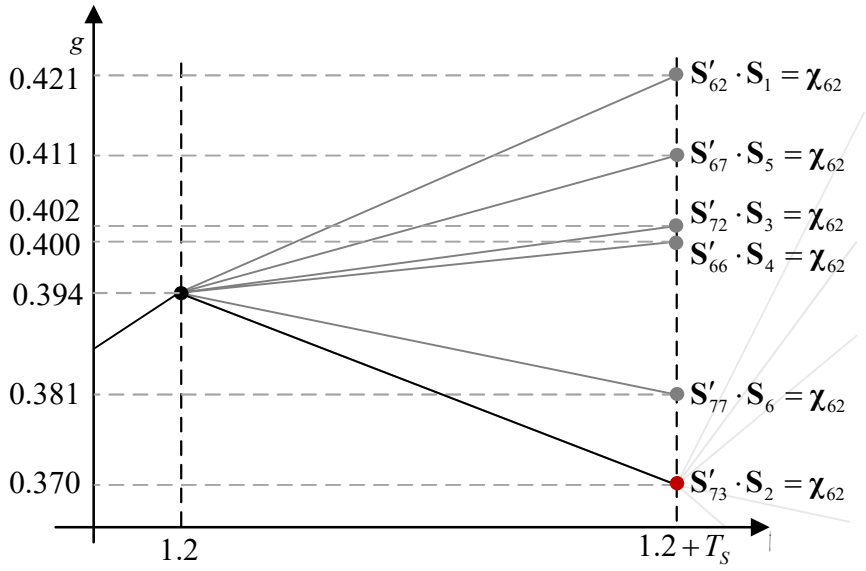


Figure 3.4 Partial simulation results of the computation of the cost function at t=1.2s with all combinations of S' and S that result in the reference vector $\boldsymbol{\chi}_{62}$.

It is significant to note that the reference state $\boldsymbol{\chi}^*_{62}$(where the sub-index indicates the number of the state according to the numeration of the tables mentioned above) can be attained with six unique combinations of the states of $\mathbf{S}'$ and $\mathbf{S}$. This is depicted in Figure 3.4 where the selected combination was $\mathbf{S}'_{73}$ and $\mathbf{S}_2$ since it is the pair that minimises the cost function g implemented according to (3.15).

[5] Deeper considerations regarding the transformer design are at this moment disregarded, since the design of a MF transformer will be approached with detail in Section IV.

This process is repeated for each new reference vector. The switching frequency, f_{sw}, was selected to be 20 kHz for the results shown below. Figure 3.5 and Figure 3.6 show results obtained during a period of 0.1 s with an output wave of 50Hz.

The first figure shows the switched currents at each of the transformer phases, in light grey, superimposed by the currents at each output phase (Output phases A, B and C in purple, blue and brown, respectively).

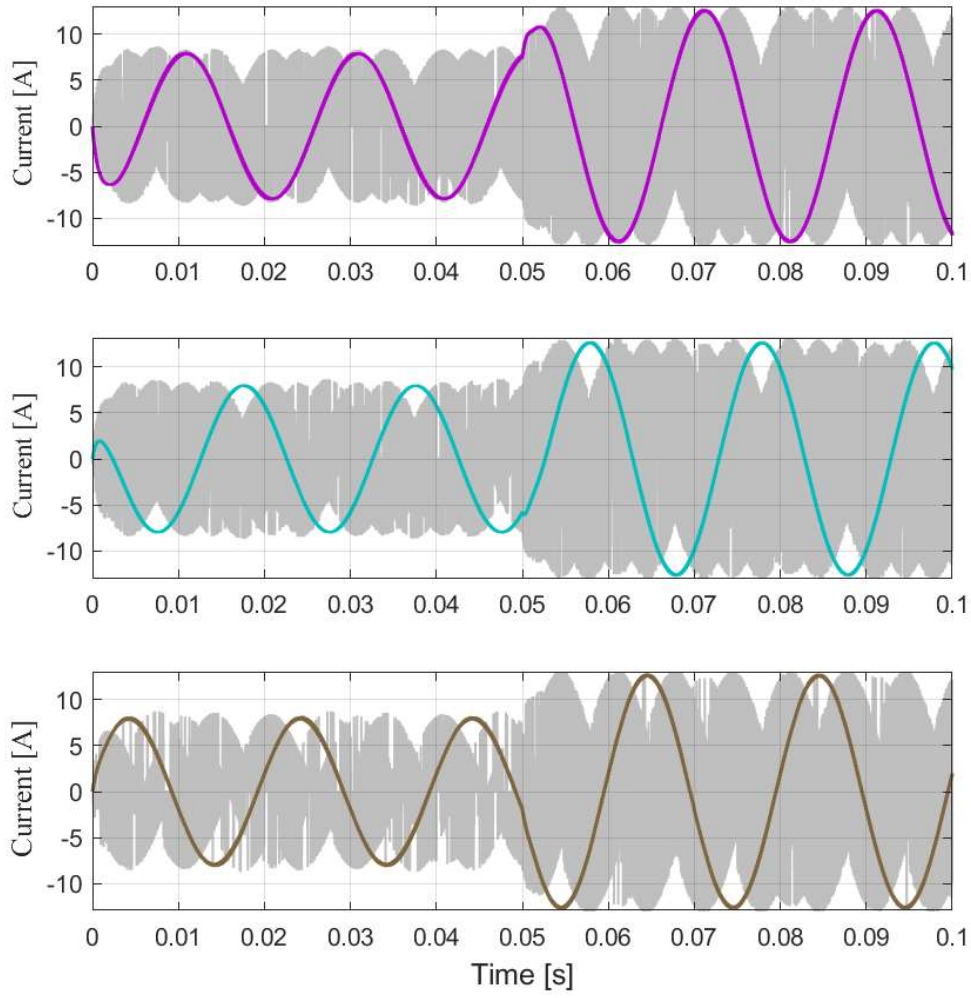


Figure 3.5 Simulation results of the output currents and transformer currents obtained for a period of 0.1 seconds. Purple, blue and brown traces depit the currents at the output phases A, B and C, repectively, while the grey traces depict the currents at each of the corresponding transformer phases.

The results of Figure 3.5 can be interpreted as if the secondary side converter is reconstructing the switched transformer currents into the sinusoidal low-frequency currents of the output, which is expected when considering that the output currents were modulated using the reference vectors $\boldsymbol{\chi}^*$.

The main results are shown in Figure 3.6, where it is possible to observe that the magnetic flux density never exceeds the reference value of 0.3 T.

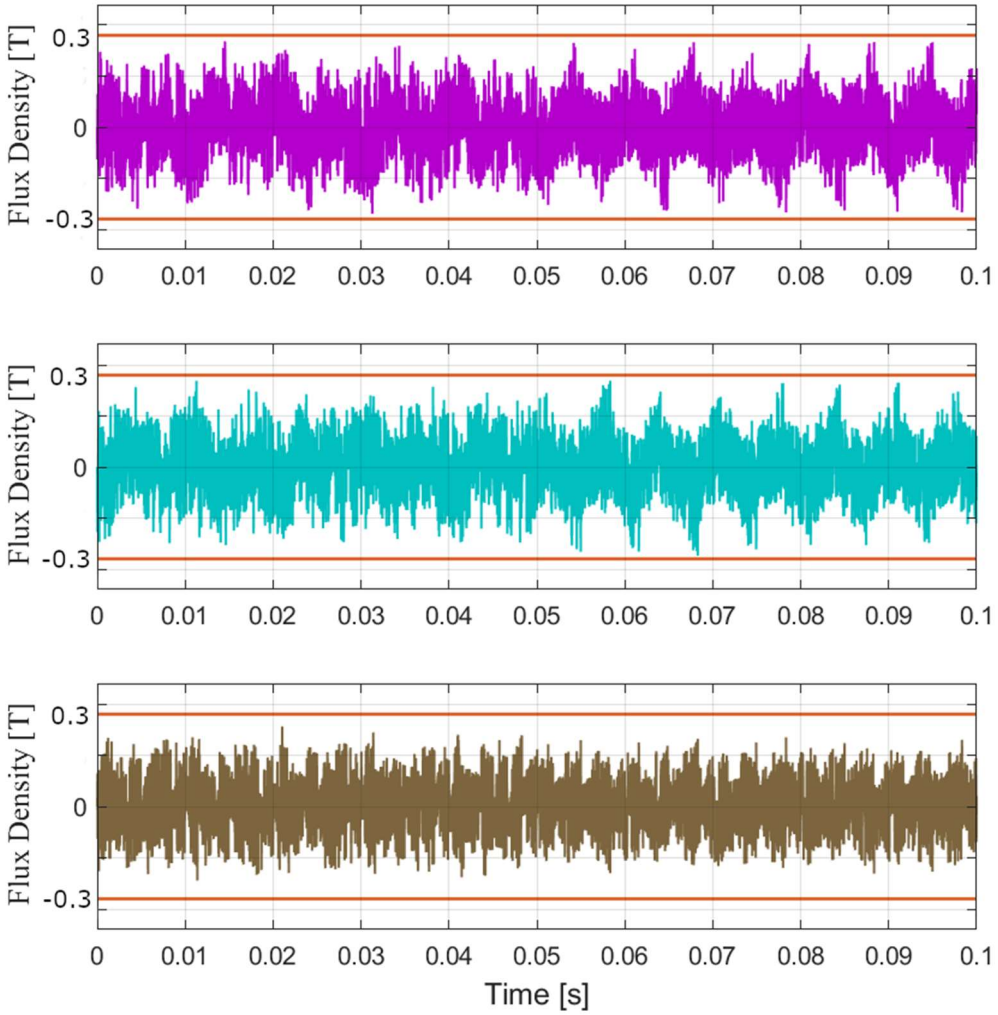


Figure 3.6 Simulation results of the magnetic flux density at each of the transformer phases with demarked limits of the defined limit for maximum flux density for the reference core. Purple, blue and brown traces show the magnetic flux density at the first, second and third winding of the transformer.

The presented results demonstrate the ability to transform a modulation/controller for an equivalent DMC and unfold it to the proposed SST.

3.2 A Leakage Tolerant Commutation Method

Matrix converters use well-timed commutation methods that prevent short-circuiting the input capacitors or opening the output inductive currents. These methods can be based on the direct measurement of the input voltage signals or the output current signals [99].

The commutation of matrix converters is mainly considered a solved challenge. However, in the unique situation of the use of matrix converters at the output of MF/HF transformers, such as the one depicted in Figure 3.1, the problem becomes non-trivial due to the energy stored in the transformer leakage inductances. Therefore, commutation methods that, besides attending to the typical constraints imposed by matrix converters, also take the recirculation of this energy into account are required.

The simplistic approach to address this issue is to add a clamping circuit at the output of the MF transformer, as suggested in [100,101] and depicted in Figure 3.7. The obvious downside of this approach is the decreased power density, increased power losses and potential distortion of the transformer voltages and currents.

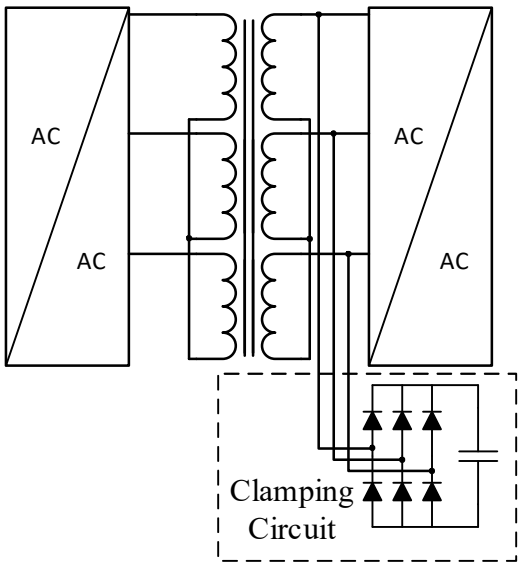


Figure 3.7 Depiction of a clamping circuit that provides a path for the circulation of the transformer's stored leakage energy

To overcome the downsides of using clamping circuits and still be able to appropriately commutate the secondary side converter, dedicated commutation methods, assisted or not by additional devices, were developed for numerous topologies. Most commutation processes do not use clamping circuitry and instead make use of the primary/source side converter to apply voltages to the transformer to ease the commutation of the secondary side converter. These

methods are called source-based commutation methods. Another alternative to these methods is the use of additional switching devices to create new paths for leakage energy recirculation [102].

Examples of application of source-based commutation methods for indirect matrix converter-based SST, where the typical virtual DC-link of the converter is replaced with an MF/HF transformer, are found in [103] and [104]. For this converter, the commutations involve only two switches, and as a consequence, the voltage applied to the single-phase transformer needs to be selected as positive or negative only according to the output current signal.

Further examples of source-based commutation in SST using single-phase transformers can be found in [105] [106] and [107], with each work emphasising the details of their topology. A particular mention should be given to the work in [108], where the authors generalise the source-based commutation method for single-phase transformer topologies using a "current decoupling stage" that circulates the currents in the output converter while using the source side converter to drive the leakage inductor current in the desired direction.

Despite all the contributions in commutation methods that handle the recirculation of the leakage energy in some way, the usage of three-phase transformers with three-phase converters is yet to be thoroughly explored. The above-presented source-based commutation methods don't consider the dependence of the circulation of the leakage energy in each phase on the other two phases. Furthermore, for the above-presented techniques, the current in the transformers can only assume two values, the output current's positive and negative amplitudes, such is not the case for topologies such as the one depicted in Figure 3.1, where the current at any coil can be a combination of the output currents of the secondary side converter.

This section will then present a source-based commutation method that is suitable for multi-phase HF/MF transformers with multi-phase converters at the secondary of the transformer.

3.2.1 State Commutation Model Description

The commutation between matrix converter states happens at a much smaller time scale than the converter control loop or switching period. On that basis, some assumptions can be made such that the converter and filters can be modelled at the commutation timescale.

The first assumption is that the leakage inductances, L_{ick}, $i \in \{1, 2, \cdots, n\}$, are much smaller than the output filter inductors. Under such conditions, the output currents can be seen to behave as current sources across the entire communication period.

The second assumption is that the input converter can be modelled as a controlled voltage source since the source-side converter commutation does not impact the leakage inductor currents (since the typical commutation methods already provide continuity to the output currents). Obviously, these controlled voltage source states are limited to the possible converter states.

The third and last assumption is that the transformer is ideal except for the stored leakage energy. The energy stored in the core's magnetisation (usually modelled as a parallel branch to the transformer composed of an inductor with a paralleled resistor) should not be considered since, similarly to the second assumption, the primary side converter already provides circulation paths for this energy.

Under these assumptions the SST from Figure 3.1 can be modelled for commutation purposes, as depicted in Figure 3.8.

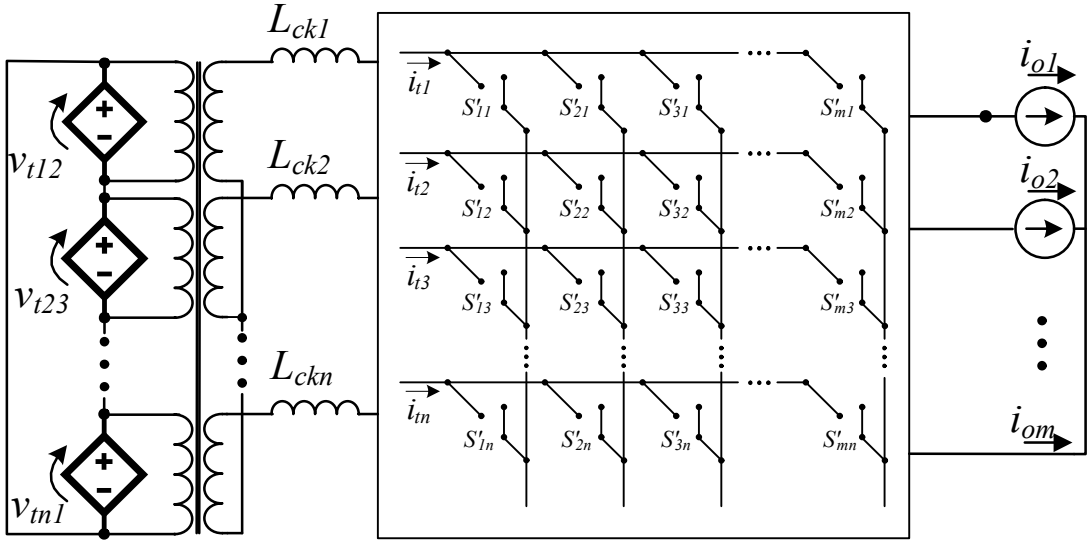


Figure 3.8 SST model for the development of commutation methods with n windings and m output phases.

In a steady state, i.e. when not commutating any converter, the transformer currents can be obtained, as per (3.17), using the transpose of matrix $\mathbf{S}'$.

$$\begin{bmatrix} i_{t1} \\ i_{t2} \\ \vdots \\ i_{tn} \end{bmatrix} = \mathbf{S}'^{T} \begin{bmatrix} i_{o1} \\ i_{o2} \\ \vdots \\ i_{om} \end{bmatrix} \tag{3.17}$$

Commutating the secondary converter is changing between states of the matrix $\mathbf{S}'$. Hereby, the state of the converter before the commutation process is referred to as $\mathbf{S}'_i$ and the desired

converter state after the commutation is referred to as $\mathbf{S}'_f$. The goal is then to transition from $\mathbf{S}'_i$ to $\mathbf{S}'_f$ obeying the standard matrix converter topological constraints (not opening the output currents nor short-circuiting the input voltages) and to ensure that adequate circulation paths for the leakage energy exist. The last constraint means that the currents across the coils must freewheel to the desired values and cannot be hard switched to their new value since that would cause severe overvoltages across the coils that would damage the semiconductors.

3.2.2 Commutation Algorithm

Consider the general case of a transformer with n windings and m output phases interlinked by an $n \times m$ matrix converter following the same model assumptions as described in the previous section. Notice that, for this case, the matrix $\mathbf{S}'$ is of size $m \times n$.

Subtracting $\mathbf{S}'_i$ to $\mathbf{S}'_f$, as per (3.18), yields matrix $\mathbf{T}$ also of size $m \times n$. Given the properties of matrixes $\mathbf{S}'_i$ and $\mathbf{S}'_f$, as per (2.5), implies that the lines of matrix $\mathbf{T}$ obey the condition in (3.19).

$$\mathbf{T} = \mathbf{S}'_f - \mathbf{S}'_i = \begin{bmatrix} S'_{f11} - S'_{i11} & S'_{f12} - S'_{i12} & \cdots & S'_{f1n} - S'_{i1n} \\ S'_{f21} - S'_{i21} & S'_{f22} - S'_{i22} & \cdots & \vdots \\ \vdots & \vdots & \ddots & \vdots \\ S'_{fm1} - S'_{im1} & \cdots & \cdots & S'_{fmn} - S'_{imn} \end{bmatrix} \tag{3.18}$$

$$\sum_{k=1}^{n} \mathrm{T}_{jk} = 0 \quad j \in \{1, 2, \cdots, \mathrm{m}\} \tag{3.19}$$

If line j obeys (3.19) by having all elements of the line being equal to 0, that means that the semiconductors that connect the input windings to the output phase j do not participate in the commutation process meaning that lines j of matrixes $\mathbf{S}'_i$ and $\mathbf{S}'_f$ are equal.

The remaining way line j can obey (3.19) is by having one index being 1 and another index being -1. Assuming that $\mathrm{T}_{jk} = 1$ and $\mathrm{T}_{ji} = -1$ that means that the current circulating at the output phase j circulates at winding i before the commutation process and is desired to circulate at winding k after the commutation.

Consider now the sign function as per (3.20) that allows to define the vector of the output currents signs as in (3.21).

$$\operatorname{sgn} x = \begin{cases} -1 & \text{if } x < 0 \\ 1 & \text{if } x \geq 0 \end{cases} \tag{3.20}$$

$$\operatorname{sgn}\left(\mathbf{I}_o\right) = \left[\operatorname{sgn}\left(I_{o1}\right) \quad \operatorname{sgn}\left(I_{o2}\right) \quad \cdots \quad \operatorname{sgn}\left(I_{om}\right)\right]^T \tag{3.21}$$

The information contained in the matrix (3.18) and vector (3.21) allows devising the necessary voltage signals to be applied in the primary voltage sources in order to safely commutate each of the output currents. This can be obtained by the element-wise multiplication of the matrix $\mathbf{T}$ and the vector $\operatorname{sgn}\left(\mathbf{I}_o\right)$ as shown in (3.22).

$$\mathbf{K} = \mathbf{T} \odot \operatorname{sgn}\left(\mathbf{I}_o\right) = \begin{bmatrix} (S'_{f11} - S'_{i11})\operatorname{sgn}\left(I_{o1}\right) & (S'_{f12} - S'_{i12})\operatorname{sgn}\left(I_{o1}\right) & \cdots & (S'_{f1n} - S'_{i1n})\operatorname{sgn}\left(I_{o1}\right) \\ (S'_{f21} - S'_{i21})\operatorname{sgn}\left(I_{o2}\right) & (S'_{f22} - S'_{i22})\operatorname{sgn}\left(I_{o2}\right) & \cdots & \vdots \\ \vdots & \vdots & \ddots & \vdots \\ (S'_{fm1} - S'_{im1})\operatorname{sgn}\left(I_{om}\right) & \cdots & \cdots & (S'_{fmn} - S'_{imn})\operatorname{sgn}\left(I_{om}\right) \end{bmatrix} \tag{3.22}$$

In general terms, each line of the matrix $\mathbf{T}$ is multiplied by -1 if the output current correspondent to that line is negative, which physically means that a positive voltage across a given coil is required to freewheel said current out of this coil assuming that the new paths for that current exist as it will become clear later.

Finally, consider the vector that describes the signals of the voltages applied to the primary of the transformer in (3.23).

$$\operatorname{sgn}\left(\mathbf{V}_t\right) = \left[\operatorname{sgn}\left(v_{t12}\right) \quad \operatorname{sgn}\left(v_{t23}\right) \quad \cdots \quad \operatorname{sgn}\left(v_{tn1}\right)\right]^T \tag{3.23}$$

Given a set of voltages, $\mathbf{v}_t$, applied to the transformer's primary the necessary constraints to commutate the output current on phase *j* are satisfied if the condition described in (3.24) equals to 2.

$$\sum_{k=1}^{n} \mathrm{K}_{jk} \operatorname{sgn}\left(v_{tk}\right) = \begin{cases} 2\text{ , } \mathbf{V}_t \text{ satisfies the constrains} \\ 0\text{ , } \mathbf{V}_t \text{ does not satisfy the constrains} \\ \text{-2, } \mathbf{V}_t \text{ does not satisfy the constrains} \end{cases} \quad j \in \{1, \cdots, \mathrm{m}\} \quad k \in \{1, \cdots, \mathrm{n}\} \tag{3.24}$$

When the value of (3.24) equates to two, it means that the voltages have the necessary signs to commutate the current in output phase *j*. When it equates to 0 it represents that only one of the transformer's primary voltages has the correct sign to commutate the current in output phase *j*. Finally, if it equates to -2, then it represents that none of the primary transformer voltages has the correct sign to commutate the current in output phase *j*. The relation in (3.24) admits no other values.

The different combinations of possibilities in (3.23) form a set of vectors with different properties that can be numbered based on the signs of each of their voltages. For a converter with 3 input phases this means that there are 6 possible unique combinations of input voltage signs, at each instant the vector with the hight amplitude that presents the required signs characteristics is selected. This set of vectors that will be used to aid the commutation are hereby referred to as Intermediate Vectors (IV).

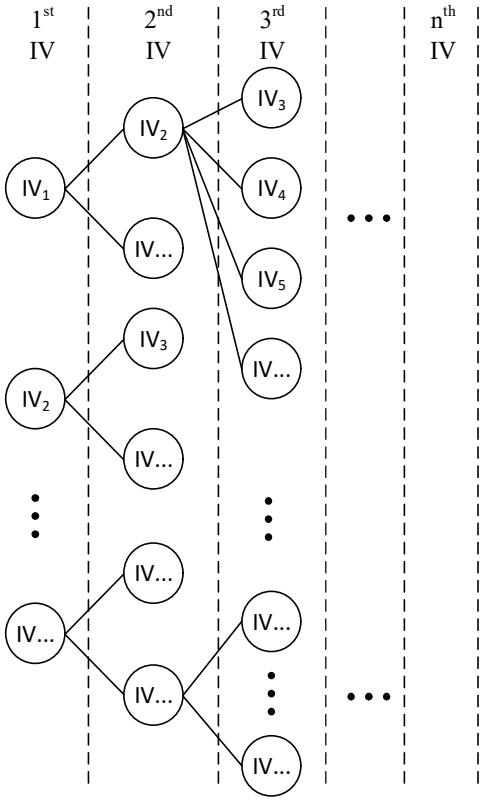


Figure 3.9 Depiction of a possible search graph where nodes represent the possible intermidate vectors on which the breath-first search algorithm can be applied to obtain the minimum set of IV.

The number and characteristics of each commutation might make it so that a single IV[6] is insufficient to commutate all the output currents. A breadth-first search can be performed across all the possible combinations of the intermediate vectors to find the smallest set of intermediate vectors that allows the commutation of all the output currents. Figure 3.9 depicts the graph representation on which the search will take place. Using the breadth-first algorithm, a minimum resulting set of necessary intermediate vectors is guaranteed.

[6] Intermediate vector refers to the source side converters states that will apply different voltages to the transformer's primary with the sole purpose of commutating the secondary side converter.

This process can be solved in real-time in a Field Programmable Gate Array (FPGA) or, for a given topology, it can be solved offline for all commutations of the secondary converter in combination with all possible signs of the output currents and signs of the input voltages. Considerations on the memory requirements for a practical application of this commutation method are taken below in Section 3.2.4.

3.2.3 Commutation Method on the Proposed Solid-State Transformer

To better illustrate the proposed method, an example is here provided for the SST topology of Figure 3.1. The resulting commutation model, as described in section 3.2.1, is depicted in Figure 3.10. Consider, for example, the state of $\mathbf{S}'_i$ as vector number 62 from Table A.2 of Appendix A while the state of $\mathbf{S}'_f$ is vector 51 from the same table.

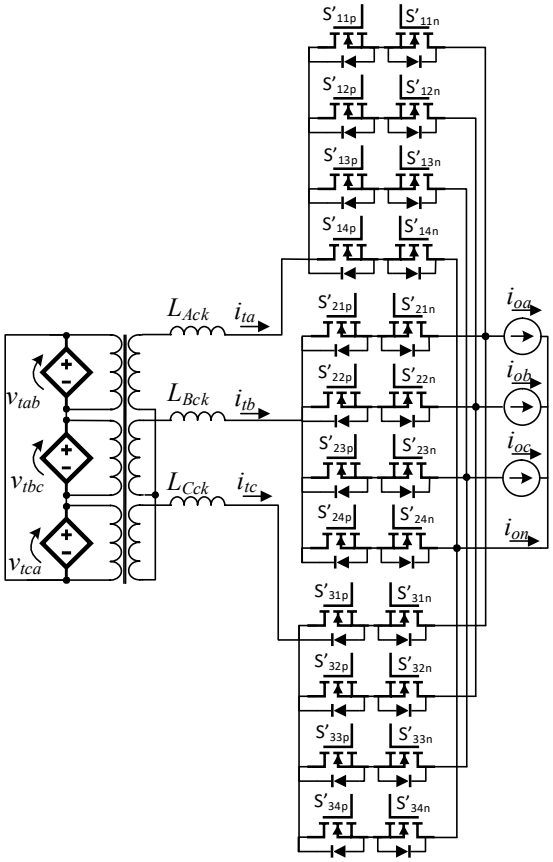


Figure 3.10 Commutation level model for the proposed SST.

The resulting matrix $\mathbf{T}$ from (3.18) is now of size 3×4 and is given by (3.25).

$$\mathbf{T} = \mathbf{S}'_f - \mathbf{S}'_i = \begin{bmatrix} -1 & 1 & 0 \\ 1 & -1 & 0 \\ 0 & 1 & -1 \\ 0 & -1 & 1 \end{bmatrix} \tag{3.25}$$

Also, for the sake of the example, consider the following signs for the output currents as given by (3.26), which translates to the output currents on output phases a and b being positive and the currents on the output phases c and d being negative.

$$\operatorname{sgn}\left(\mathbf{I}_o\right) = \begin{bmatrix} 1 & 1 & -1 & -1 \end{bmatrix}^T \tag{3.26}$$

Matrix $\mathbf{K}$ can then be computed as per (3.27).

$$\mathbf{K} = \mathbf{T} \odot \operatorname{sgn}\left(\mathbf{I}_o\right) = \begin{bmatrix} -1 & 1 & 0 \\ 1 & -1 & 0 \\ 0 & -1 & 1 \\ 0 & 1 & -1 \end{bmatrix} \tag{3.27}$$

The sign of the voltages at the coils depends on the applied intermediate vector. For this topology, six different voltage vectors can be obtained, with the properties highlighted in Table 3.1.

Table 3.1 Combinations of the signs of the voltages applied to the transformer windings for each intermediate vector.

Intermediate Vector	$\operatorname{sgn}(v_{ab})$	$\operatorname{sgn}(v_{bc})$	$\operatorname{sgn}(v_{ca})$
IV 1	1	1	−1
IV 2	1	−1	1
IV 3	1	−1	−1
IV 4	−1	1	1
IV 5	−1	1	−1
IV 6	−1	−1	1

Solving (3.24) for each intermediate vector and each output current, it is possible to compute Table 3.2, where according to the same equation, a given intermediate vector respects the conditions to switch the current on a given output phase if and only if the result of (3.24) equates to 2. Therefore, for the set of conditions described above, the intermediate vector IV 1 allows the switch of the current on phase n, IV 2 enables the switch of the currents on phases *b* and *c* and so on and so forth.

Table 3.2 Computation of the feasibility criteria in (3.24) for each intermediate vector and each output phase current. A given intermediate vector satisfies the criteria to switch a given output phase current when it's result is 2 (highlighted in green).

Intermediate Vector	Sum on Phase a	Sum on Phase b	Sum on Phase c	Sum on Phase n
IV 1	0	0	-2	2
IV 2	-2	2	2	-2
IV 3	-2	2	0	0
IV 4	2	-2	0	0
IV 5	2	-2	-2	2
IV 6	0	0	2	-2

The minimum set of intermediate vectors that allows the switch of all currents is comprised of the intermediate vectors IV2 and IV5, which can be applied in any order.

After determining the intermediate vectors, the commutation process starts by opening the non-conducting semiconductors of the load-side converter, Figure 3.11 a. The first intermediate vector can then be applied. This vector (IV 5) respects the conditions to commutate the output currents i_{oa} and i_{on} as per Table 3.2. Consequently, new paths for these currents are created by closing the semiconductor S'_{21p} and semiconductor S'_{34n}, the selection between the positive conducting and negative conducting is done taking into consideration the signal of the output current, this can be seen in Figure 3.11 b).

Following a defined, but relatively small, delay, the semiconductors S'_{11p} and S'_{24n} can be opened as the current that was once flowing through them has now freewheeled into the new winding, as depicted in Figure 3.11 c). The second intermediate vector (IV 2) can then be applied. This vector respects the conditions necessary to commutate the currents i_{ob} and i_{oc}. Therefore, new current paths for these currents can be created by closing the semiconductors S'_{12p} and S'_{23n} as depicted in Figure 3.11 d). Once again, this causes the winding currents to freewheel to these semiconductors aided by the voltage the source side converter applies.

After another slight delay, the semiconductors S'_{22p} and S'_{33n} can be opened since the current of the output phases i_{ob} and i_{oc} is now flowing across the semiconductors closed in the previous step, as depicted in Figure 3.11 e). Finally, the remaining non-conducting semiconductors of the conducting bidirectional switches can be closed (S'_{12n}, S'_{21} , S'_{23p} and S'_{34}), finalizing the commutation steps, as shown in Figure 3.11 f). If necessary, the source-side converter can then apply the desired final vector, thereby finishing the commutation process.

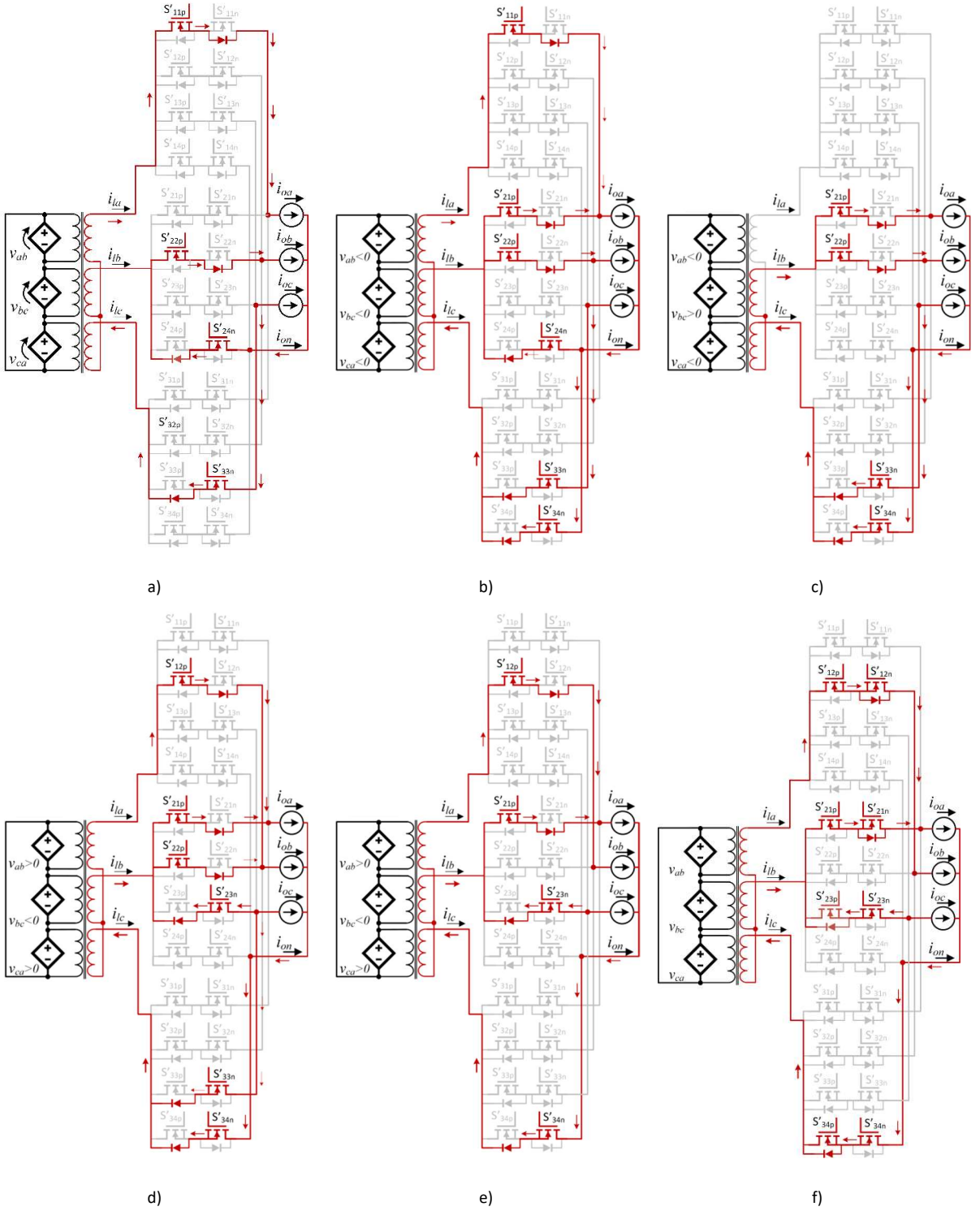


Figure 3.11 Step-by-Step depictions of the leakage tolerant commutation method when transitioning the state of the load side converter. a) Step 1 – Opening non conducting semiconductors; b) Step 2 – Apply first intermediate vector and create new current paths on the load side converter; c) Step – 3 – Open the new non-conducting semiconductors; d) Step 4- Apply second intermediate vector and create new current paths on the load side converter; e) Open the new non-conducting semiconductors; f) Close the non-conducting semiconductors of the conducting bidirectional switches and apply the source side final vector.

3.2.4 General Considerations on the Commutation Method for the Proposed Solid-State Transformer

The described commutation process requires either the online/real-time computation of the necessary intermediate vectors or the storage in a lookup table of all possible vector transitions of the output side converter computed offline.

Since the commutation process depends on the sign of the output currents, the solution can be obtained offline for all the possible combinations of the signs of the output currents. For the proposed topology, there are 14 possible arrangements of the output current signs. More generally, the number of possible combinations of the output currents is given by $2^m - 2$ where m is the number of output phases.

It is then possible to generate a set of 14 tables with 81×81 positions where each position stores the required intermediate vectors necessary to perform the commutation between S_i' and S_f' for a given set of output current signs. An example of 1 of the 14 tables is depicted in Figure 3.12, which shows the minimum number of intermediate vectors needed to perform the commutation. Each of the coordinates of this table stores the necessary set of intermediate vectors.

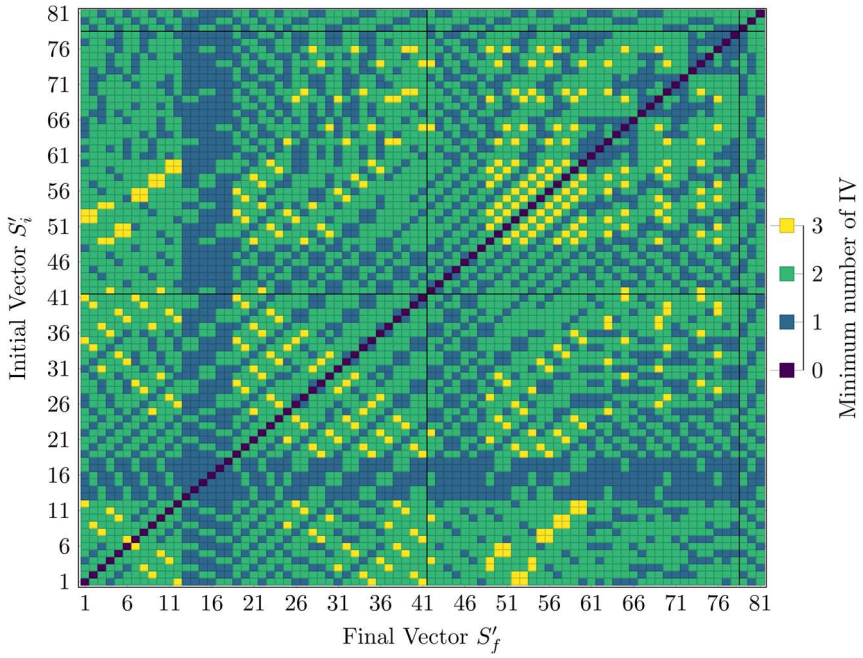


Figure 3.12 Example of a table storing the number of necessary intermediate vectors when the signals of the output currents are given by $\mathrm{sgn}(\mathbf{I}_o) = [1 \;\; 1 \;\; -1 \;\; -1]^T$. The blue, green and yellow squares mean that 1, 2 or 3 intermediate vectors, respectively, are required to commutate the converter between the corresponding states.

To minimise the storage requirements for all the information necessary to perform the commutation, it can be noted that each of the 14 tables is symmetrical along the diagonal from (1,1) to (81,81), allowing to reduce the total storage size to roughly half. Furthermore, it can be noted that the set of possible current signs can also be divided into two groups where, for each state of the first group, a negated state in the other group exists. Therefore, it is only necessary to store half of the tables since the requirements for the remaining can be easily computed from the first half simply by multiplying the requirements by -1. The resulting storage space required using the properties mentioned above and without any compression sums up to roughly 90 kB.

The average number of intermediate vectors can be used as a metric of the commutation process's average time. Figure 3.13 shows the average number of necessary intermediate vectors to go from a given initial vector S_i' to the final vector S_f' across all the conditions of the output currents. The total average for any vector transition sums to 1.69 intermediate vectors per transition. Furthermore, notice that the table is divided into 9 zones according to the vector's characteristics as stated in section 2.2.6, where it can be concluded that transitions from vectors in the range of 43 to 79 to vectors in the same range involve, on average, a higher number of intermediate vectors. Such consideration can be taken into account in the predictive controller control function.

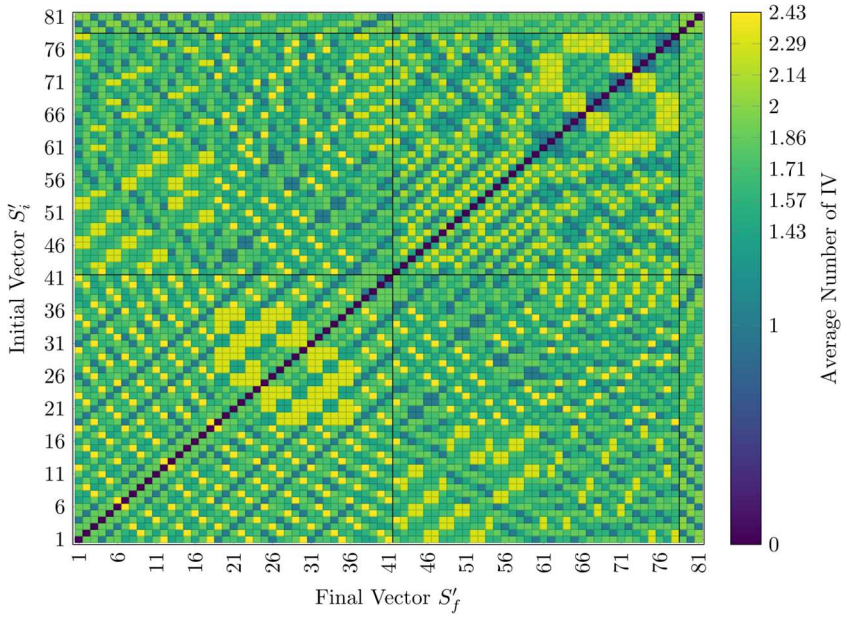


Figure 3.13 Depiction of the average number of intermediate vectors for any possible state of the output currents required to commuate the SST between two corresponding states. The gradient color scale goes from blue, for 1 intermediate vector, to yellow for 2.43 average intermediate vectors.

The commutation time will depend not only on the semiconductor's turn-on and turn-off times, as it usually does, but also on the value of leakage inductance. The minimum time that the intermediate vector must be applied is proportional to the leakage inductance and inversely proportional to the voltage applied across the coil as per (3.28).

$$t_{min} \propto \frac{L_{ck}}{|v_t|} \tag{3.28}$$

It then becomes clear that it is desirable to have a transformer designed with minimum leakage inductance and to use vectors which, besides respecting the sign criteria obtained with the proposed method, also have the highest possible amplitude.

Assuming that: the output currents are sinusoidal with amplitude I_o; the input voltages are also sinusoidal with a voltage amplitude V_i; the transformer is star connected; and that the leakage inductances are balanced and reduced to the primary side of the transformer then t_{min} can be computed per (3.29).

$$v_t = L_{ck}\frac{di_L}{dt} \Rightarrow t_{\min} = \frac{4I_o L_{ck}}{V_i} \tag{3.29}$$

Considering that the input voltage amplitude is 230V, a depiction of the minimum time the intermediate vector must be applied to ensure that all of the winding currents can finish the freewheeling process is shown in Figure 3.14,

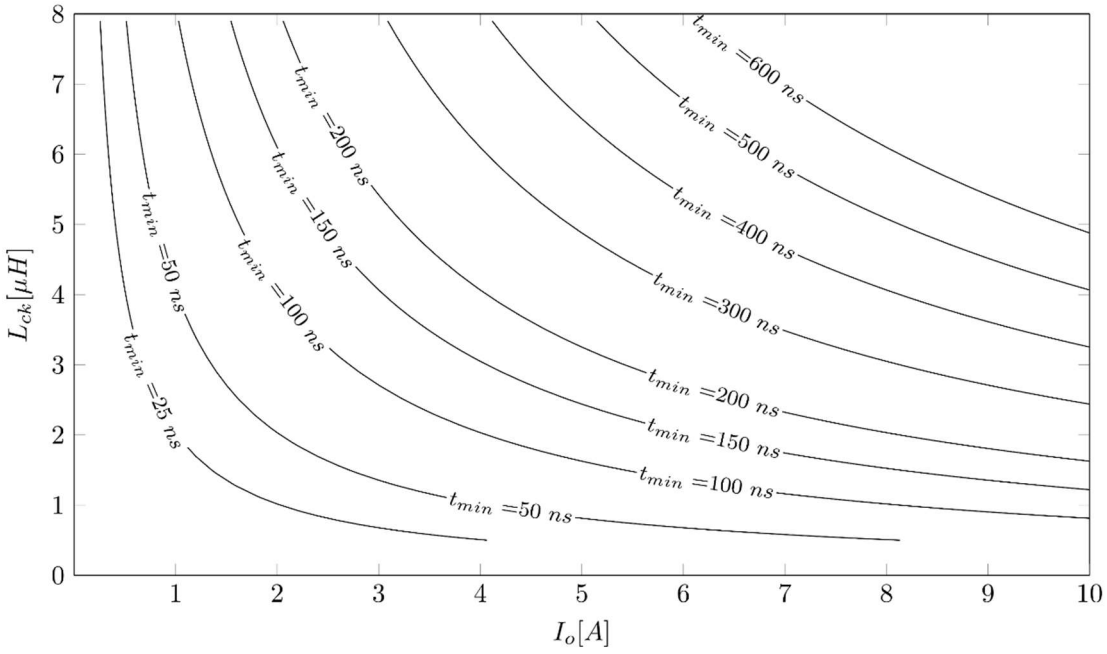


Figure 3.14 Contour on the minimum freewheeling commutation time as a function of the output current amplitude and the leakage inductance with an input voltage amplitude $V_i = 230V$.

Considering the deadtimes applied for the primary and secondary converter as t_{com} the total commutation time for a single intermediate vector is given by $t_{min} + 4t_{com}$. The total commutation time is then given by (3.30), where t_{Tcom} is the total commutation time and n_{IV} is the number of required intermediate vectors.

$$t_{Tcom} = \sum_{1}^{n_{IV}} \left(t_{min} + 4t_{com}\right) + 2t_{com} \tag{3.30}$$

Since the computed average number of intermediate vectors was computed to be 1.69 than the average commutation time is $1.69(t_{min} + 4t_{com}) + 2t_{com} \approx 1.69t_{min} + 8.76t_{com}$. For $t_{com} = 100ns$ and $t_{min} = 400ns$ $t_{Tcom} \approx 1.5\mu s$. The converter switching period should be so that the average commutation time remains less than 10% of this period. As such a limitation an upper bound for the switching frequency is given by (3.31).

$$f_{sw} \leq \frac{0.1}{1.69t_{min} + 8.76t_{com}} \tag{3.31}$$

3.3 Considerations on the proposed topology

As mentioned at the beginning of this chapter, the proposed SST topology aims for applications where high-power density and/or high-power-to-mass ratio are required. The use of single-stage matrix converters allows an increase in the power density of the converters by a factor of 2.5 and increases the power-to-weight ratio by a factor of 5 [65]. Furthermore, according to the same authors, it also enables higher efficiencies for higher switching frequencies, a property desirable to reduce the MF/HF transformer volume and weight.

A summary of properties comparing the proposed topology to a typical SST topology formed by an AC/DC rectifier followed by an isolated dual active bridge and a DC/AC inverter is shown in Table 3.3.

Table 3.3 Properties comparison of a typical SST topology and the proposed SST topology.

	Typical SST	Proposed SST
Number of switches	28	48
Number of conversion stages	4	2
Electrolytic capacitor banks	2	0
Number of switches carrying the input current	2	3
Number of switches carrying the output current	2	3
Number of transformer windings	1	3

Despite the increased number of semiconductors, the absence of intermediate energy storage and fewer conversion stages can potentially result in higher power densities and power-to-mass ratios. The increased number of switches results in more switches sharing the input and output load currents; this means that the average load current per switch is less in the proposed topology than in the typical SST. Furthermore, the proposed topology is still capable of operating even after a failure in one of the output or input bidirectional switches, whereas, in the typical SST, a failure in one of the output switches results in a loss of the correspondent phase voltage.

3.3.1 Further modulation and commutation optimisations

The current description of the modulation method explores the redundant vectors that lead to the same reference control action (shown in Figure 3.3) to select the combination that minimises

the transformer flux. However, and as shown by the relation in (3.13), the minimisation of the flux depends only on the vector of the primary 3x3 DMC. This means that there is likely extra redundancy since among the redundant combinations, there can be more than one with the same primary input vector. The additional redundancy can be used to select combinations among the vector combinations that already minimise the transformer flux and also minimise the number of necessary commutation steps.

Even though the commutation method is optimised with regard to the number of intermediate vectors, it can still be further optimised in relation to the commutation time. To do so, the explicit value of the amplitudes of the input voltages and output currents would be required. This would allow, at the beginning of each IV of the commutation process, to explicitly compute the maximum current variation across a single winding, which, combined with the explicit measurement of the input capacitor voltages and the primary vector applied to the converter, allows to compute the required freewheeling time. These can drastically decrease the commutation time since most commutations do not need freewheeling the winding currents between the minimum and maximum currents; as such, the relation could be explicitly computed.

Chapter 4

SYSTEM DESIGN AND CONTROL

This chapter covers two main contributions – the proposed controller methodology and an optimised filter design. The chapter is divided into three sections: the design of the MF Transformer, a grid-connected filter design methodology that minimises the energy stored in the filter, and finally proposes a control methodology for the SST.

4.1 MF Transformer Sizing

Consequence of the necessity to recirculate the transformer leakage inductance current to commutate the secondary side converter it is desirable to design a transformer with low leakage inductance. With reduced leakage inductance and high-power density as the main design targets, a planar transformer topology was selected.

4.1.1 Introduction to Planar Transformers

Planar transformer research emerged in the early 1990s when miniaturisation of switched-mode power supplies was a trending topic [109]. This topic is even more relevant today, with switched power converters being used in high-demanding industries such as railways, ships, aeroplanes, and satellites, among many others.

Besides the miniaturisation advantages, planar transformers bring reproducibility to parasitic components (since the windings can be manufactured with PCBs), which are typically not observed in other transformer designs. The higher area-to-volume ratio allows for a higher cooling surface, and the nature of its fabrication process makes it easy to interleave windings to reduce leakage inductance.

The most apparent downsides to planar transformers are the large area footprint, lower copper filling factors, a limited number of turns, and higher winding capacities.

Planar magnetic windings are created by planar-wound structures such as laminated copper in multilayer PCBs. As such, planar cores depicted in Figure 4.1 are characterised by having a window where the width, l_w, is much higher than the height, h_w (with the dimensions according to Figure 4.1).

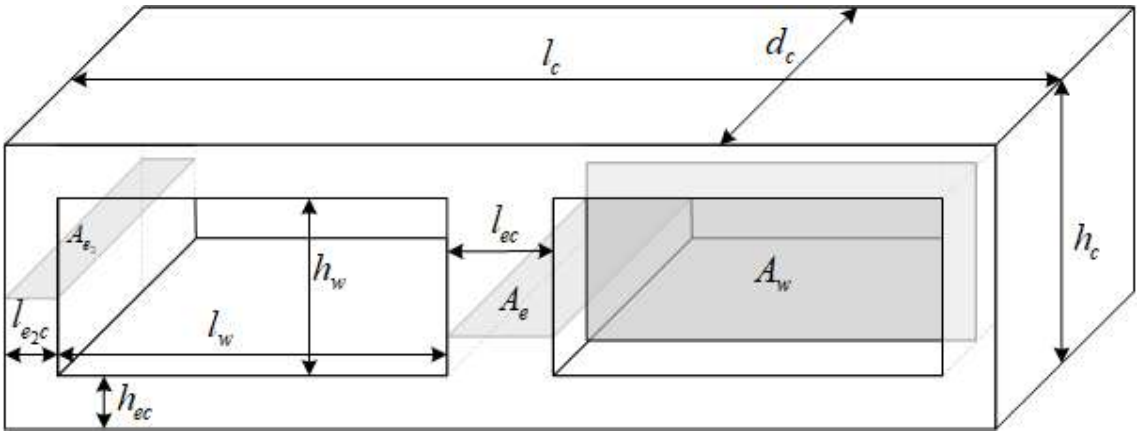


Figure 4.1 Depiction of a planar magnetic core, with detailed dimensions and relevant areas.

The planar wound structures can be seen in Figure 4.2 and Figure 4.3 for a single-phase and a three-phase transformer, respectively. The use of Printed Circuit Boards (PCBs) to create the wound structures makes it easy to have interleaved structures and, as such, reduces the leakage inductance. On the other hand, this comes at the cost of increased parasitic capacitances due to the increased surface area.

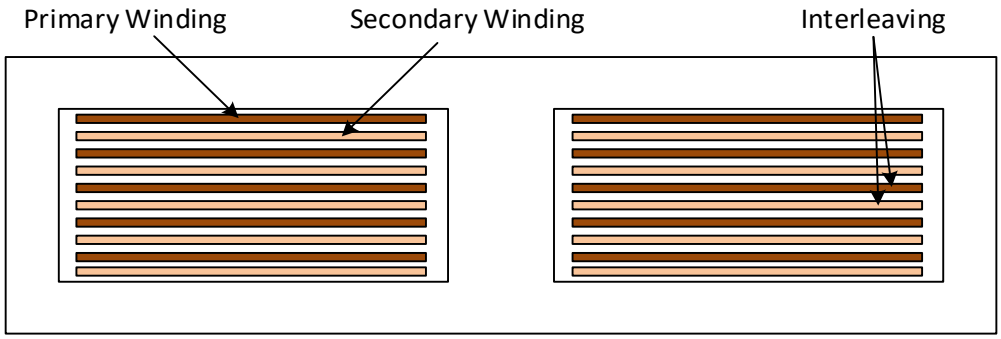


Figure 4.2 Depiction of interleaving structures for a single-phase transformer.

Figure 4.2 depicts the interleaving of two different windings for a single-phase transformer, while Figure 4.3 depicts the interleaving between 3 pairs of windings in two different arrangements.

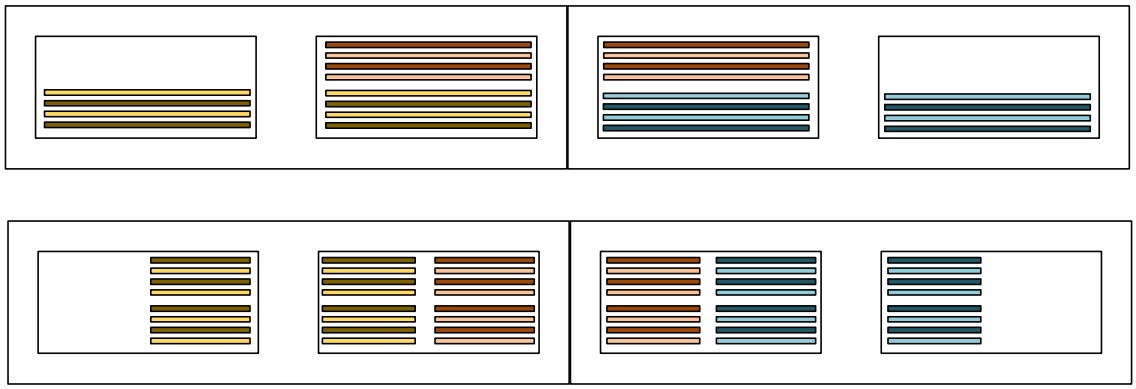


Figure 4.3 Depiction of two different interleaving structures for a three-phase transformer.

4.1.2 Transformer sizing relations

In every manner identical to more traditional transformer designs, the power handling capability of a transformer is intimately connected to the 4th power of the transformer core linear dimension, also called the area product. More specifically, the power handling capability of the transformer can be given by (4.1) where S_j is the apparent power of winding j, A_w and A_e are window winding area and the effective core cross-section, B_m is the maximum magnetic flux density the core material can operate at. J_o is the current density on the window area and k_f, k_b and k_{cu} are factors that consider the waveform factor, the core stacking factor, and the winding area filling factor.

$$\sum_j S_j = A_w A_e k_f k_b B_m f_s k_{cu} J_o \tag{4.1}$$

These variables will be a function of the operating conditions, materials and technologies employed in the transformer.

k_v is defined as the ratio between the RMS values of the applied voltage waveform and the average value of the same voltage as per (4.2)

$$k_v = \frac{V_{trms}}{\langle v_t \rangle} = \frac{V_{trms}}{\frac{1}{\tau}\int_0^{\tau} v_t(t)\,dt} \tag{4.2}$$

Where $v_t(t)$ is the voltage waveform applied to the winding, and τ is the time necessary to achieve the maximum flux density from the point the with null flux density. The integration in

(4.2) can be further expanded to (4.3), where $k_f = k_v/(\tau f)$ where f is the frequency of $v_t(t)$ [110].

$$V_{trms} = k_f f N k_b A_e B_m \tag{4.3}$$

As such the value of k_f varies for different shapes the voltage waveform with the value $\sqrt{2}\pi$ for sinusoidal waveforms and 4.0 for square waveforms.

The factor k_{cu} is defined as the ratio of the total copper cross-section that crosses the winding window area to the window area cross-section. The total conduction area is given by the number of turns N_j in winding j in (4.4).

$$k_{cu} = \frac{\sum_j N_j A_{cj}}{A_w} \tag{4.4}$$

Finally, the k_b represents the core stacking factor which is the ratio between the effective cross-section of the magnetic core and the cross-section A_e. This value is around 0.95 for laminated and tape-wound cores and unitary for ferrite cores.

The relation established in (4.1) allows for a preliminary selection of the magnetic core as it must obey (4.5) where A_p is typically named the area product of the magnetic core.

$$A_p = A_w A_e \geq \frac{k_f k_b B_m f_s k_{cu} J_o}{\sum_j S_j} \tag{4.5}$$

The selection of the remaining parameters will depend on the design goals and selected materials. Among the different core materials, ferrite cores are widely available in shapes like the one depicted in Figure 4.1. Combined with the existing availability of ferrite cores for planar transformers from previous works of the research group, the material selection was constrained to ferrite cores with $B_m \approx 300mT$.

The transformer losses can be subdivided into winding and magnetic core losses.

The winding losses result from the joule effect caused by the current circling the winding and its resistance as per (4.6).

$$P_{cu} = \sum_j I_j^2 R_j = \sum_j \rho_{wj} \frac{l_{cj}}{A_{cj}} I_j^2 \tag{4.6}$$

Since the length of each winding turn is not necessarily constant, it is typical to consider the mean length of a turn (MLT), considering that I_j can be given by the current density of winding

j, J_{cuj}, divided by the cross-section of the winding j conductor, A_{cj} then (4.6) can be expanded to (4.7)[7].

$$P_{cu} = \sum_j \rho_{wj} \frac{N_j \mathrm{MLT} J_{cuj}^2 A_{cj}^2}{A_{cj}} \tag{4.7}$$

Considering the total winding volume and assuming all windings use the same material with resistivity ρ_w then the losses, disregarding high-frequency effects, can be computed according to (4.8).

$$P_{cu} = \rho_w \mathrm{MLT} A_w k_{cu} J_o^2 \tag{4.8}$$

Core losses are typically given by the Steinmetz equation [111] shown in (4.9).

$$P_{fe} = K_c f^{\alpha} B_m^b + b f^{\alpha} B_m^{\beta} \tag{4.9}$$

α and β are constants that depend on material properties and these losses are generally given per unit volume. The manufacturers typically provide these constants, but they can also be obtained experimentally [112].

By replacing the current density of (4.1) in (4.8) it can be shown that P_{cu} is inversely proportional to the square value of the maximum flux density and frequency as in (4.10).

$$P_{cu} \propto \frac{1}{f^2 B_m^2} \tag{4.10}$$

In opposition, a direct inspection of (4.9) shows that the magnetic core losses are proportional to frequency and maximum flux density powered by α and β respectively. Considering a and b as the proportionality constants for the copper and core losses, respectively, the total losses, P_t, can be described by (4.11).

$$P_t = P_{cu} + P_{fe} = \frac{a}{f^2 B_m^2} + b f^{\alpha} B_m^{\beta} \tag{4.11}$$

Unless for the particular case where $\alpha = \beta$ there is no global minimum of the losses function.

[7] The effective conductor area can be reduced due to the skin effect. The skin depth is given by $\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$, for a reference frequency of 50kh $\delta = 292\mu m$. Given the nature of copper layers in planar transformer this effect posses little influence in the effective conductor cross section and as such the effect is disregarded.

$$\frac{\delta P_t}{\delta B_m} = -\frac{2a}{f^2 B_m^3} + \beta b f^{\alpha} B_m^{\beta-1} \tag{4.12}$$

$$\frac{\delta P_t}{\delta f} = -\frac{2a}{f^3 B_m^2} + \alpha b f^{\alpha-1} B_m^{\beta} \tag{4.13}$$

Equalling (4.12) and (4.13) to zero and replacing P_{cu} and P_{fe} in both equation yields (4.14) as the optimum value for P_t for a fixed value of B_m and (4.15)for a fixed value of f.

$$P_{cu} = \frac{\beta}{2} P_{fe} \tag{4.14}$$

$$P_{cu} = \frac{\alpha}{2} P_{fe} \tag{4.15}$$

The above relations allow us to roughly understand the required transformer area product and the computation of losses. The minimum required number of turns on the primary winding will be dependent on the waveform factor, the rms voltage applied to the primary winding, V_{tprms}, the maximum flux density and the core's cross-section as per (4.16).

$$n_{\min} = \frac{V_{tprms}}{k_f f B_{O/\max} A_c} \tag{4.16}$$

The corresponding magnetising inductance for the winding, j, is then function of the winding j number of turns and the magnetic reluctance of the corresponding winding flux path R_c as in (4.17).

$$L_{magj} = \frac{n_j^2}{R_c} \tag{4.17}$$

The leakage inductance can be approximated analytically using Dowell's formula [113] or improved analytical models [114].

The above analytical formulation serves as the basis for the preliminary sizing parameters of the planar transformer, whose design is covered in the following subsection.

4.1.3 Planar Transformer sizing

As previously mentioned, the availability of the ferrite cores in the research department restricted the core's selection. Previous works used a MagInc 0R49938EC ferrite core with an

extensive material characterisation for the design of a single-phase planar transformer [115]. At a switching frequency of 30 kHz, this core can handle a power of 3.4 kVA. The set of requirements described in Table 4.1 were defined for the laboratory-scaled prototype.

Table 4.1 Planar transformer requirements specification.

Specification	Value	Unit
Number of input/output phases	3	-
Power per phase	3	kVA
Maximum Leakage inductance per phase	1	μH
Minimum Magnetizing inductance	4	mH
Maximum peak primary voltage	600	V
Turns Ratio	4:3	1:n
Maximum magnetic flux density	250	mT
Maximum core temperature	180	$°C$
Core depth	37	mm
Single Core length	102	mm
Core window area	535	mm^2

The selection of the number of turns, as well as their distribution, were obtained using an iterative solver based on the relations described in section 4.1.2 (or similar variations) [116,117].

The iterative solver outputted several results, and the one with the least power loss was selected. The resulting planar transformer has 28 turns on the primary windings, and 21 turns on the secondary windings. The windings are interleaved, with each primary layer having 3 turns and each secondary layer having 4 turns. Between each layer, a FR4 pre-preg with a thickness of 300μm. The copper trace thickness is 70μm and each primary turn has a width of 8 mm while each secondary turn has a turn has a width of 10 mm.

The selected solution was then evaluated in a 2D finite element (FEM) solver [118] and the magnetic fields were solved for multiple excitation frequencies between 25 kHz and 300 kHz. The primary was excited with sinusoidal voltages with the amplitudes according to Table 4.1, the secondary was excited with a current source that results in the desired apparent power per phase. The 2D model and the resulting mesh are shown in Figure 4.4.

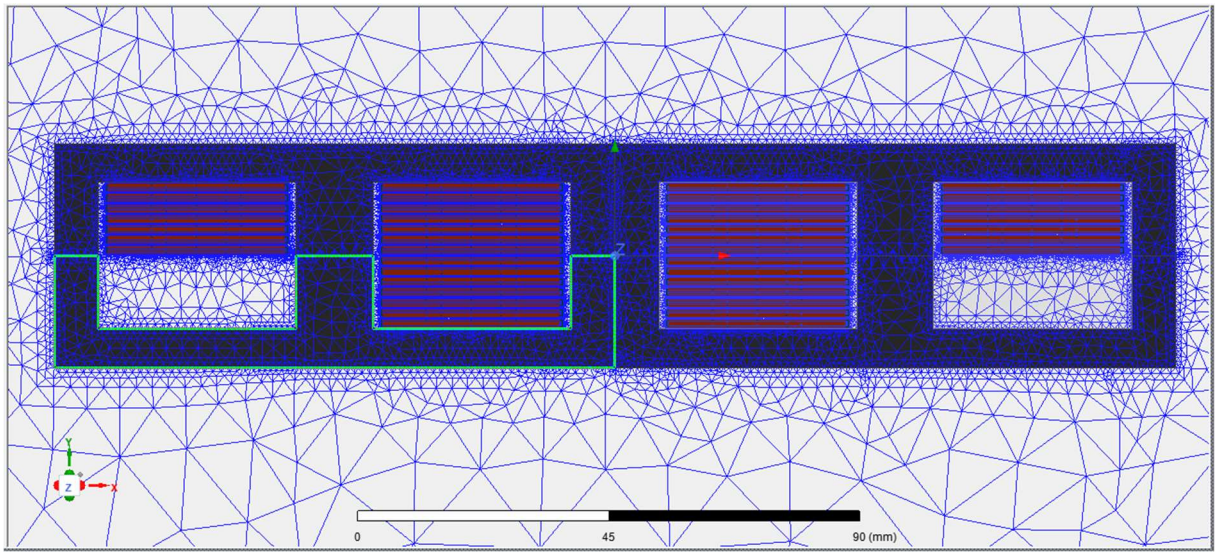
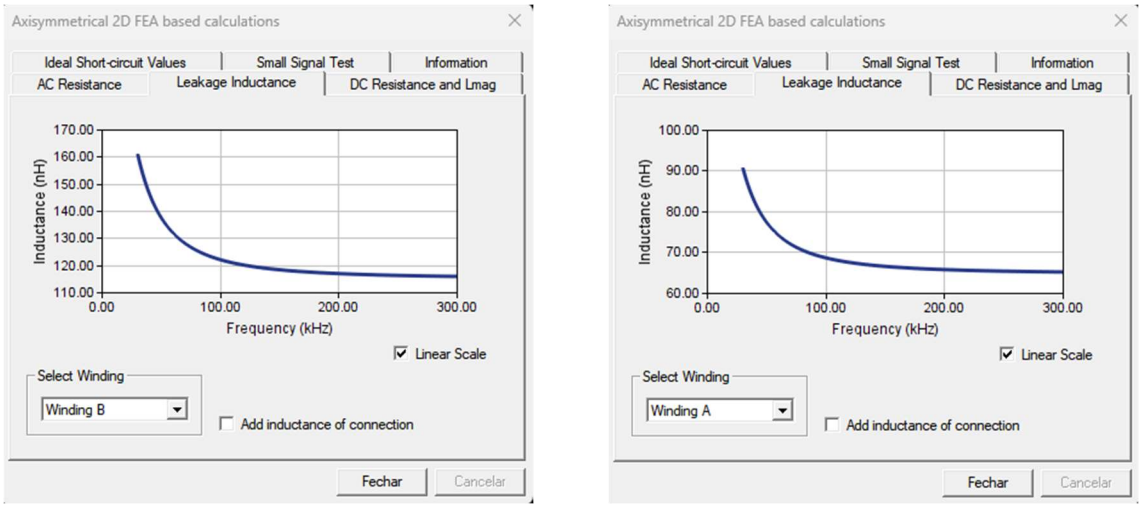


Figure 4.4 2D FEM model of the planar transformer and the used mesh. Element sizes were set by maximum length ($35\mu m$ for the copper traces, $100\mu m$ for the FR4 material, $1mm$ for the core and $4mm$ for the air).

The resulting leakage inductances as a function of the frequency for the primary and secondary windings with the highest leakage inductance are shown in Figure 4.5. The resulting leakage inductance is well below the target value, allowing for reduced freewheeling times in the commutation process.



a) b)

Figure 4.5 Leakage inductance as a function of the frequency for the a) primary and b) secondary windings with the highest leakage inductance.

Similarly, results for the AC resistance value in the primary and secondary windings with the highest resistance value are shown in Figure 4.6.

a) b)

Figure 4.6 Winding resistance as a function of the frequency for the primary and secondary windings with the highest resistance values.

PeMag reported an operating temperature of 130°C for the core well within the maximum Curie temperature of the material (200°C).

The self and mutual inductances per phase are shown in Table 4.2, where L_{11} is the primary self-inductance, L_{22} is the secondary self-inductance and L_{12} is the mutual inductance.

Table 4.2 Self and mutual inductances of each phase windings at 35 kHz.

	L_{11} $[mH]$	$L_{12} = L_{21}$ $[mH]$	L_{22} $[mH]$
Phase A	15.908	11.931	8.948
Phase B	17.768	13.326	9.995
Phase C	15.907	11.931	8.948

The leakage inductance at each frequency can be computed as per (4.18) whered n is the turns ratio between each winding pair (notice that the values for the self and mutual inductances are different at different frequencies, as evidenced by Figure 4.6).

$$L_{lck} = L_{11} - nL_{12} - nL_{21} + n^2 L_{22} \tag{4.18}$$

Finally, the results for the magnetic flux density field are plotted in Figure 4.7, where it is possible to observe that the maximum magnetic flux density remains within the requirements.

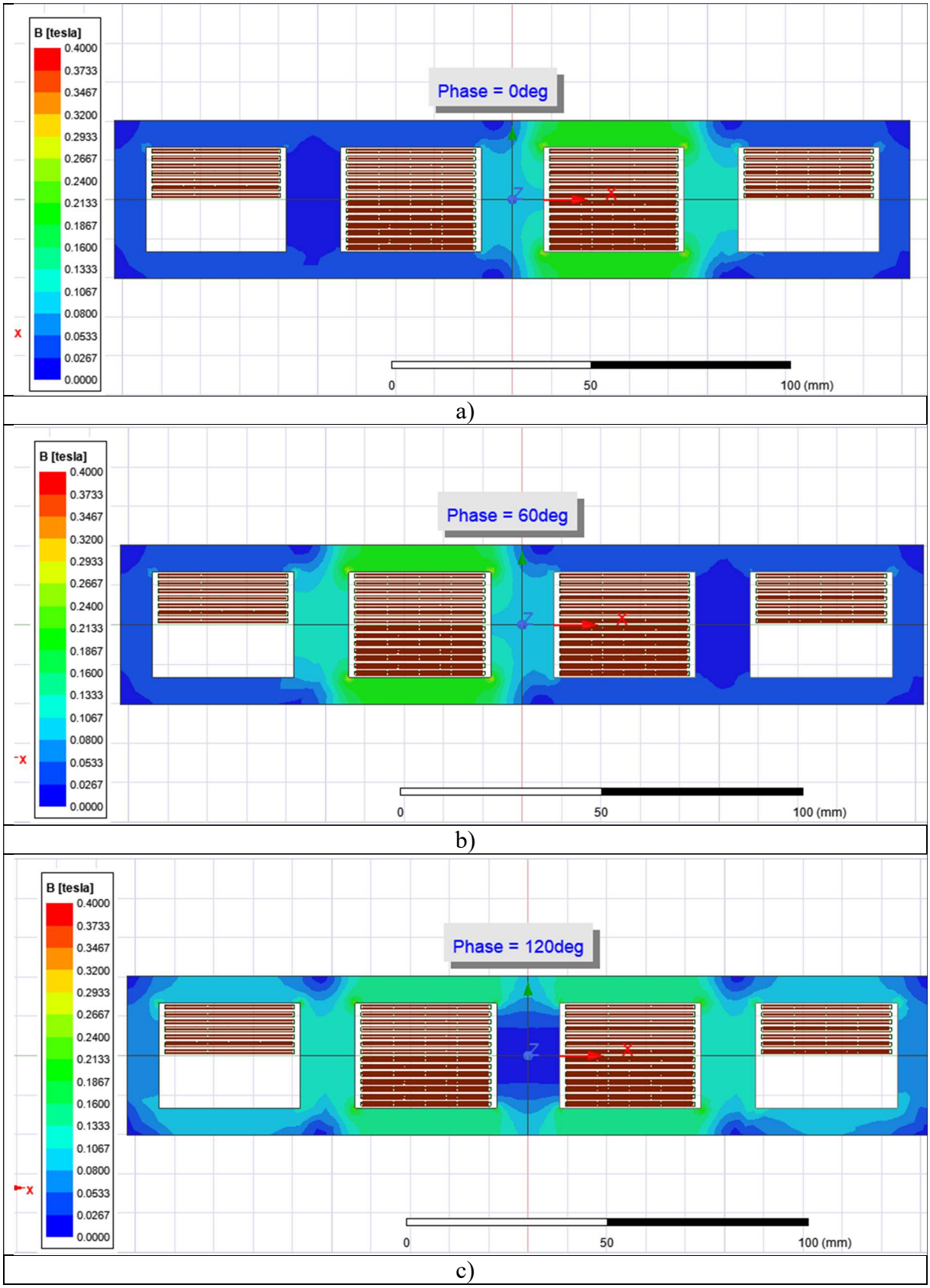


Figure 4.7 Depiction of the magnitude of the magnetic flux density field for different phases: a) 0°, b) 60° and c) 120°.

4.2 Optimized Filter Design

Switching power electronic converters operate at frequencies much higher than sources or loads and rely on filters to smooth voltages or currents. Matrix converters require a voltage source behaviour at the input and a current source behaviour at the output, given the inductive nature of the three-phase grid supply combined with the normative constraints regarding the input current THD, such as [119], low pass filters are required to attenuate the high-frequency currents at the voltage source input side of matrix converters.

Filter sizing implicates the existence of a set of criteria to be fulfilled by a suitable filter. Namely, the filter must provide a required attenuation at a given band of frequencies. This criterion is usually translated into a cut-off frequency and a roll-off rate that meet the demanded attenuation band. Though the filter frequency response is extremely important, other criteria are relevant when sizing the filter. These include the maximum consumed reactive power when the converter is idling, the maximum phase difference between the output and input voltages of the filter, maximum dissipated power in damping resistors, and maximum stored energy in the filter, among others.

The classical sizing of low pass 2nd order filters results in 2nd order transfer functions that can be well characterised by a natural frequency and a damping factor. The sizing of these filters is well documented, e.g., in [120], and can simply be formulated in a systematic manner. The downside of 2nd order filters is their roll-off rate at 40dB/dec, which implies setting off the cut-off frequency at least a full frequency decade below the switching frequency and consequently increasing the capacitance and/or inductance of the filter, as shown by (4.19) which represents the cut-off frequency for a 2nd order low pass filter.′

$$\omega_n = \sqrt{\frac{1}{LC}} \tag{4.19}$$

To further decrease the size of passive components, the roll-off rate must be increased; this can be achieved at the cost of higher-order filters. However, with the use of higher-order filters, design complexity is highly increased. 3rd order filters can, in some conditions, be reduced into 2nd order filters using some approximations.

A typical method to design higher-order filters is to use well-known polynomial functions to generate transfer functions with desired characteristics. The characteristic coefficients of the filters can usually be obtained in normalised lookup tables, leaving for the designer the work of sizing the passive components such that the coefficients match those given by the tables. This

process complexity further expands when the source and load sides of the filters are not impedance matched, which is usually the case for switched power converters. As a consequence, the filters require some sort of damping that is usually done using resistive elements in the filter (active damping utilising the power converter is also possible, as shown in [121]).

After obtaining the transfer function, a set of equations is solved to obtain the values of the passive components. Possibly, the set of equations does not yield a real solution for every element, thus requiring the filter designer to fine-tune component values until the desired response is approximated. Furthermore, little design flexibility is given beyond the point of obtaining a single solution to fulfil the initial requirements.

A different design process is detailed in this section. The filter design problem will be formulated as an optimisation problem for which an optimisation algorithm will be used to search for suitable parameters for the filter passive components to fulfil the design requirements.

4.2.1 Problem Definition

The proposed design approach aims to optimise the filter design regarding its frequency response and stored energy. To do so, consider the following variables: H_n is the transfer function of an nth-order filter of a topology selected by the filter designer, which has the gain frequency response given by $G_n(\omega)$. The objective frequency gain response of the filter is $G_n^*(\omega)$ and can be obtained, for example, by selecting characteristic polynomial filters such as Chebyshev or Butterworth filters. The optimisation parameters are naturally the values of the passive components of the filter. $\boldsymbol{l}$ is the set of all inductors in the filter, $\{L_1, \dots, L_{nl}\}$, with *nl* being the total number of inductors. $\boldsymbol{c}$ is the set of all capacitors in the filter, $\{C_1, \dots, C_{nc}\}$, with *nc* being the total number of capacitors. Finally, $\boldsymbol{r}$ is the set of all resistors in the filter, $\{R_1, \dots, R_{nr}\}$, with *nr* being the total number of resistors.

The optimisation process requires the determination of the gain response, $G_n(\omega)$, as a function of the $\boldsymbol{l}$, $\boldsymbol{c}$ and $\boldsymbol{r}$ parameters of the filter, $G_n(\omega, \boldsymbol{l}, \boldsymbol{c}, \boldsymbol{r})$. It is also necessary to compute the energy stored in the filter at a given nominal power, P_{nom} and nominal voltage, V_{nom}, given by $W(\boldsymbol{l}, \boldsymbol{c}, V_{nom}, P_{nom})$.

The values of the passive components are contained within bonds limited by L_{min}, L_{max}, C_{min}, C_{max}, R_{min} and R_{max}. Furthermore, the optimisation should also be constrained to filters that have a minimum power factor, $PF_{\min}$, at a given reduced power level of the converter, P_{min}, given by $PF_n(\boldsymbol{l},\boldsymbol{c},\boldsymbol{r},P_{\min})$.

The above definition results in the following formulation that aims to minimise three functions as shown in (4.20). The first, in (4.21), is a metric of the proximity of $G_n(\omega)$ to the desired response $G_n^*(\omega)$. The second, in (4.22), aims to reduce the energy stored in the filter, and thus its size.

$$\text{Minimize } \{f_1(\text{x}), f_2(\text{x})\} \tag{4.20}$$

Where:

$$f_1(\text{x}) = \int_{\omega_0}^{\omega_f} \left| G_n^*(\omega) - G_n(\omega,\boldsymbol{l},\boldsymbol{c},\boldsymbol{r}) \right| d(\log\omega) \tag{4.21}$$

$$f_2(\text{x}) = W(\boldsymbol{l},\boldsymbol{c},V_{nom},P_{nom}) \tag{4.22}$$

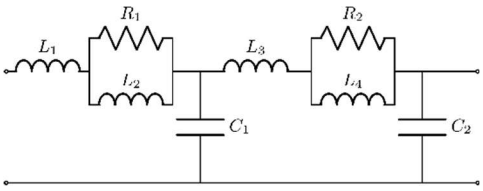
Subjected to

$$\begin{aligned} &PF_n(\boldsymbol{l},\boldsymbol{c},\boldsymbol{r},P_{\min}) \geq PF_{\min} \\ &L_{\min} \leq \boldsymbol{l}_i \leq L_{\max} \\ &C_{\min} \leq \boldsymbol{c}_i \leq C_{\max} \\ &R_{\min} \leq \boldsymbol{r}_i \leq R_{\max} \end{aligned} \tag{4.23}$$

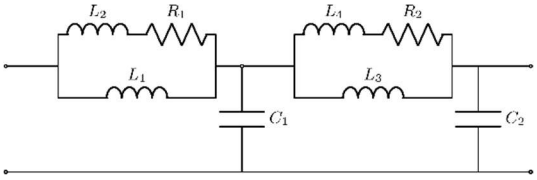
The relation in (4.23) shows the optimisation constraints related to the bound values of inductors, resistors and capacitors, as wells as the power factor constraint.

4.2.2 Sizing a 6th-order filter with passive damping

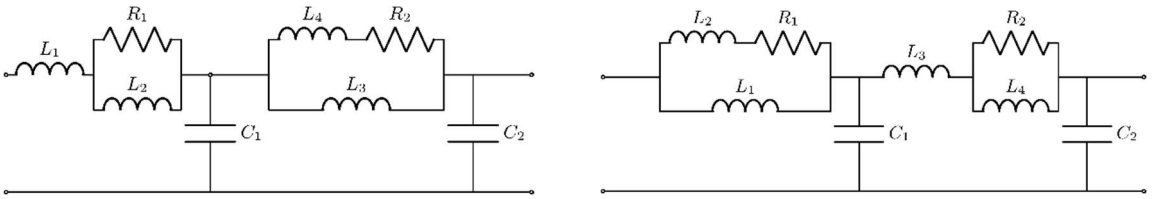
In this section, the previously outlined method will be applied to the four different filter topologies shown in Figure 4.8. All topologies use 6 reactive elements and 2 resistors for the damping of each stage.



a) Topology I



b) Topology II



c) Topology III d) Topology IV

Figure 4.8 Four different low-pass filter topologies for the input filter of the proposed SST. a) Topology I, b) Topology II, c) Topology III and d) Topology IV.

Filter Topologies Characterization

All the proposed topologies can be characterised by a 6th order transfer function (4.24), defined by ten coefficients, three for the numerator, $\begin{bmatrix} b_2 & b_1 & b_0 \end{bmatrix}$, and seven for the denominator, $\begin{bmatrix} a_6 & a_5 & a_4 & a_3 & a_2 & a_1 & a_0 \end{bmatrix}$.

$$H_n = \frac{b_2 s^2 + b_1 s + b_0}{a_6 s^6 + a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{4.24}$$

The coefficients take the values in (4.25) for the filter Topology I.

$$\begin{cases} a_6 = C_1 C_2 L_1 L_2 L_3 L_4 \\ a_5 = C_1 C_2 ((L_1 + L_2) L_3 L_4 R_1 + L_1 L_2 (L_3 + L_4) R_2) \\ a_4 = (C_1 + C_2) L_1 L_2 L_4 + (L_3 + L_4)(C_1 C_2 L_1 R_1 R_2 + C_2 L_2 + C_1 C_2 L_2 R_1 R_2) \\ a_3 = L_1 L_2 (C_1 R_2 + C_2 R_2) + L_1 L_4 (C_1 R_1 + C_2 R_1) + L_2 L_4 (C_1 R_1 + C_2 R_1 + C_2 R_2) + C_2 L_3 (L_2 R_2 + L_4 R_1) \\ a_2 = L_2 L_4 + R_1 R_2 (C_1 (L_1 + L_2) + C_2 (L_2 + L_3 + L_4) \\ a_1 = L_2 R_2 + L_4 R_1 \\ a_0 = R_1 R_2 \\ b_2 = L_2 L_4 \\ b_1 = L_2 R_2 \\ b_0 = R_1 R_2 \end{cases}$$

(4.25)

Topology II has the coefficients according to (4.26).

$$\begin{cases} a_6 = C_1C_2L_1L_2L_3L_4 \\ a_5 = C_1C_2L_1L_3(R_2L_2 + L_4R_1) \\ a_4 = C_1L_1L_2(L_3 + L_4) + C_2L_1L_2(L_3 + L_4) + C_2L_3L_4(L_1 + L_2) + C_1C_2L_1L_3R_1R_2 \\ a_3 = C_1L_1(L_2R_2 + L_3R_1 + L_4R_1) + C_2L_1(L_2R_2 + L_3R_1 + L_3R_2 + L_4R_1) + C_2L_2L_3R_2 + C_2L_3L_4R_1 \\ a_2 = L_1L_3 + L_1L_4 + L_2L_3 + L_2L_4 + R_1R_2(C_1L_1 + C_2L_1 + C_2L_3) \\ a_1 = L_1R_2 + L_2R_2 + L_3R_1 + L_4R_1 \\ a_0 = R_1R_2 \\ b_2 = L_1L_3 + L_1L_4 + L_2L_3 + L_2L_4 \\ b_1 = L_1R_2 + L_2R_2 + L_3R_1 + L_4R_1 \\ b_0 = R_1R_2 \end{cases}$$

(4.26)

Topology III has the coefficients according to (4.27).

$$\begin{cases} a_6 = C_1C_2L_1L_2L_3L_4 \\ a_5 = C_1C_2L_3(L_1L_2R_2 + L_1L_4R_1 + L_2L_4R_1) \\ a_4 = C_1L_1L_2(L_3 + L_4) + C_2L_1L_2(L_3 + L_4) + C_2L_2L_3L_4 + C_1C_2L_3R_1R_2(L_1 + L_2) \\ a_3 = C_1R_1(L_1 + L_2)(L_3 + L_4) + C_2R_1(L_3(L_1 + L_2) + L_4(L_1 + L_2 + L_3)) + L_2R_2(C_1L_1 + C_2(L_1 + L_3)) \\ a_2 = L_2L_3 + L_2L_4 + C_1R_1R_2(L_1 + L_2) + C_2R_1R_2(L_1 + L_2 + L_3) \\ a_1 = L_2R_2 + L_3R_1 + L_4R_1 \\ a_0 = R_1R_2 \\ b_2 = L_2L_3 + L_2L_4 \\ b_1 = L_2R_2 + L_3R_1 + L_4R_1 \\ b_0 = R_1R_2 \end{cases}$$

(4.27)

Topology IV has the coefficients according to (4.28)

$$\begin{cases} a_6 = C_1C_2L_1L_2L_3L_4 \\ a_5 = C_1C_2L_1(L_3L_4R_1 + L_2R_2(L_3 + L_4)) \\ a_4 = C_2L_4(L_2L_3 + L_1(L_2 + L_3)) + C_1L_1(L_2L_4 + C_2R_1R_2(L_3 + L_4)) \\ a_3 = C_2L_4R_1(L_1 + L_3) + C_2R_2(L_2(L_3 + L_4) + L_1(L_2 + L_3 + L_4)) + C_1L_1(L_4R_1 + L_2R_2) \\ a_2 = L_2L_4 + C_2R_1R_2(L_3 + L_4) + L_1(L_4 + R_1R_2(C_1 + C_2)) \\ a_1 = L_4R_1 + R_2(L_1 + L_2) \\ a_0 = R_1R_2 \\ b_2 = L_1L_4 + L_2L_4 \\ b_1 = L_1R_2 + L_2R_2 + L_4R_1 \\ b_0 = R_1R_2 \end{cases} \quad (4.28)$$

The above-described transfer functions will be used to compute the frequency gain response of the filter $G_n(\omega)$.

The energy stored in each filter inductor is computed using (4.29).

$$W_{Li} = L_i I_{Li}^2 \quad , \quad i \in \{1,2,3,4\} \tag{4.29}$$

The current I_{Li} is the root mean square (RMS) current that crosses the i^{th} inductor. An approximation for this value can be obtained from the nominal current of the filter and the reactance of each filter component considering only the first harmonic component of the currents. The currents for each inductor in each topology are in (4.30), (4.31), (4.32) and (4.33) for topologies I, II, III and IV, respectively, where X_1, X_2, X_3 and X_4 are the reactance of each inductor at the fundamental frequency.

$$\begin{cases} I_{L1} = I_{nom} \\ I_{L2} = I_{nom} \dfrac{R_1}{\sqrt{R_1^2 + X_{L2}^2}} \\ I_{L3} = I_{nom} \\ I_{L4} = I_{nom} \dfrac{R_2}{\sqrt{R_2^2 + X_{L4}^2}} \end{cases} \tag{4.30}$$

$$\begin{cases} I_{L1} = I_{nom} \dfrac{\sqrt{R_1^2 + X_{L2}^2}}{\sqrt{R_1^2 + (X_{L2} + X_{L1})^2}} \\ I_{L2} = I_{nom} \dfrac{X_{L1}}{\sqrt{R_1^2 + (X_{L2} + X_{L1})^2}} \\ I_{L3} = I_{nom} \dfrac{\sqrt{R_2^2 + X_{L4}^2}}{\sqrt{R_2^2 + (X_{L3} + X_{L4})^2}} \\ I_{L4} = I_{nom} \dfrac{X_{L3}}{\sqrt{R_2^2 + (X_{L3} + X_{L4})^2}} \end{cases} \tag{4.31}$$

$$\begin{cases} I_{L1} = I_{nom} \\ I_{L2} = I_{nom} \dfrac{R_1}{\sqrt{R_1^2 + X_{L2}^2}} \\ I_{L3} = I_{nom} \dfrac{\sqrt{R_2^2 + X_{L4}^2}}{\sqrt{R_2^2 + (X_{L3} + X_{L4})^2}} \\ I_{L4} = I_{nom} \dfrac{X_{L3}}{\sqrt{R_2^2 + (X_{L3} + X_{L4})^2}} \end{cases} \tag{4.32}$$

$$\begin{cases} I_{L1} = I_{nom} \dfrac{\sqrt{R_1^2 + X_{L2}^2}}{\sqrt{R_1^2 + (X_{L2} + X_{L1})^2}} \\ I_{L2} = I_{nom} \dfrac{X_{L1}}{X_{L1} + \sqrt{R_1^2 + X_{L2}^2}} \\ I_{L3} = I_{nom} \\ I_{L4} = I_{nom} \dfrac{R_2}{\sqrt{R_2^2 + X_{L4}^2}} \end{cases} \tag{4.33}$$

The energy stored in each capacitor is given by (4.34) where V_j is the RMS voltage across the capacitor, which can be approximated directly by the nominal input voltage.

$$W_{Cj} = V_j^2 C_j \quad , \; i \in \{1,2\} \tag{4.34}$$

The total energy, W_t, can then be computed as per (4.35).

$$W_t = \sum_i W_{Li} + \sum_j W_{Cj} \tag{4.35}$$

Reference Transfer Function and Preliminary Results

The reference frequency gain response, $G_n^*(\omega)$, was obtained using the common Chebyshev type I filter [122] whose gain response is given by (4.36), where ε is the ripple factor (which sets the bandpass gain and ripple), ω_0 is the cut-off frequency and T_n is the Chebyshev polynomial of order n [122].

$$G_n^*(\omega) = \frac{1}{\sqrt{1+\varepsilon^2 T_n^2(\omega/\omega_0)}} \tag{4.36}$$

The values of the passband ripple factor, the cut-off frequency and the filter order were set respectively to $\varepsilon = 0.1$, ω_o = 10 kHz and $n = 4$ with the resulting gain response shown in the red trace of Figure 4.9. Since the Chebyshev type I filter transfer function is composed of only poles, the filter order is selected to 4 to match the expected final roll-off rate of the proposed filter topologies (which have 6 poles and 2 zeros).

In order to set some baseline reference filter designs for each topology, the optimisation problem was solved considering only the minimization of $f_1(x)$ as per (4.21). In other words, this meant minimising only the difference between the gain responses of each filter topology, disregarding the stored energy in the filter. The results of that optimisation process are also traced in Figure 4.9, showing good approximations to $G_n^*(\omega)$ for any of the filter topologies.

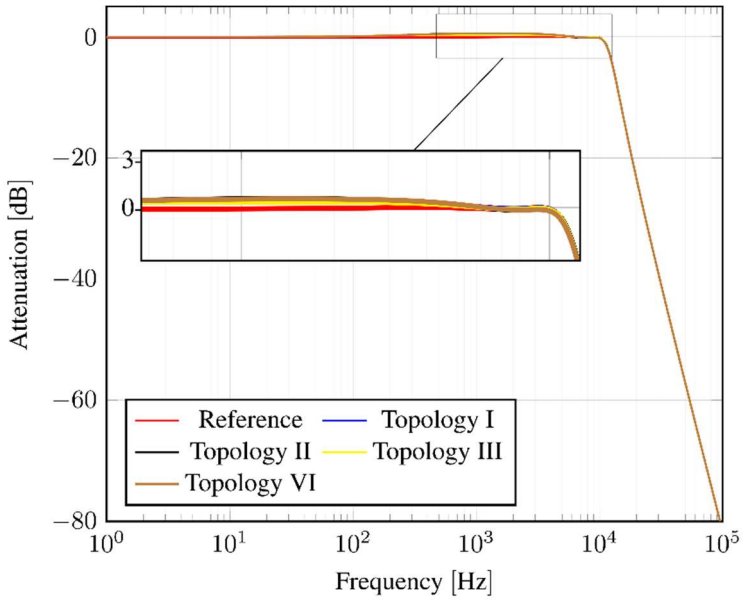


Figure 4.9 Frequency response of the reference function $G_n^*(\omega)$ in the red trace and the gain frequency response of the proposed topologies I, II, III and IV in blue, black, yellow and brown, respectively.

When the focus of the filter design is only characterised by its frequency response, this method suffices to obtain the sizing of the filter components, which for high-order unmatched filter designs can be cumbersome to solve analytically.

To set a baseline for the energy stored in the filter, the resulting stored energies in each topology, for a nominal voltage, V_{nom}, of 230 V and a nominal current, i_{nom}, of 22 A at an operating frequency of 50 Hz were computed, and the results are presented in Table 4.3.

Table 4.3 Filter's stored energy for Topologies I, II, III and IV using the baseline method described in this section.

	Topology I	Topology II	Topology III	Topology VI
Energy Stored [J]	4.80	4.71	4.96	4.95

The resulting energies will be used as a comparison point for the results obtained in the multi-objective optimisation.

Multi-objective Optimization Results

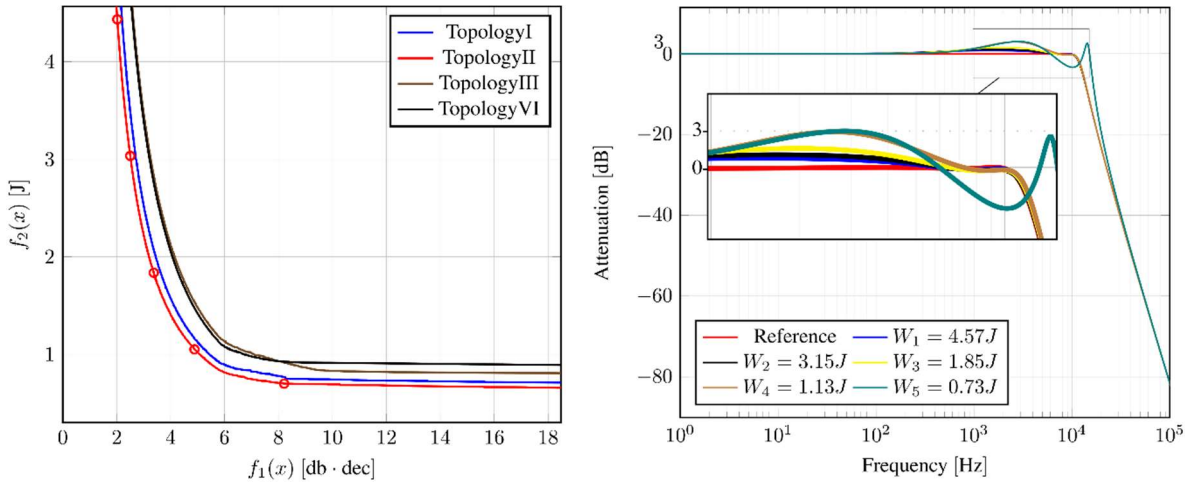
The optimisation results used the same reference gain frequency response as in (4.36), with the same parameters as in the previous section.

The optimisation was done for each of the four topologies individually, which yielded the Pareto fronts depicted in Figure 4.10 a), where the results for topology II (in the red trace)

dominated the remaining results. Five different points of the Pareto front of the results relative to topology II were plotted, regarding their gain frequency response, in Figure 4.10 b).

The main conclusion from applying the proposed method to the four filter topologies selected is that Topology II dominates the solution space and is preferred throughout the entire range of approximations and stored filter energies.

The results highlighted in Figure 4.10 b) are all satisfactory regarding their gain frequency response, with the result with minimum stored energy (green trace) having a slight amplification near the cut-off frequency. For that reason, the filter sizing depicted in the brown trace with 1.13 J was selected, which represents a reduction of 3.58 J in the stored energy compared to the baseline values. The chosen filter parameters are shown in Table 4.4.



a) b)

Figure 4.10 a) Depiction of the Pareto fronts for topologies I, II, III and IV in blue, red, brown, and black, respectively. b) Gain frequency response of 5 different solution of topology II (respectively marked in a)).

Table 4.4 Selected Filter Components for Topology II

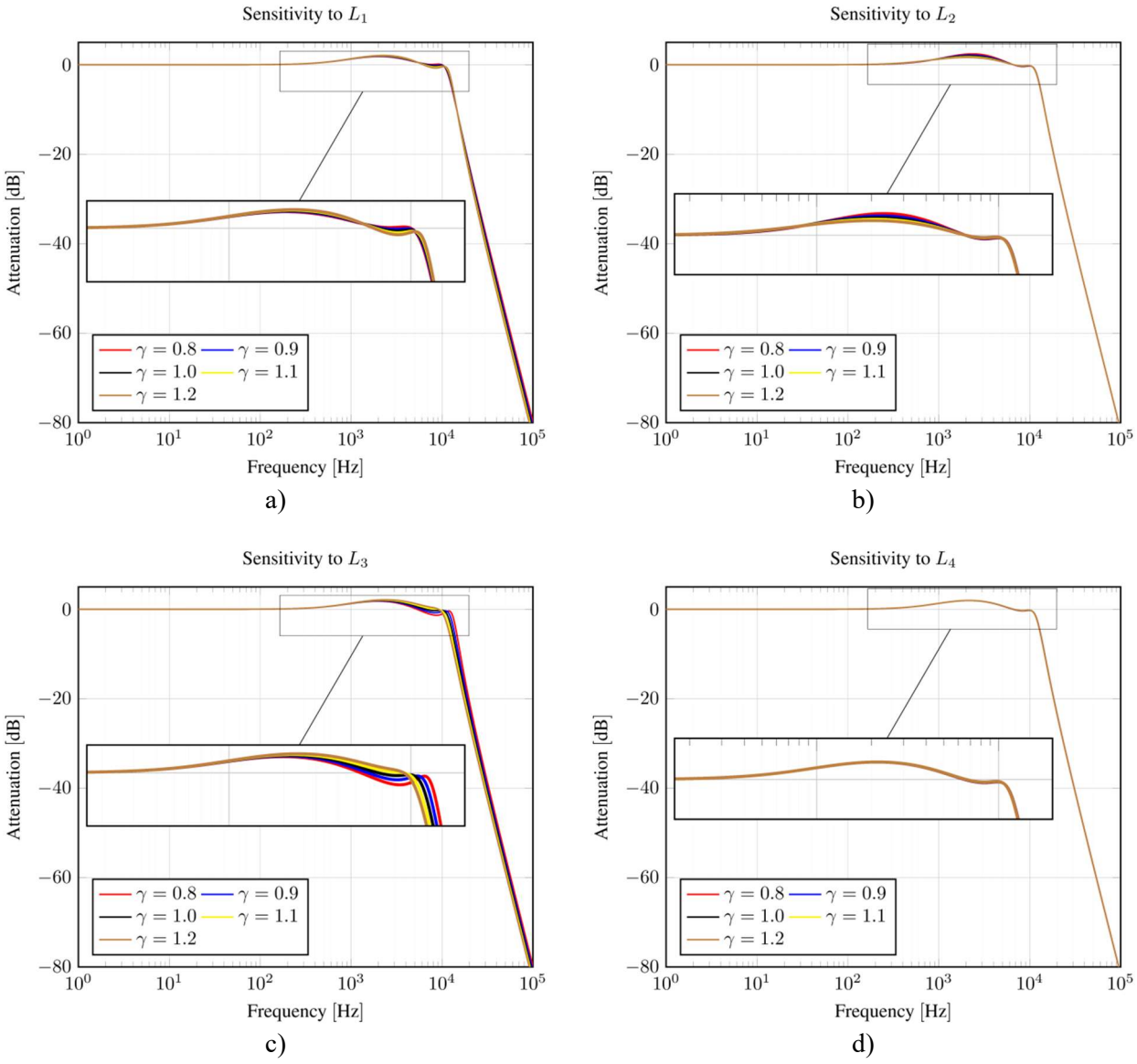
	L_1	L_2	L_3	L_4	R_1	R_2	C_1	C_2
Value	$1.03mH$	$89.5\mu H$	$210.0\mu H$	$5\mu H$	5.1 Ω	4.5Ω	$3.4\mu F$	$4.0\mu F$

Sensitivity Analysis

As a consequence of the use of higher-order filters, the sensitivity of each filter component sizing in the filter frequency response is difficult, if possible, to compute analytically. As such, to understand the influence of each component in the filter's gain frequency response each of

the component sizing was scaled by a factor γ and the resulting frequency response was computed for γ equal to 0.8, 0.9, 1.0, 1.1 and 1.2 with the results presented in Figure 4.11.

This sensitivity analysis revealed that both the capacitors C_1 and C_2 along with the inductor L_3 and the resistor R_1 are the most sensitive sizing values. Despite the presented frequency responses being all acceptable, this analysis hides the potential impact of the combined component sensitivity in the transfer function.



a) b)

c) d)

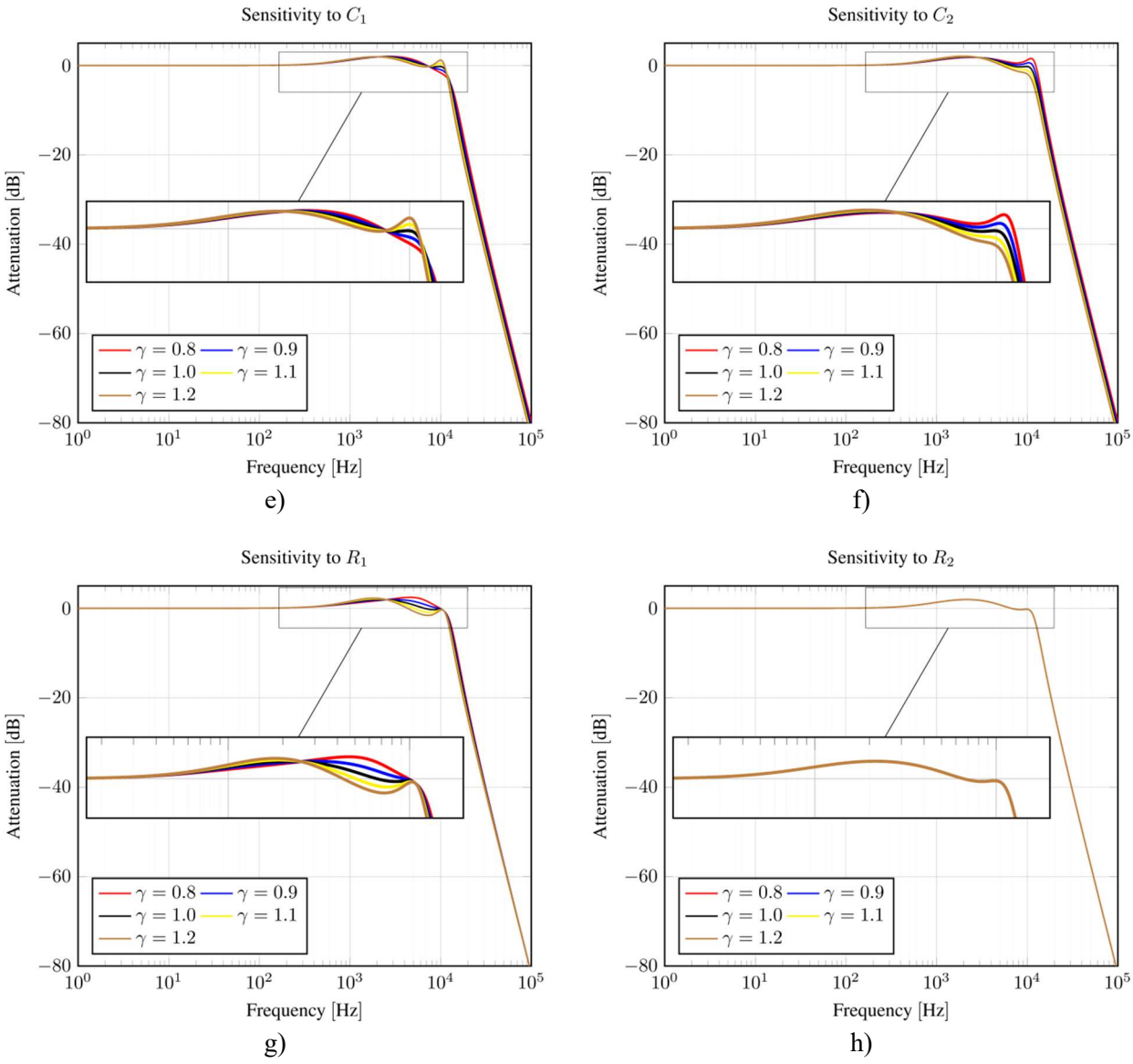


Figure 4.11 Sensitivity analysis to the optimized Topology III filter gain frequency response where each component is individually scaled by 5 different values of γ. a) Sensitivity to L_1; b) Sensitivity to L_2; c) Sensitivity to L_3; d) Sensitivity to L_4; e) Sensitivity to C_1; f) Sensitivity to C_2; g) Sensitivity to R_1; h) Sensitivity to R_2.

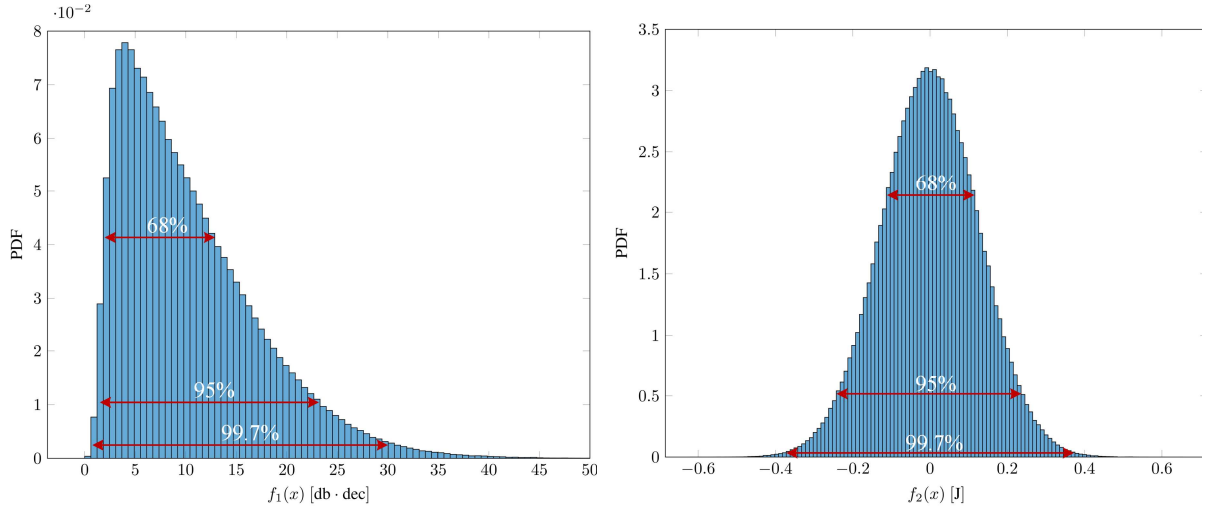
To address this problem, a Monte Carlo simulation is performed, where each component value is obtained by a random number that obeys a normal distribution. The expected value is the sizing value from the optimisation process, and the standard deviation is obtained from the component tolerances such that 95% of their values are within a tolerance of 5% for resistors, 20% for capacitors and 30% for the inductors of their original expected value.

For each filter sizing, two components are evaluated: 1) A metric of the difference of the gain frequency response compared to the initially sized filter, for which the function in (4.21) can

be repurposed; 2) The difference between the energy stored in the filter compared to the initially sized filter.

The Monte Carlo simulation was repeated with increasing population sizes until the variance of the above-described metrics stabilised, indicating that the sampled population size is representative of the entire population of possible filters with the layered conditions. This returned a population size of 10^6 filters with slightly different components.

The obtained probability density functions for the two proposed metrics are presented in Figure 4.12 a) and b) for the frequency response and stored energy, respectively. These results show that while the stored energy is expected to remain the same as the one sized by the optimisation algorithm, with a 95% probability of having a deviation lower than 0.25 J, the frequency response is expected to have a slight difference of about 5 dB·dec, which was observed to be small. More importantly, despite the worst case having a deviation of about 93 dB·dec, its likelihood is extremely low in the order of 0.001%, and it is expected that 95% of the possible filters remain within a 22 dB·dec difference of the original filter which was also observed to be sufficiently small so that their frequency responses are similar.



a) b)

Figure 4.12 Probability density functions of the metrics of a) closeness to the original frequency response and b) the stored energy difference to the originally optimized filter.

4.3 Control method for the Matrix Converter based SST

This section formalises a control strategy for the proposed SST converter using the χ converter equivalent discussed in Section 3.1.1 combined with the filter topology selected by the optimisation process in Section 4.2.2.

A schematic overview of the full control system can be seen in

Figure 4.13. The leakage tolerant commutation method detailed in section 3.2 allows for the safe commutation of both conversion stages while ensuring that the leakage energy of the transformer is recirculated. The modulation method detailed in section 3.1 receives the control action for a single matrix converter and unfolds it as two control actions for both the primary and secondary converter using the available redundancy to select vectors that minimise the transformer flux. This modulator is fed by a model predictive current controller whose current references are given by a non-linear voltage controller. The description of these controllers is the object of study in this section.

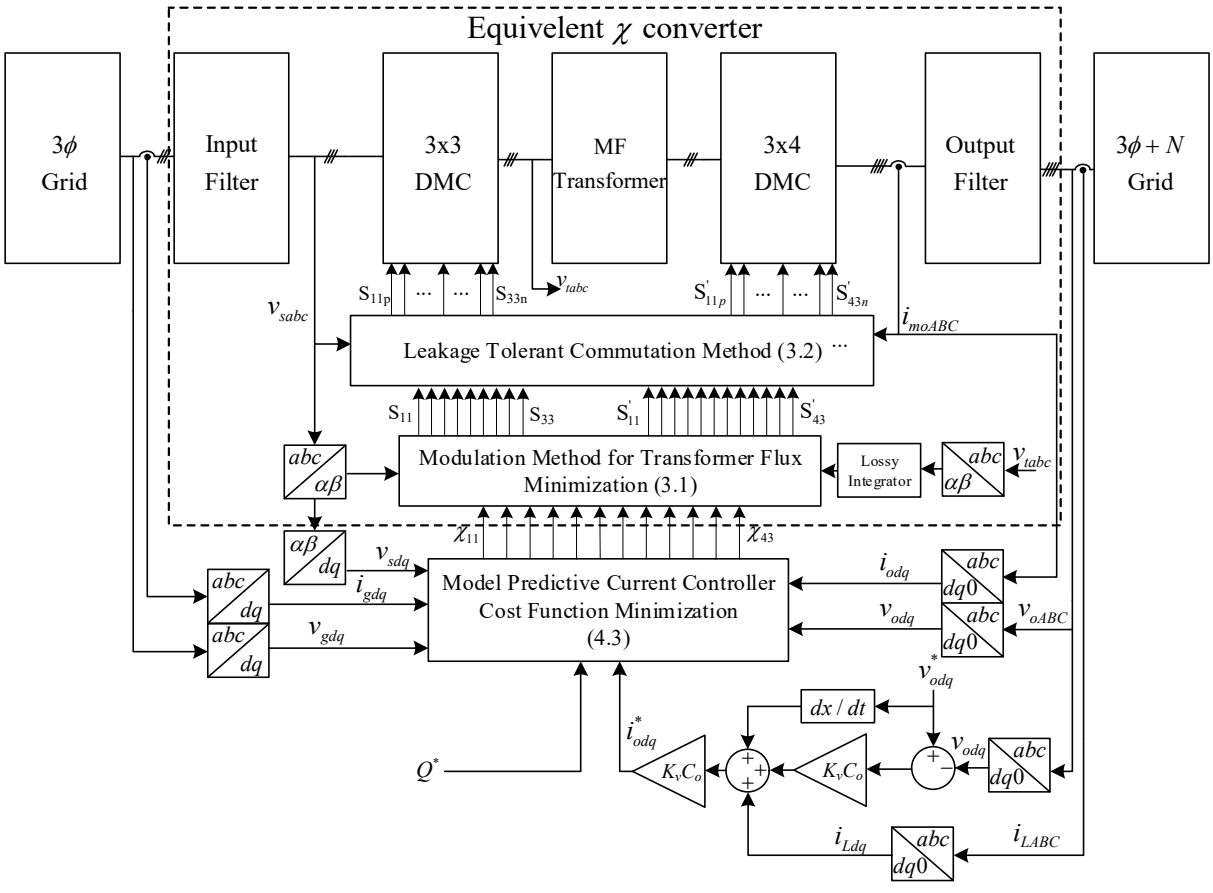


Figure 4.13 Schematization of the full control scheme operation, including the leakage tolerant commutation, the modulation method, the MPC current controller and the non-linear voltage controller.

Ultimately, what the modulation method enables is that the SST can be controlled as a single 3x4 DMC named χ equivalent converter, as such the controllers can be sized for the system depicted in Figure 4.14.

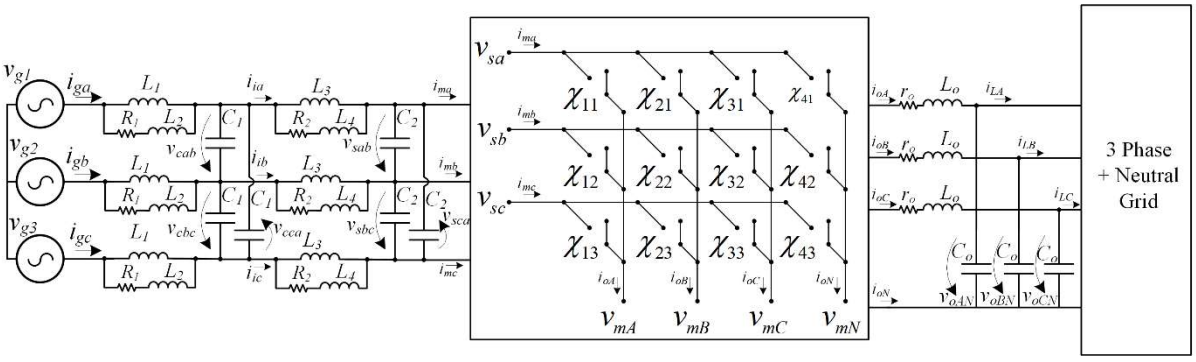


Figure 4.14 Depiction of the proposed SST topology with input and output filters using the χ equivalent converter for the combination of both matrix converter and transformer.

The input filter is composed by two sequential stages with two inductors, one capacitor and one damping resistor, $\{L_1, L_2, L_3, L_4, R_1, R_2, C_1, C_2\}$. The capacitors are delta connected and the and the L_2 and L_4 inductors are in series with the damping resistors R_1 and R_2, respectively, to improve the high frequency attenuation.

The control strategy is composed of an MPC current controller with a non-linear on-load voltage control for the output capacitor voltages. To obtain the control equations, the following section will model the proposed input and output filter dynamics followed by a discretisation that will allow the prediction of the relevant quantities as a function of the different converter vectors.

4.3.1 Modelling of the Matrix Converter-Based SST

In order to obtain suitable prediction equations has described in (2.28) it is necessary to obtain the equations that describe the dynamics of the input and output filter state variables. This will be done considering the χ approximation of the combination of both matrix converters and the MF/HF transformer.

Modelling of the input filter

Considering a set of sinusoidal voltages composed by $[v_{ga}\ v_{gb}\ v_{gc}]^T$ depicted in Figure 4.14, and inspecting the voltage loop composed by the grid voltages, inductors L_1 and the capacitors C_1 it is possible to obtain (4.37).

$$\begin{cases} v_{ga} = L_1 \dfrac{di_{l1a}}{dt} + v_{cab} - L_1 \dfrac{di_{l1b}}{dt} + v_{gb} \\ v_{gb} = L_1 \dfrac{di_{l1b}}{dt} + v_{cbc} - L_f \dfrac{di_{l1c}}{dt} + v_{gc} \\ v_{gc} = L_1 \dfrac{di_{l1c}}{dt} + v_{cca} - L_1 \dfrac{di_{l1a}}{dt} + v_{ga} \end{cases} \Leftrightarrow \begin{cases} v_{ga} - v_{gb} = L_1 \dfrac{di_{l1a}}{dt} - L_1 \dfrac{di_{l1b}}{dt} + v_{cab} \\ v_{gb} - v_{gc} = L_1 \dfrac{di_{l1b}}{dt} - L_1 \dfrac{di_{l1c}}{dt} + v_{cbc} \\ v_{gc} - v_{ga} = L_1 \dfrac{di_{l1c}}{dt} - L_1 \dfrac{di_{l1a}}{dt} + v_{cca} \end{cases} \quad (4.37)$$

With some mathematical manipulation and rewriting the equation in a matrix form (4.37) can be manipulated to (4.38).

$$\begin{bmatrix} \dfrac{di_{l1a}}{dt} \\ \dfrac{di_{l1b}}{dt} \\ \dfrac{di_{l1c}}{dt} \end{bmatrix} = \begin{bmatrix} -\dfrac{2}{3L_1} & -\dfrac{1}{3L_1} & 0 \\ 0 & -\dfrac{2}{3L_1} & -\dfrac{1}{3L_1} \\ -\dfrac{1}{3L_1} & 0 & -\dfrac{2}{3L_1} \end{bmatrix} \begin{bmatrix} v_{cab} \\ v_{cbc} \\ v_{cca} \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_1} & 0 & 0 \\ 0 & \dfrac{1}{L_1} & 0 \\ 0 & 0 & \dfrac{1}{L_1} \end{bmatrix} \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} \quad (4.38)$$

A similar process can be made to obtain the dynamics of the currents across the L_2 inductors, considering this time the voltage loop across L_2 and R_1 as opposed to L_1, the equations describing this voltage loop can be seen in (4.39).

$$\begin{cases} v_{ga} = L_2 \dfrac{di_{l2a}}{dt} + R_1 i_{l2a} + v_{cab} - L_2 \dfrac{di_{l2b}}{dt} - R_1 i_{l2b} + v_{gb} \\ v_{gb} = L_2 \dfrac{di_{l2b}}{dt} + R_1 i_{l2b} + v_{cbc} - L_2 \dfrac{di_{l2c}}{dt} - R_1 i_{l2c} + v_{gc} \\ v_{gc} = L_2 \dfrac{di_{l2c}}{dt} + R_1 i_{l2c} + v_{cca} - L_2 \dfrac{di_{l2a}}{dt} - R_1 i_{l2a} + v_{ga} \end{cases} \Rightarrow \begin{cases} v_{ga} - v_{gb} = L_2 \dfrac{di_{l2a}}{dt} + R_1 i_{l2a} - L_2 \dfrac{di_{l2b}}{dt} - R_1 i_{l2b} + v_{cab} \\ v_{gb} - v_{gc} = L_2 \dfrac{di_{l2b}}{dt} + R_1 i_{l2b} - L_2 \dfrac{di_{l2c}}{dt} - R_1 i_{l2c} + v_{cbc} \\ v_{gc} - v_{ga} = L_2 \dfrac{di_{l2c}}{dt} + R_1 i_{l2c} - L_2 \dfrac{di_{l2a}}{dt} - R_1 i_{l2a} + v_{cca} \end{cases}$$

(4.39)

Once again, manipulating (4.39) the dynamics of the currents in the inductors L_2 are given by (4.40).

$$\begin{bmatrix} \frac{di_{l2a}}{dt} \\ \frac{di_{l2b}}{dt} \\ \frac{di_{l2c}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{2}{3L_2} & -\frac{1}{3L_2} & 0 \\ 0 & -\frac{2}{3L_2}v & -\frac{1}{3L_2} \\ -\frac{1}{3L_2} & 0 & -\frac{2}{3L_2} \end{bmatrix} \begin{bmatrix} v_{cab} \\ v_{cbc} \\ v_{cca} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_2} & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & \frac{1}{L_2} \end{bmatrix} \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} + \begin{bmatrix} -\frac{R_1}{L_2} & 0 & 0 \\ 0 & -\frac{R_1}{L_2} & 0 \\ 0 & 0 & -\frac{R_1}{L_2} \end{bmatrix} \begin{bmatrix} i_{l2a} \\ i_{l2b} \\ i_{l2c} \end{bmatrix}$$

(4.40)

To obtain the dynamics of capacitors C_1 voltages, the currents at their nodes can be inspected and are given by (4.41).

$$\begin{cases} i_{ga} = C_1 \frac{dv_{cab}}{dt} - C_1 \frac{dv_{cca}}{dt} + i_{ia} \\ i_{gb} = C_1 \frac{dv_{cbc}}{dt} - C_1 \frac{dv_{cab}}{dt} + i_{ib} \\ i_{gc} = C_1 \frac{dv_{cca}}{dt} - C_1 \frac{dv_{cbc}}{dt} + i_{ic} \end{cases} \tag{4.41}$$

Using (4.41) it is possible to write the dynamics of the C_1 capacitor voltages as per (4.42).

$$\begin{bmatrix} \frac{dv_{cab}}{dt} \\ \frac{dv_{cbc}}{dt} \\ \frac{dv_{cca}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{2}{3C_1} & -\frac{1}{3C_1} \\ -\frac{1}{3C_1} & 0 & -\frac{2}{3C_1} \\ -\frac{2}{3C_1} & -\frac{1}{3C_1} & 0 \end{bmatrix} \begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} + \begin{bmatrix} 0 & \frac{2}{3C_1} & \frac{1}{3C_1} \\ \frac{1}{3C_1} & 0 & \frac{2}{3C_1} \\ \frac{2}{3C_1} & \frac{1}{3C_1} & 0 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{4.42}$$

The dynamics of the currents across the L_1 and L_2 inductors as well as the voltages in the C_1 capacitors can be obtained in a set of dq coordinates synchronous with the input grid voltages. They can be attained by using the suitable transform matrixes described in (1.1) and (1.5). Furthermore consider that $\mathbf{X_{\alpha\beta}} = \left(\mathbf{C}^{\mathrm{T}}\,\mathbf{K}\,\mathbf{C}\right)\left(\mathbf{C}^{\mathrm{T}}\mathbf{X_{abc}}\right)$ this is possible since $\mathbf{C}\,\mathbf{C}^{\mathrm{T}} = \mathbf{I}$ where $\mathbf{I}$ is the appropriate sized identity matrix, the same is also true for the dq transform and $\mathbf{X_{dq}} = \left(\mathbf{D}^{\mathbf{T}}\,\mathbf{K}\,\mathbf{D}\right)\left(\mathbf{D}^{\mathbf{T}}\mathbf{X_{\alpha b}}\right)$. The resulting dynamics in dq for (4.38), (4.40) and (4.42) can respectively be found in (4.43), (4.44) and (4.45) where the ω cross terms were neglected.

$$\begin{bmatrix} \frac{di_{l1d}}{dt} \\ \frac{di_{l1q}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{2L_1} & -\frac{1}{2\sqrt{3}L_1} \\ \frac{1}{2\sqrt{3}L_1} & -\frac{1}{2L_1} \end{bmatrix} \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_1} \end{bmatrix} \begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix} \tag{4.43}$$

$$\begin{bmatrix} \frac{di_{l2d}}{dt} \\ \frac{di_{l2q}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{2L_2} & -\frac{1}{2\sqrt{3}L_2} \\ \frac{1}{2\sqrt{3}L_2} & -\frac{1}{2L_2} \end{bmatrix} \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_2} & 0 \\ 0 & \frac{1}{L_2} \end{bmatrix} \begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix} + \begin{bmatrix} -\frac{R_1}{L_2} & 0 \\ 0 & -\frac{R_1}{L_2} \end{bmatrix} \begin{bmatrix} i_{l2d} \\ i_{l2q} \end{bmatrix} \tag{4.44}$$

$$\begin{bmatrix} \frac{dv_{cd}}{dt} \\ \frac{dv_{cq}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{1}{2C_1} & -\frac{1}{2\sqrt{3}C_1} \\ \frac{1}{2\sqrt{3}C_1} & \frac{1}{2C_1} \end{bmatrix} \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} + \begin{bmatrix} -\frac{1}{2C_1} & \frac{1}{2\sqrt{3}C_1} \\ -\frac{1}{2\sqrt{3}C_1} & -\frac{1}{2C_1} \end{bmatrix} \begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix} \tag{4.45}$$

A closer inspection of the filter topology in Figure 4.14 shows that the input filter can be divided into two similar stages. As such the dynamics for the currents in the inductors L_3 and L_4 as well as the dynamics for the voltages in the capacitors C_2 can simply be directly deduced from (4.43), (4.44) and (4.45) respectively to (4.46), (4.47) and (4.48).

$$\begin{bmatrix} \frac{di_{l3d}}{dt} \\ \frac{di_{l3q}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{2L_3} & -\frac{1}{2\sqrt{3}L_3} \\ \frac{1}{2\sqrt{3}L_3} & -\frac{1}{2L_3} \end{bmatrix} \begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_3} & 0 \\ 0 & \frac{1}{L_3} \end{bmatrix} \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} \tag{4.46}$$

$$\begin{bmatrix} \frac{di_{l4d}}{dt} \\ \frac{di_{l4q}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{2L_4} & -\frac{1}{2\sqrt{3}L_4} \\ \frac{1}{2\sqrt{3}L_4} & -\frac{1}{2L_4} \end{bmatrix} \begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_4} & 0 \\ 0 & \frac{1}{L_4} \end{bmatrix} \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} + \begin{bmatrix} -\frac{R_2}{L_4} & 0 \\ 0 & -\frac{R_2}{L_4} \end{bmatrix} \begin{bmatrix} i_{l4d} \\ i_{l4q} \end{bmatrix} \tag{4.47}$$

$$\begin{bmatrix} \frac{dv_{sd}}{dt} \\ \frac{dv_{sq}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{1}{2C_2} & -\frac{1}{2\sqrt{3}C_2} \\ \frac{1}{2\sqrt{3}C_2} & \frac{1}{2C_2} \end{bmatrix} \begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix} + \begin{bmatrix} -\frac{1}{2C_2} & \frac{1}{2\sqrt{3}C_2} \\ -\frac{1}{2\sqrt{3}C_2} & -\frac{1}{2C_2} \end{bmatrix} \begin{bmatrix} i_{md} \\ i_{mq} \end{bmatrix} \tag{4.48}$$

Finally, the dynamics of the grid currents can directly be given by

$$\begin{bmatrix} \frac{di_{gd}}{dt} \\ \frac{di_{gq}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{di_{l1d}}{dt} \\ \frac{di_{l1q}}{dt} \end{bmatrix} + \begin{bmatrix} \frac{di_{l2d}}{dt} \\ \frac{di_{l2q}}{dt} \end{bmatrix} \tag{4.49}$$

Modelling of the output filter

By inspecting the output voltage loops, it is possible to write the dynamics of the currents at the output converter currents as per (4.50).

$$\begin{cases} -v_{mAN} + L_o \dfrac{di_{oa}}{dt} + r_o i_{oa} + v_{oAN} = 0 \\ -v_{mBN} + L_o \dfrac{di_{oa}}{dt} + r_o i_{ob} + v_{oBN} = 0 \\ -v_{mCN} + L_o \dfrac{di_{oc}}{dt} + r_o i_{oc} + v_{oCN} = 0 \end{cases} \Rightarrow \begin{cases} \dfrac{di_{oa}}{dt} = \dfrac{r_o}{L_o} i_{oa} + \dfrac{1}{L_o} v_{oAN} - \dfrac{1}{L_o} v_{mAN} \\ \dfrac{di_{ob}}{dt} = \dfrac{r_o}{L_o} i_{ob} + \dfrac{1}{L_o} v_{oBN} - \dfrac{1}{L_o} v_{mBN} \\ \dfrac{di_{oc}}{dt} = \dfrac{r_o}{L_o} i_{oc} + \dfrac{1}{L_o} v_{oCN} - \dfrac{1}{L_o} v_{mCN} \end{cases} \tag{4.50}$$

The dynamics of the output currents in (4.50) can be written in dq coordinates by considering the same reference frame synchronous with the input grid voltages resulting in the relation in (4.51).

$$\begin{bmatrix} \dfrac{di_{od}}{dt} \\ \dfrac{di_{oq}}{dt} \\ \dfrac{di_{o0}}{dt} \end{bmatrix} = \frac{r_o}{L_o} \begin{bmatrix} i_{od} \\ i_{oq} \\ i_{o0} \end{bmatrix} + \frac{1}{L_o} \begin{bmatrix} v_{od} \\ v_{oq} \\ v_{o0} \end{bmatrix} - \frac{1}{L_o} \begin{bmatrix} v_{md} \\ v_{mq} \\ v_{m0} \end{bmatrix} \tag{4.51}$$

The summation of the currents at the output capacitor nodes results in the relation in (4.52).

$$\begin{cases} i_{oA} = i_{LA} + C_o \dfrac{dv_{oAN}}{dt} \\ i_{oB} = i_{LB} + C_o \dfrac{dv_{oBN}}{dt} \\ i_{oC} = i_{LC} + C_o \dfrac{dv_{oBN}}{dt} \end{cases} \tag{4.52}$$

The dynamics of the output capacitor voltages in a dq coordinate reference frame synchronous with the input voltages can be given by (4.53).

$$\begin{bmatrix} \dfrac{dv_{od}}{dt} \\ \dfrac{dv_{oq}}{dt} \\ \dfrac{dv_{o0}}{dt} \end{bmatrix} = \frac{1}{C_o} \begin{bmatrix} i_{od} \\ i_{oq} \\ i_{o0} \end{bmatrix} - \frac{1}{C_o} \begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{bmatrix} \tag{4.53}$$

4.3.2 Model Predictive Control of the SST input and output currents

Prediction of the input grid current

The dynamics of the input grid current can be written as the sum of the dynamics of currents i_{l1} and i_{l2} as per (4.54)

$$\begin{bmatrix} \frac{di_{gd}}{dt} \\ \frac{di_{gq}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{di_{l1d}}{dt} \\ \frac{di_{l1q}}{dt} \end{bmatrix} + \begin{bmatrix} \frac{di_{l2d}}{dt} \\ \frac{di_{l2q}}{dt} \end{bmatrix} \tag{4.54}$$

A prediction for the grid currents can be written using the Euler Backward method where the discretisation period is given by T_s as shown in (4.55).

$$\begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}_{k+1} = \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}_{k} + T_s \begin{bmatrix} \frac{di_{gd}}{dt} \\ \frac{di_{gq}}{dt} \end{bmatrix}_{k+1} = \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}_{k} + T_s \begin{bmatrix} \frac{di_{l1d}}{dt} \\ \frac{di_{l1q}}{dt} \end{bmatrix}_{k+1} + T_s \begin{bmatrix} \frac{di_{l2d}}{dt} \\ \frac{di_{l2q}}{dt} \end{bmatrix}_{k+1} \tag{4.55}$$

Replacing (4.43) and (4.44) in (4.55) and simplifying results in the relation in (4.56).

$$\begin{aligned} \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}_{k+1} = \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}_{k} + \begin{bmatrix} -T_s \frac{L_1+L_2}{2L_1L_2} & -T_s \frac{L_1+L_2}{2\sqrt{3}L_1L_2} \\ T_s \frac{L_1+L_2}{2\sqrt{3}L_1L_2} & -T_s \frac{L_1+L_2}{2L_1L_2} \end{bmatrix} \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix}_{k+1} + \\ + \begin{bmatrix} T_s \frac{L_1+L_2}{L_1L_2} & 0 \\ 0 & T_s \frac{L_1+L_2}{L_1L_2} \end{bmatrix} \begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix}_{k+1} + \begin{bmatrix} -T_s \frac{R_1}{L_2} & 0 \\ 0 & -T_s \frac{R_1}{L_2} \end{bmatrix} \begin{bmatrix} i_{l2d} \\ i_{l2q} \end{bmatrix}_{k+1} \end{aligned} \tag{4.56}$$

Equation (4.56) depends on the measurement of the grid current and the predictions of: the grid voltages $\left[v_{gd}\ v_{gq}\right]^T$; the C_1 capacitor voltages $\left[v_{cd} v_{cq}\right]^T$; and the L_2 inductor currents $\left[i_{l2d}\ i_{l2q}\right]^T$.

By once again using the Euler Backward method it is possible to obtain a prediction for $\left[i_{l2d}\ i_{l2q}\right]^T_{k+1}$ as per (4.57).

$$\begin{bmatrix} i_{l2d} \\ i_{l2q} \end{bmatrix}_{k+1} = \begin{bmatrix} i_{l2d} \\ i_{l2q} \end{bmatrix}_{k} + \begin{bmatrix} -\frac{1}{2L_2} & -\frac{1}{2\sqrt{3}L_2} \\ \frac{1}{2\sqrt{3}L_2} & -\frac{1}{2L_2} \end{bmatrix} \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix}_{k+1} + \begin{bmatrix} \frac{1}{L_2} & 0 \\ 0 & \frac{1}{L_2} \end{bmatrix} \begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix}_{k+1} + \begin{bmatrix} -\frac{R_1}{L_2} & 0 \\ 0 & -\frac{R_1}{L_2} \end{bmatrix} \begin{bmatrix} i_{l2d} \\ i_{l2q} \end{bmatrix}_{k+1} \quad (4.57)$$

Solving for $\left[i_{l2d}\ i_{l2q}\right]_{k+1}^{T}$ results in (4.58).

$$\begin{bmatrix} i_{l2d} \\ i_{l2q} \end{bmatrix}_{k+1} = \begin{bmatrix} \frac{L_2}{R_1+L_2} & 0 \\ 0 & \frac{L_2}{R_1+L_2} \end{bmatrix} \begin{bmatrix} i_{l2d} \\ i_{l2q} \end{bmatrix}_{k} + \begin{bmatrix} -\frac{1}{2(R_1+L_2)} & -\frac{1}{2\sqrt{3}(R_1+L_2)} \\ \frac{1}{2\sqrt{3}(R_1+L_2)} & -\frac{1}{2(R_1+L_2)} \end{bmatrix} \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix}_{k+1} + \begin{bmatrix} \frac{1}{R_1+L_2} & 0 \\ 0 & \frac{1}{R_1+L_2} \end{bmatrix} \begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix}_{k+1}$$

(4.58)

Replacing (4.58) in (4.56)

$$\begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}_{k+1} = \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}_{k} + \begin{bmatrix} -\frac{T_s(L_1+L_2+R_1)}{2L_1(L_2+R_1)} & -\frac{T_s(L_1+L_2+R_1)}{2\sqrt{3}L_1(L_2+R_1)} \\ \frac{T_s(L_1+L_2+R_1)}{2\sqrt{3}L_1(L_2+R_1)} & -\frac{T_s(L_1+L_2+R_1)}{2L_1(L_2+R_1)} \end{bmatrix} \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix}_{k+1} +$$

$$+ \begin{bmatrix} \frac{T_s(L_1+L_2+R_1)}{L_1(L_2+R_1)} & 0 \\ 0 & \frac{T_s(L_1+L_2+R_1)}{L_1(L_2+R_1)} \end{bmatrix} \begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix}_{k+1} + \begin{bmatrix} -\frac{R_1T_s}{R_1+L_2} & 0 \\ 0 & -\frac{R_1T_s}{R_1+L_2} \end{bmatrix} \begin{bmatrix} i_{l2d} \\ i_{l2q} \end{bmatrix}_{k}$$

(4.59)

Applying the Euler backward method to the dynamic of the capacitor voltages $\left[v_{cd}v_{cq}\right]^{T}$ results in (4.60).

$$\begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix}_{k+1} = \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix}_{k} + T_s \begin{bmatrix} \frac{dv_{cd}}{dt} \\ \frac{dv_{cq}}{dt} \end{bmatrix}_{k+1} = \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix}_{k} + \begin{bmatrix} \frac{T_s}{2C_1} & -\frac{T_s}{2\sqrt{3}C_1} \\ \frac{T_s}{2\sqrt{3}C_1} & \frac{T_s}{2C_1} \end{bmatrix} \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}_{k+1} + \begin{bmatrix} -\frac{T_s}{2C_1} & \frac{T_s}{2\sqrt{3}C_1} \\ -\frac{T_s}{2\sqrt{3}C_1} & -\frac{T_s}{2C_1} \end{bmatrix} \begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix}_{k+1}$$

(4.60)

Replacing (4.60) in (4.59) and simplifying yields (4.61).

$$\begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}_{k+1} = \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}_{k} + \begin{bmatrix} -\dfrac{T_s\left(L_1+L_2+R_1\right)}{2L_1\left(L_2+R_1\right)} & -\dfrac{T_s\left(L_1+L_2+R_1\right)}{2\sqrt{3}L_1\left(L_2+R_1\right)} \\ \dfrac{T_s\left(L_1+L_2+R_1\right)}{2\sqrt{3}L_1\left(L_2+R_1\right)} & -\dfrac{T_s\left(L_1+L_2+R_1\right)}{2L_1\left(L_2+R_1\right)} \end{bmatrix} \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix}_k - \frac{T_s^2\left(L_1+L_2+R_1\right)}{3C_1L_1\left(L_2+R_1\right)} \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}_{k+1}$$
$$+ \frac{T_s^2\left(L_1+L_2+R_1\right)}{3C_1L_1\left(L_2+R_1\right)} \begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix}_{k+1} + \frac{T_s\left(L_1+L_2+R_1\right)}{L_1\left(L_2+R_1\right)} \begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix}_{k+1} - \frac{R_1T_s}{R_1+L_2} \begin{bmatrix} i_{l2d} \\ i_{l2q} \end{bmatrix}_k$$

(4.61)

Solving (4.61) for the $\left[i_{gd}\ i_{gq}\right]_{k+1}^{T}$ currents give (4.62)

$$\begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}_{k+1} = \frac{3C_1L_1\left(L_2+R_1\right)}{3C_1L_1\left(L_2+R_1\right)+\left(L_1+L_2+R_1\right)T_s^2} \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}_k + \frac{3C_1\left(L_1+L_2+R_1\right)T_s^2}{3C_1L_1\left(L_2+R_1\right)+\left(L_1+L_2+R_1\right)T_s^2} \begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix}_{k+1} +$$
$$+ \begin{bmatrix} -\dfrac{3C_1\left(L_1+L_2+R_1\right)T_s}{6C_1L_1\left(L_2+R_1\right)+2\left(L_1+L_2+R_1\right)T_s^2} & -\dfrac{\sqrt{3}C_1\left(L_1+L_2+R_1\right)T_s}{6C_1L_1\left(L_2+R_1\right)+2\left(L_1+L_2+R_1\right)T_s^2} \\ \dfrac{\sqrt{3}C_1\left(L_1+L_2+R_1\right)T_s}{6C_1L_1\left(L_2+R_1\right)+2\left(L_1+L_2+R_1\right)T_s^2} & -\dfrac{3C_1\left(L_1+L_2+R_1\right)T_s}{6C_1L_1\left(L_2+R_1\right)+2\left(L_1+L_2+R_1\right)T_s^2} \end{bmatrix} \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix}_k +$$
$$- \frac{3C_1L_1R_1T_s}{3C_1L_1\left(L_2+R_1\right)+\left(L_1+L_2+R_1\right)T_s^2} \begin{bmatrix} i_{l2d} \\ i_{l2q} \end{bmatrix}_k + \frac{\left(L_1+L_2+R_1\right)T_s^2}{3C_1L_1\left(L_2+R_1\right)+\left(L_1+L_2+R_1\right)T_s^2} \begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix}_{k+1}$$

(4.62)

Once again taking advantage of the fact that both filter states are similar it is possible to write the prediction of the currents $\left[i_{id}\ i_{iq}\right]_{k+1}^{T}$ as per (4.63), and for the prediction of the voltages $\left[v_{sd}\ v_{sq}\right]_{k+1}^{T}$ as per (4.64).

$$\begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix}_{k+1} = \frac{3C_2L_3\left(L_4+R_2\right)}{3C_2L_3\left(L_4+R_2\right)+\left(L_3+L_4+R_2\right)T_s^2} \begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix}_k + \frac{3C_1\left(L_1+L_2+R_1\right)T_s^2}{3C_2L_3\left(L_4+R_2\right)+\left(L_3+L_4+R_2\right)T_s^2} \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix}_{k+1} +$$
$$+ \begin{bmatrix} -\dfrac{3C_2\left(L_3+L_4+R_2\right)T_s}{6C_2L_3\left(L_4+R_2\right)+2\left(L_3+L_4+R_2\right)T_s^2} & -\dfrac{\sqrt{3}C_2\left(L_3+L_4+R_2\right)T_s}{6C_2L_3\left(L_4+R_2\right)+2\left(L_3+L_4+R_2\right)T_s^2} \\ \dfrac{\sqrt{3}C_2\left(L_3+L_4+R_2\right)T_s}{6C_2L_3\left(L_4+R_2\right)+2\left(L_3+L_4+R_2\right)T_s^2} & -\dfrac{3C_2\left(L_3+L_4+R_2\right)T_s}{6C_2L_3\left(L_4+R_2\right)+2\left(L_3+L_4+R_2\right)T_s^2} \end{bmatrix} \begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix}_k +$$
$$- \frac{3C_2L_3R_2T_s}{3C_2L_3\left(L_4+R_2\right)+\left(L_3+L_4+R_2\right)T_s^2} \begin{bmatrix} i_{l4d} \\ i_{l4q} \end{bmatrix}_k + \frac{\left(L_3+L_4+R_2\right)T_s^2}{3C_2L_3\left(L_4+R_2\right)+\left(L_3+L_4+R_2\right)T_s^2} \begin{bmatrix} i_{md} \\ i_{mq} \end{bmatrix}_{k+1}$$

(4.63)

$$\begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix}_{k+1} = \begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix}_{k} + \begin{bmatrix} \frac{T_s}{2C_2} & -\frac{T_s}{2\sqrt{3}C_2} \\ \frac{T_s}{2\sqrt{3}C_2} & \frac{T_s}{2C_2} \end{bmatrix} \begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix}_{k+1} + \begin{bmatrix} -\frac{T_s}{2C_2} & \frac{T_s}{2\sqrt{3}C_2} \\ -\frac{T_s}{2\sqrt{3}C_2} & -\frac{T_s}{2C_2} \end{bmatrix} \begin{bmatrix} i_{md} \\ i_{mq} \end{bmatrix}_{k+1} \tag{4.64}$$

The relations in (4.62) and (4.63) allow the prediction of the input grid currents where $\left[i_{md}\ i_{mq}\right]_{k+1}^{T}$ depend on the output converter currents and the converter vector. It also depends on the explicit measurement of the input grid current and voltage, the voltages $\left[v_{cd}\ v_{cq}\right]^{T}$, the voltages $\left[v_{sd}\ v_{sq}\right]^{T}$, the inductor currents $\left[i_{l2d}\ i_{l2q}\right]^{T}$ and $\left[i_{l4d}\ i_{l4q}\right]^{T}$ as well as the intermediate filter current $\left[i_{id}\ i_{iq}\right]^{T}$.

In an effort to reduce the number of explicit current measurements, assuming that $L_2 \ll L_1$ and $L_4 \ll L_3$ the approximation in (4.65) and (4.66) can be done.

$$\begin{bmatrix} i_{l1d} \\ i_{l1q} \end{bmatrix} \approx \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} - \begin{bmatrix} \frac{L_1}{R_1}\frac{di_{l1d}}{dt} \\ \frac{L_1}{R_1}\frac{di_{l1q}}{dt} \end{bmatrix} = \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} - \begin{bmatrix} -\frac{1}{2R_1} & -\frac{1}{2\sqrt{3}R_1} \\ \frac{1}{2\sqrt{3}R_1} & -\frac{1}{2R_1} \end{bmatrix} \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} - \begin{bmatrix} \frac{1}{R_1} & 0 \\ 0 & \frac{1}{R_1} \end{bmatrix} \begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix} \tag{4.65}$$

$$\begin{bmatrix} i_{l3d} \\ i_{l3q} \end{bmatrix} \approx \begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix} - \begin{bmatrix} \frac{L_3}{R_2}\frac{di_{l1d}}{dt} \\ \frac{L_3}{R_2}\frac{di_{l1q}}{dt} \end{bmatrix} = \begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix} - \begin{bmatrix} -\frac{1}{2R_2} & -\frac{1}{2\sqrt{3}R_2} \\ \frac{1}{2\sqrt{3}R_2} & -\frac{1}{2R_2} \end{bmatrix} \begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} - \begin{bmatrix} \frac{1}{R_2} & 0 \\ 0 & \frac{1}{R_2} \end{bmatrix} \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} \tag{4.66}$$

Replacing (4.65) in (4.62) and (4.66) in (4.63) results in (4.67) and (4.68), respectively.

$$\begin{aligned} \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}_{k+1} \approx\ & \frac{3C_1L_1\left(L_2+R_1\right)}{3C_1L_1\left(L_2+R_1\right)+\left(L_1+L_2+R_1\right)T_s^2} \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}_{k} + \frac{3C_1\left(L_1+L_2+R_1\right)T_s^2-3C_1L_1T_s}{3C_1L_1\left(L_2+R_1\right)+\left(L_1+L_2+R_1\right)T_s^2} \begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix}_{k+1} + \\ & + \begin{bmatrix} \frac{-3C_1\left(L_1+L_2+R_1\right)T_s+3C_1L_1T_s}{6C_1L_1\left(L_2+R_1\right)+2\left(L_1+L_2+R_1\right)T_s^2} & \frac{-\sqrt{3}C_1\left(L_1+L_2+R_1\right)T_s+\sqrt{3}C_1L_1T_s}{6C_1L_1\left(L_2+R_1\right)+2\left(L_1+L_2+R_1\right)T_s^2} \\ \frac{\sqrt{3}C_1\left(L_1+L_2+R_1\right)T_s-\sqrt{3}C_1L_1T_s}{6C_1L_1\left(L_2+R_1\right)+2\left(L_1+L_2+R_1\right)T_s^2} & \frac{-3C_1\left(L_1+L_2+R_1\right)T_s+3C_1L_1T_s}{6C_1L_1\left(L_2+R_1\right)+2\left(L_1+L_2+R_1\right)T_s^2} \end{bmatrix} \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix}_{k} + \\ & + \frac{\left(L_1+L_2+R_1\right)T_s^2}{3C_1L_1\left(L_2+R_1\right)+\left(L_1+L_2+R_1\right)T_s^2} \begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix}_{k+1} \end{aligned} \tag{4.67}$$

$$\begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix}_{k+1} \approx \frac{3C_2L_3\left(L_4+R_2\right)}{3C_2L_3\left(L_4+R_2\right)+\left(L_3+L_4+R_2\right)T_s^2}\begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix}_k + \frac{3C_1\left(L_1+L_2+R_1\right)T_s^2-3C_2L_3T_s}{3C_2L_3\left(L_4+R_2\right)+\left(L_3+L_4+R_2\right)T_s^2}\begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix}_{k+1} + \\ + \begin{bmatrix} \frac{-3C_2\left(L_3+L_4+R_2\right)T_s+3C_2L_3T_s}{6C_2L_3\left(L_4+R_2\right)+2\left(L_3+L_4+R_2\right)T_s^2} & \frac{-\sqrt{3}C_2\left(L_3+L_4+R_2\right)T_s+\sqrt{3}C_2L_3T_s}{6C_2L_3\left(L_4+R_2\right)+2\left(L_3+L_4+R_2\right)T_s^2} \\ \frac{\sqrt{3}C_2\left(L_3+L_4+R_2\right)T_s-\sqrt{3}C_2L_3T_s}{6C_2L_3\left(L_4+R_2\right)+2\left(L_3+L_4+R_2\right)T_s^2} & \frac{-3C_2\left(L_3+L_4+R_2\right)T_s+3C_2L_3T_s}{6C_2L_3\left(L_4+R_2\right)+2\left(L_3+L_4+R_2\right)T_s^2} \end{bmatrix}\begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix}_k + \\ + \frac{\left(L_3+L_4+R_2\right)T_s^2}{3C_2L_3\left(L_4+R_2\right)+\left(L_3+L_4+R_2\right)T_s^2}\begin{bmatrix} i_{md} \\ i_{mq} \end{bmatrix}_{k+1}$$

(4.68)

With the relation in (4.67) and (4.68) it is possible to predict the both the grid current, $\left[i_{gd}\ i_{gq}\right]_{k+1}^T$, and the intermediate filter current $\left[i_{id}\ i_{iq}\right]_{k+1}^T$ with the explicit measurements of the voltages$\left[v_{gd}\ v_{gq}\right]_k^T$, $\left[v_{cd}\ v_{cq}\right]_k^T$ and $\left[v_{sd}\ v_{sq}\right]_k^T$ combined with the measurements of the currents $\left[i_{gd}\ i_{gq}\right]_k^T$ and $\left[i_{id}\ i_{iq}\right]_k^T$. It is important to note that the approximation $\left[v_{gd}\ v_{gq}\right]_{k+1}^T \approx \left[v_{gd}\ v_{gq}\right]_k^T$ is considered since there is no feasible manner to predict the future grid voltage. Furthermore, and since the reference frame is synchronous with the grid voltages then $v_{gq}=0$.

With the relation in (4.67) and (4.68) the prediction of the grid current is made in two steps, first by predicting the intermediate filter current for the possible values of the input matrix converter current, $\left[i_{md}\ i_{mq}\right]_{k+1}^T$, and then using that prediction to directly compute the input grid current.

Prediction of the output converter current

By inspection of the output voltage loops, the relation in (4.69) can

$$\begin{bmatrix} \frac{di_{od}}{dt} \\ \frac{di_{oq}}{dt} \\ \frac{di_{o0}}{dt} \end{bmatrix} = -\frac{r_o}{L_o}\begin{bmatrix} i_{od} \\ i_{oq} \\ i_{o0} \end{bmatrix} - \frac{1}{L_o}\begin{bmatrix} v_{od} \\ v_{oq} \\ v_{o0} \end{bmatrix} + \frac{1}{L_o}\begin{bmatrix} v_{md} \\ v_{mq} \\ v_{m0} \end{bmatrix} \tag{4.69}$$

Using the Euler Backward method, it is possible to obtain the relation in (4.70).

$$\begin{bmatrix} i_{od} \\ i_{oq} \\ i_{o0} \end{bmatrix}_{k+1} = \begin{bmatrix} i_{od} \\ i_{oq} \\ i_{o0} \end{bmatrix}_{k} - \frac{T_s r_o}{L_o} \begin{bmatrix} i_{od} \\ i_{oq} \\ i_{o0} \end{bmatrix}_{k+1} - \frac{T_s}{L_o} \begin{bmatrix} v_{od} \\ v_{oq} \\ v_{o0} \end{bmatrix}_{k+1} + \frac{T_s}{L_o} \begin{bmatrix} v_{md} \\ v_{mq} \\ v_{m0} \end{bmatrix}_{k+1} \tag{4.70}$$

Solving (4.70) for $\left[i_{od}\ i_{oq}\ i_{o0}\right]_{k+1}^{T}$ allows to write the relation in (4.71).

$$\begin{bmatrix} i_{od} \\ i_{oq} \\ i_{o0} \end{bmatrix}_{k+1} = \frac{L_o}{L_o + T_s r_o} \begin{bmatrix} i_{od} \\ i_{oq} \\ i_{o0} \end{bmatrix}_{k} - \frac{T_s}{L_o + T_s r_o} \begin{bmatrix} v_{od} \\ v_{oq} \\ v_{o0} \end{bmatrix}_{k+1} + \frac{T_s}{L_o + T_s r_o} \begin{bmatrix} v_{md} \\ v_{mq} \\ v_{m0} \end{bmatrix}_{k+1} \tag{4.71}$$

Equation (4.71) allows the prediction of the output currents, $\left[i_{od}\ i_{oq}\ i_{o0}\right]_{k+1}^{T}$, using the future output voltages of the converter (that are a function of the converter state and the voltages $\left[v_{sd}\ v_{sq}\right]^{T}$) and the explicit measurements of the output currents $\left[i_{od}\ i_{oq}\ i_{o0}\right]_{k}^{T}$ and the output voltages $\left[v_{od}\ v_{oq}\ v_{o0}\right]_{k}^{T}$ where once again it is assumed that the output voltage variation during the period T_s is negligible and as such $\left[v_{od}\ v_{oq}\ v_{o0}\right]_{k+1}^{T} \approx \left[v_{od}\ v_{oq}\ v_{o0}\right]_{k}^{T}$.

Model predictive control cost function and vector selection

Assuming a reference output converter current $\left[i_{od}^{*}\ i_{oq}^{*}\ \ i_{o0}^{*}\right]^{T}$ and a reference input reactive power Q_g^{*} the objective of the MPC is to track this reference values by selecting the optimal vectors at each period T_s. Setting references for the output currents already sets the input active power leaving no extra degrees of freedom.

The predicted reactive power can be computed as per (4.72).

$$Q_{g(k+1)} = v_{gd(k+1)} i_{gq(k+1)} - v_{gq(k+1)} i_{gd(k+1)} \tag{4.72}$$

A cost function g_g is defined as in (4.73), the closer the prediction values for the output currents and the input reactive power are to their respective reference values the smaller is the value of g_g.

$$g_{g(k+1)} = w_1 \left(Q_g^{*} - Q_{g(k+1)}\right)^2 + w_2 \left(i_{od}^{*} - i_{od(k+1)}\right)^2 + w_3 \left(i_{oq}^{*} - i_{oq(k+1)}\right)^2 + w_4 \left(i_{o0}^{*} - i_{o0(k+1)}\right)^2 \tag{4.73}$$

Weighting factors w_1, w_2 and w_3 are the predictive controllers gains and need to be tuned for the correct controller operation. The initial search values are obtained by normalization where

$w_1 = 1/S_{nom}^2$ where S_{nom} is the nominal apparent power of the SST, and $w_1 = w_3 = w_3 = 1/I_{nom}^2$ where I_{nom} is the nominal output current of the SST.

Since the selected vector is only applied at the end of the T_s period the prediction horizon needs to be expanded by one period time step. This is detailed in Section 2.2.7 and depicted in Figure 2.13. A flowchart describing the vector selection process is shown in Figure 4.15.

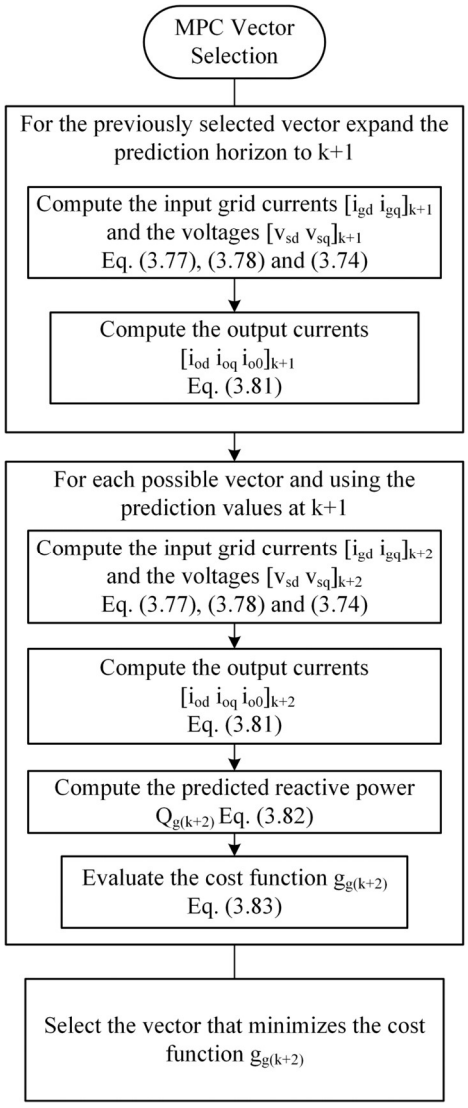


Figure 4.15 Flowchart of the vector selection process using the prediction equations detailed in this section.

The detailed vector selection process makes it so that the MPC controller will select the vector that best tracks the input reactive power output currents. Finding a reference for the output currents is the topic of the next section where an output voltage controller generates the reference values $\left[i_{od}^* \; i_{oq}^* \;\; i_{o0}^*\right]^T$.

4.3.3 On load non-linear control of the SST output voltages

Consider a set of output voltage references given by $\left[v_{od}^{*}\ v_{oq}^{*}\ v_{o0}^{*}\right]^{T}$ and the output voltages $\left[v_{od}\ v_{oq}\ v_{o0}\right]^{T}$, the error $[e_{vd}\ e_{vq}\ e_{v0}]$ between the output voltage references can be defined as per (4.74).

$$\begin{bmatrix} e_{vd} \\ e_{vq} \\ e_{v0} \end{bmatrix} = \begin{bmatrix} v_{od}^{*} \\ v_{oq}^{*} \\ v_{o0}^{*} \end{bmatrix} - \begin{bmatrix} v_{od} \\ v_{oq} \\ v_{o0} \end{bmatrix} \tag{4.74}$$

A set of positive definite Lyapunov functions $\left[V_{vd}\ V_{vq}\ V_{v0}\right]^{T}$, can be defined as per (4.75):

$$\begin{bmatrix} V_{vd} \\ V_{vq} \\ V_{v0} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} e_{vd}^{2} \\ e_{vq}^{2} \\ e_{v0}^{2} \end{bmatrix} \tag{4.75}$$

To guarantee asymptotic stability the derivative of each function V_{vd}, V_{vq} and V_{v0} must be negative definite resulting in the stability condition in (4.76).

$$\begin{cases} \dfrac{dV_{vd}}{dt}(\mathrm{e}_{vd} \neq 0) = e_{vd}\dfrac{de_{vd}}{dt} < 0 \\ \dfrac{dV_{vq}}{dt}(\mathrm{e}_{vq} \neq 0) = e_{vq}\dfrac{de_{vq}}{dt} < 0 \\ \dfrac{dV_{v0}}{dt}(\mathrm{e}_{v0} \neq 0) = e_{v0}\dfrac{de_{v0}}{dt} < 0 \end{cases} \tag{4.76}$$

The relation in (4.76) can be satisfied by constraining the error time derivates as per (4.77)

$$\begin{cases} \dfrac{de_{vd}}{dt} = -K_{v}e_{vd} \\ \dfrac{de_{vq}}{dt} = -K_{v}e_{vq} \\ \dfrac{de_{v0}}{dt} = -K_{v}e_{v0} \end{cases} \quad , \text{ where } K_{v} > 0 \tag{4.77}$$

In (4.77) K_v, is a design variable constrained to be positive and related to the inverse of the time constant of the error decay to zero. Replacing the voltage error definition of (4.74) in (4.77) the relation in (4.78) is obtained.

$$\begin{cases} \dfrac{dv_d^*}{dt} - \dfrac{dv_{0d}}{dt} = -K_v e_{vd} \\ \dfrac{dv_{dq0}^*}{dt} - \dfrac{dv_{oq}}{dt} = -K_v e_{vq} \\ \dfrac{dv_{dq0}^*}{dt} - \dfrac{dv_{o0}}{dt} = -K_v e_{v0} \end{cases} \tag{4.78}$$

Replacing (4.53) in (4.78) the reference values for the output currents $\left[i_{od}^* \; i_{oq}^* \; i_{o0}^*\right]^T$ can be obtained according to (4.79).

$$\begin{bmatrix} i_{od}^* \\ i_{oq}^* \\ i_{o0}^* \end{bmatrix} = C_0 K_v \begin{bmatrix} e_{vd} \\ e_{vq} \\ e_{v0} \end{bmatrix} + C_0 \begin{bmatrix} \dfrac{dv_{od}^*}{dt} \\ \dfrac{dv_{oq}^*}{dt} \\ \dfrac{dv_{o0}^*}{dt} \end{bmatrix} + \begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{bmatrix} \tag{4.79}$$

The relation in (4.79) provides the reference values of the output currents for (4.73), this relation depends on the measurements of the load currents $\left[i_{Ld} \; i_{Lq} \; i_{L0}\right]^T$, the measurements of the output capacitor voltages $\left[v_{od} \; v_{oq} \; v_{o0}\right]^T$ as well as the time derivative of the reference output voltages. Since the reference output voltages in the dq reference frame are mostly constant than it is assumed that these time derivates are equal to 0.

4.3.4 Discussion of the proposed controller

The proposed controller directly controls the output gird voltages with sinusoidal balanced input currents even for unbalanced loads. The direct control of the output voltages also means that the SST will be able to keep the output voltages regulated during sags and swell events, it will also work as a series harmonic compensator reducing the harmonic content on the output gird voltage when compared to the input grid voltages. The same behaviour is expected for the input grid currents where the power factor of the load as well as additional harmonic content can be mitigated in the upstream current.

Additionally, by setting the input reactive power reference, it is possible to provide grid support services such as injecting and consuming reactive power for voltage compensation in the input grid.

Chapter 5

SOLID STATE TRANSFORMER SIMULATION AND EXPERIMENTAL RESULTS

5.1 Simulation Results

This section shows simulation results obtained with the proposed solid-state transformer topology and the input filter sized by the optimisation algorithm. All results are obtained with a linear transformer model reduced to its primary, characterised by its number of turns, winding resistance, R_{cu}, leakage and magnetising inductances, L_{ck} and L_m respectively. These parameters along with the input phase-to-phase voltage, V_{ph-ph}, and the switching frequency, f_{sw}, are shown in Table 5.1 and their values are representative of equipment currently available in the Electrical Machines Laboratory. The simulation was performed using switched models of MOSFET devices, simulation time steps where set to $2\mu s$ with the exception of simulations for the commutation process where the simulation time step was set to $10ns$.

Table 5.1 Set of parameters used for all simulations performed in Chapter 4.

r_t	R_{cu}	L_{ck}	L_m	f_{sw}	V_{ph-ph}
1	80 mΩ	1 μH	8 mH	35 kHz	400 V

Simulation results will be shown for the commutation process and for the proposed modulation scheme using an output RL load with a power factor close to 0.8.

5.1.1 Simulation results for the commutation process

Simulation results for the commutation process were obtained in the same conditions as the suggested example depicted in Figure 3.11. The resulting waveforms for the voltages and currents at each winding are shown in Figure 5.1 consecutively for the first, second and third windings. After each of the intermediate vectors, a freewheeling period follows to commutate

the output currents (FW in the figure). Once the freewheeling period is over the non-conducting semiconductors need to be opened before applying the next intermediate vector (ONC in the figure).

The most crucial detail of the commutation process is that the currents freewheel with a slope proportional to the winding voltage and inversely proportional to the leakage inductance, always providing a path for the circulation of the leakage energy, which results in safe commutations with no overvoltages on the secondary of the transformer.

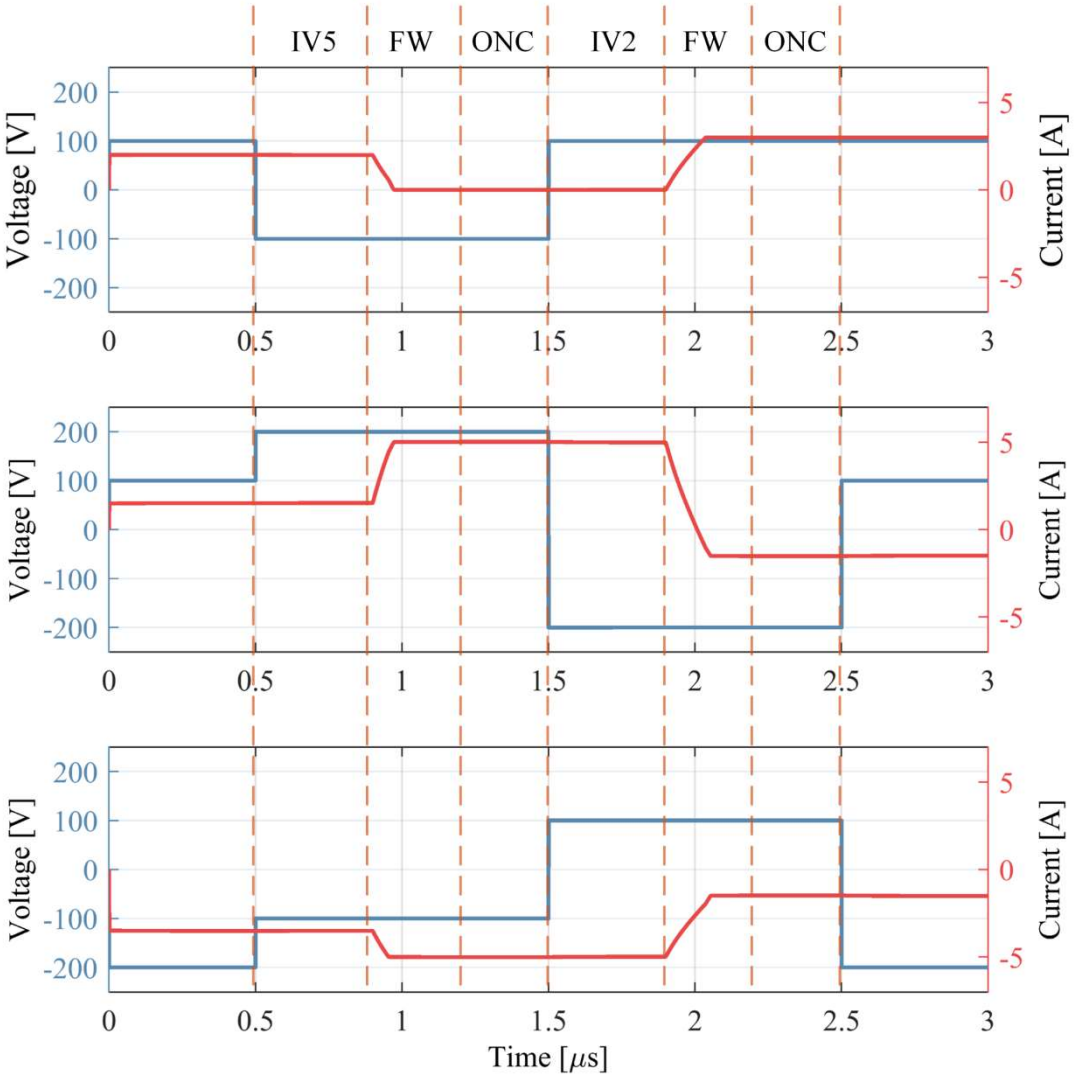


Figure 5.1 Waveform of the commutation process for the example commutation of section 3.2.3. Winding voltages are in blue and windings currents are in red for the first second and third winding, respectively.

5.1.2 Simulation Results of the SST topology with an inductive load

The proposed SST topology, including the input filter sized in section 3.3, was simulated, supplying an unbalanced RL load with a 10% load imbalance in phase b. A 3×4 Venturini modulation method implemented as described in section 2.2.7 is used to set the reference vector for the equivalent χ matrix converter with the modulation method implemented according to section 3.1.

Figure 5.2 shows the waveforms of the input currents with a step on the Venturini modulation index at t=0.5s with an average current THD of 2.1%. The resulting output load currents are shown in Figure 5.3 with the neutral current in orange with all output currents averaging 1.5% THD.

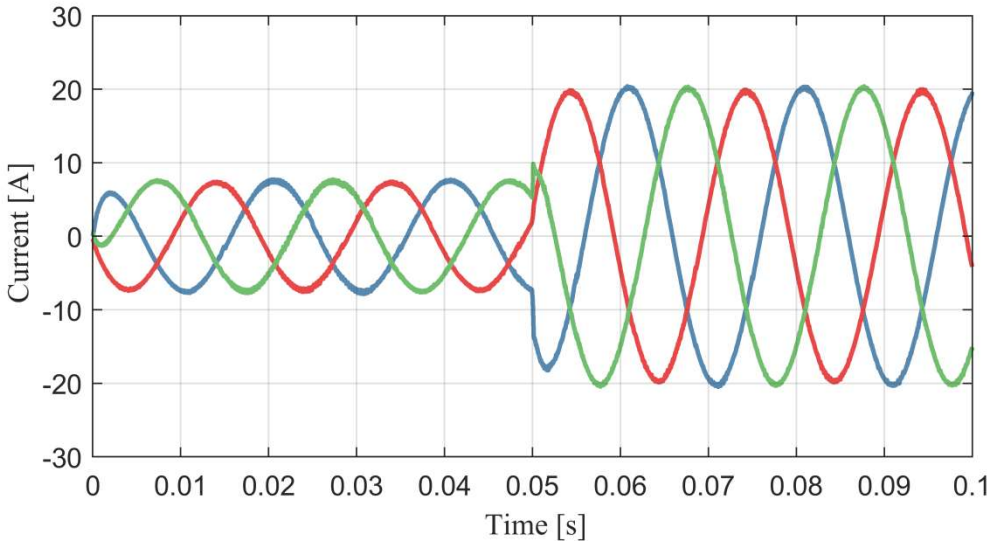


Figure 5.2 Waveforms of the input current of the SST in the input phases a, b and c, in blue, red and green, respectively.

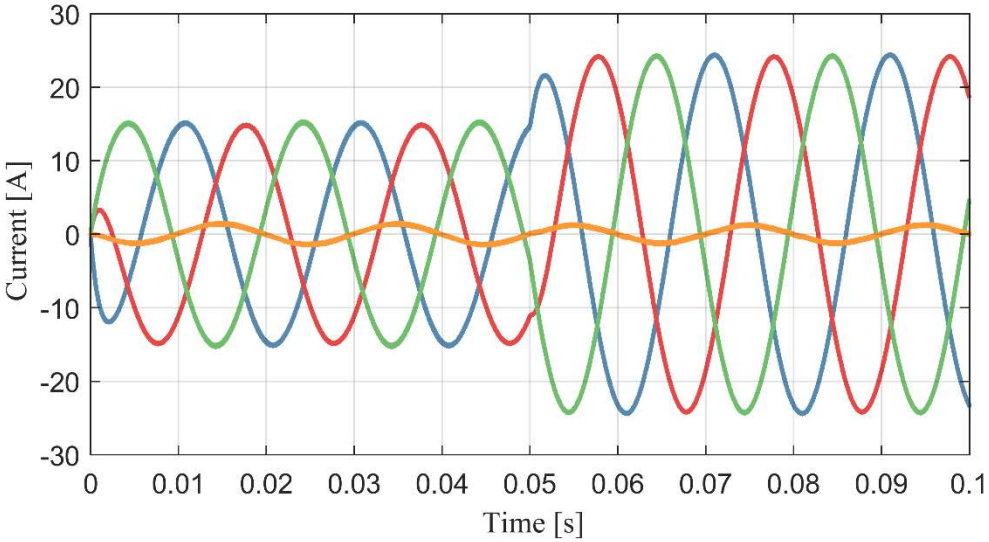


Figure 5.3 Waveforms of the output current of the SST in the output phases A, B, C and neutral in blue, red, green and orange, respectively.

The resulting transformer primary windings voltages for the same scenario above during the period between 0.05 s and 0.06 s are shown in Figure 5.4. An interesting remark is that the voltages hardly appear to have a periodic repetition pattern, showing a behaviour that at the first glance can look aperiodic. This is a consequence of the way the reference vectors of $\boldsymbol{\chi}$ are being unfolded, since the transformer flux is constantly minimised, which in turn depend on the transformer's flux at the moment of computation resulting in the waves shown in Figure 5.4.

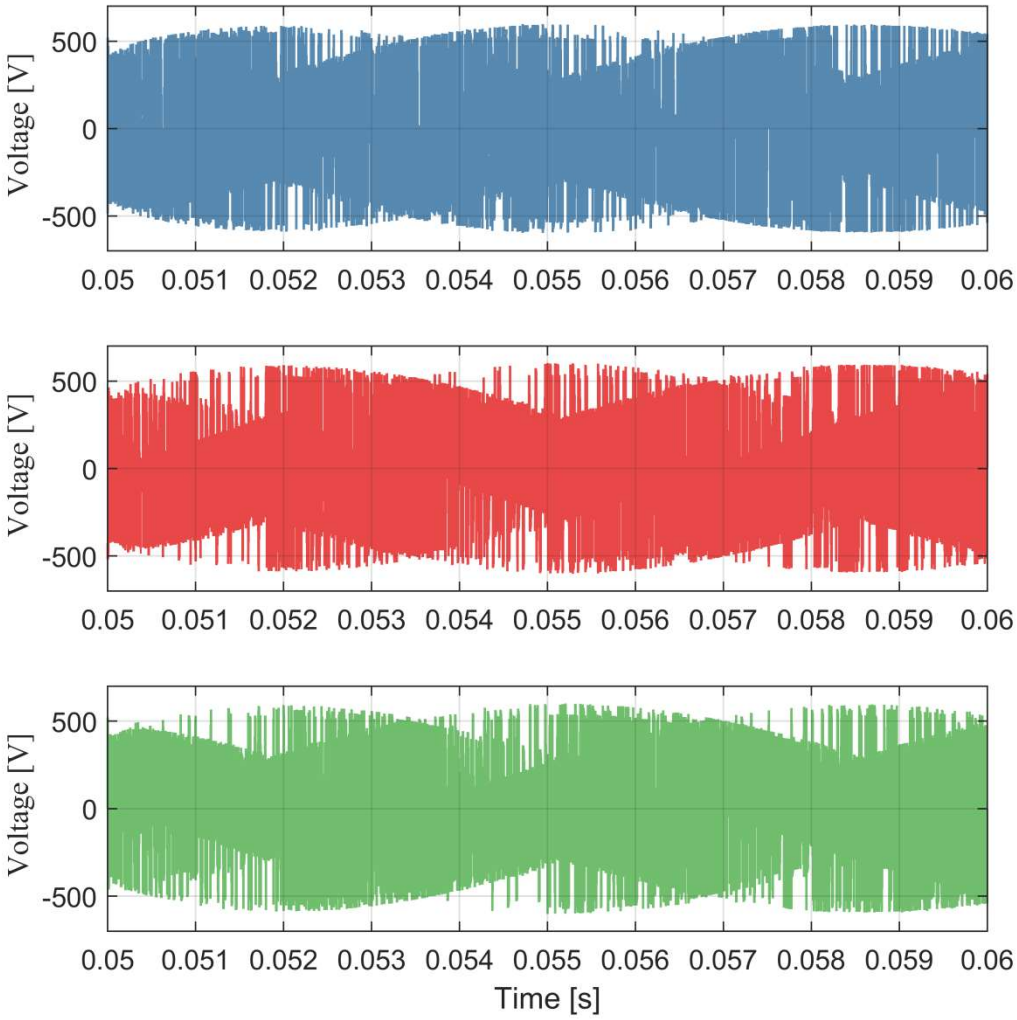


Figure 5.4 Waveforms of the primary winding voltages in the first, second and third windings in blue, red and green respectively.

To highlight the potential capabilities of the proposed SST for grid applications, the converters are used to have a unitary input power factor while supplying an unbalanced inductive load with a 0.86 power factor. The power factor correction is enabled at t=0.5s of the simulation with the current and voltage waveforms being depicted in Figure 5.5.

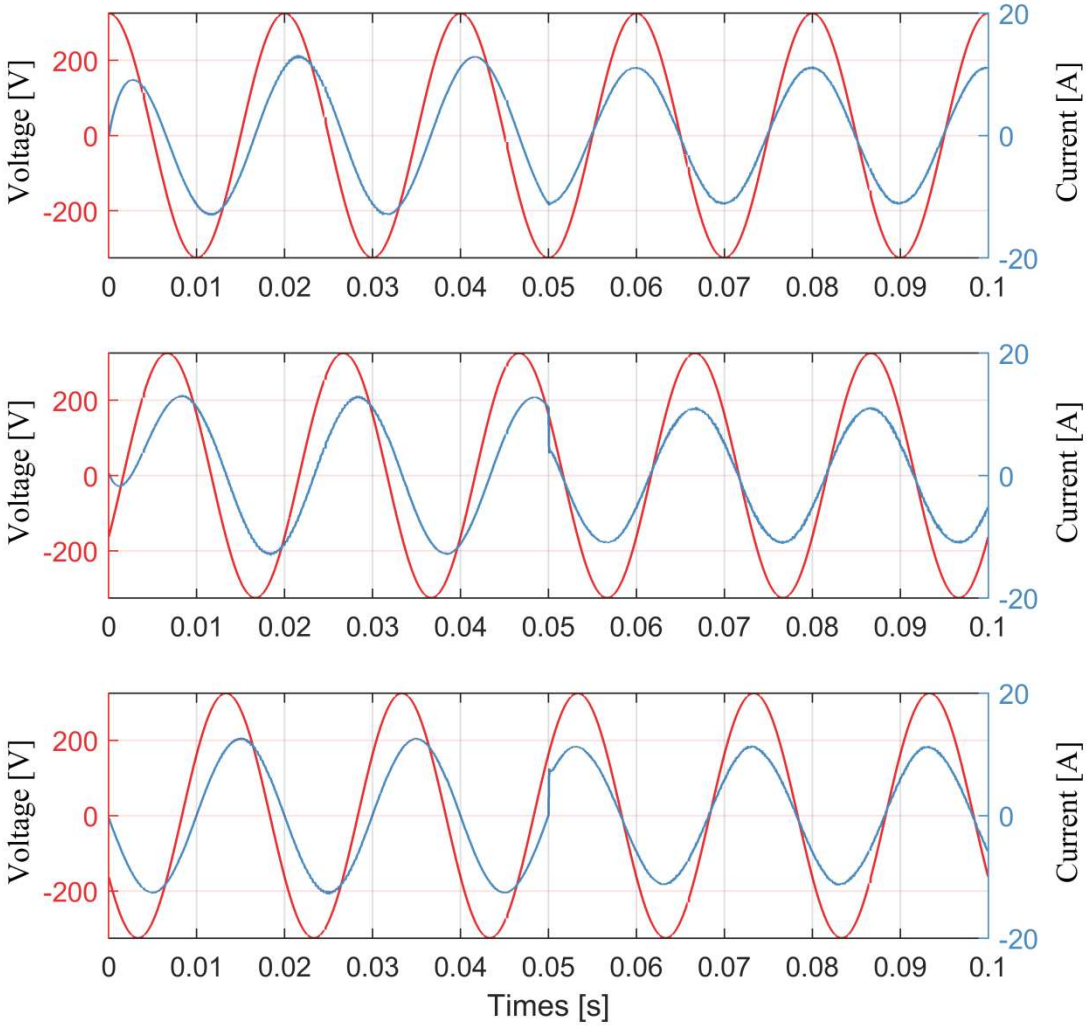


Figure 5.5 Waveforms of the input grid currents (in blue) and voltages (in red) where for the first 0.5 seconds there is no unitary power factor regulation and for the remaining 0.5 seconds a unitary power factor is obtained at the input. The waveforms are sequentially shown for the input phases a, b and c.

The obtained waveforms, with similar THDs as the ones obtained in the previous simulations, show the ability to control the input power factor, which can also be used to inject reactive power into the upstream grid.

The resulting active and reactive powers, as well as the resulting power factor during the simulation, can be observed in Figure 5.6, where initially, the output power factor is mimicked at the input, and it's driven to be unitary at t=0.5s, resulting in a decrease to practically zero reactive power.

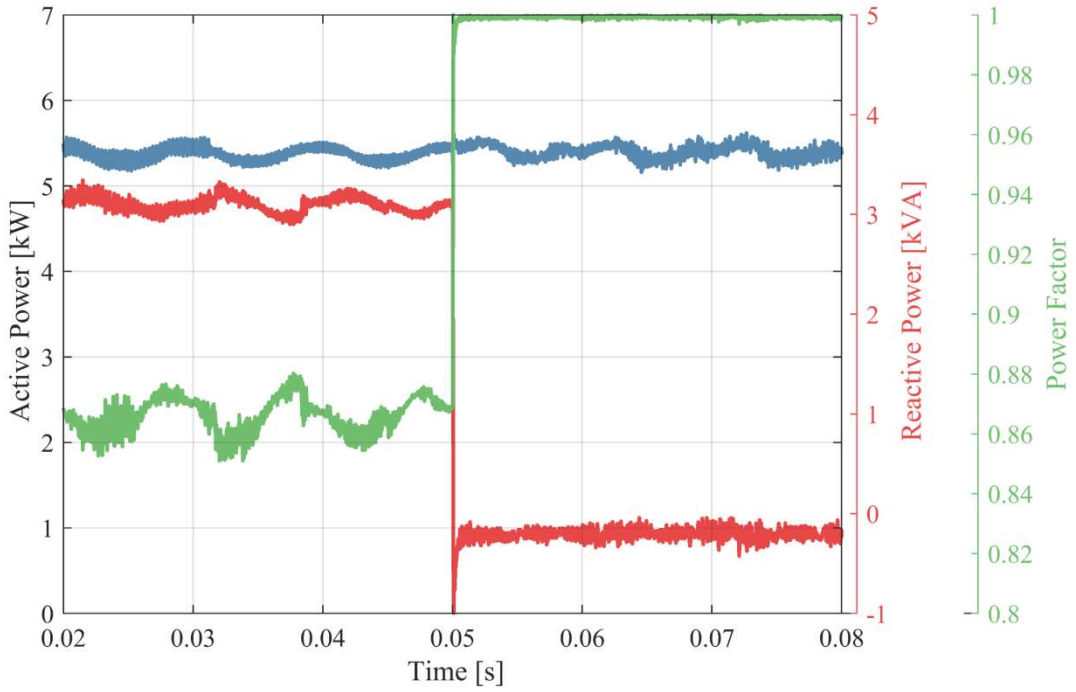


Figure 5.6 Waveforms for the active power (blue), reactive power (red) and power factor (green) during the transition from non-regulated power factor to regulated power factor.

5.1.3 Simulation Results of the model predictive current controller and on-load non-linear voltage controller

The proposed control method in Section 4.3.3 is simulated in this section using the equivalent converter model χ and the input filter sized in Section 4.2.2.

The predictions models in (4.67), (4.68) and (4.71) are discretised with a T_S of 15 μs and the converter is connected to a grid with an input voltage of 230V and controlling an output grid voltage, in grid-forming mode, of 110V. The parameters used in the simulation are shown in Table 5.2. The SST is supplying a grid with three phase to neutral load P_a, P_b and P_c. The output filter is an LC filter as depicted in Figure 4.14.

Table 5.2 Simulation parameters for the SST equivalent model χ with the controller designed in Section 4.3.3.

Parameter	Symbol	Value
Discretization Period	T_s	$15\ \mu s$
Input Grid Voltage	V_g	$230\ V$
Output Grid Voltage	V_o	$110\ V$
Sag Voltage	V_{gswag}	$161\ V$
Swell Voltage	V_{gswell}	$300\ V$
Input and Output grid frequency	$\{f_i, f_o\}$	$\{50,50\}\ Hz$
Inductances	$\{L_1, L_2, L_3, L_4, L_o\}$	$\{1030, 89.4, 210, 5\}\ \mu H$
Resistances	$\{R_1, R_2, r_o\}$	$\{5.1, 4.9, 0.1\}\ \Omega$
Capacitances	$\{C_1, C_2, C_o\}$	$\{3.4, 4.0\}\ \mu F$
Phase a, b and c powers	$\{P_a, P_b, P_c, P_{a2}\}$	$\{1.1,1.1,1.1,0.4\}\ kW$
Voltage controller gain	K_v	2500
Predictive Controller gains	$\{w_1, w_2, w_3, w_4\}$	$\{1e^{-5}, 1, 1, 0.5\}\ kW$

Three different events are tested during the simulation: at $t = 0.25s$ an additional load, P_{a2}, is connected to the output phase a increasing the baseline load by 25% and consequently unbalancing the three-phase load; at $t = 0.5$ the input grid voltages suffer a balanced voltage sag of 30%; at $t = 0.75$ the input grid voltages suffer a balanced voltage swell of 30%.

The grid voltage is depicted in Figure 5.7, showing the two events, sag and swell, at $t = 0.025\ s$ and $t = 0.05$ s, respectively.

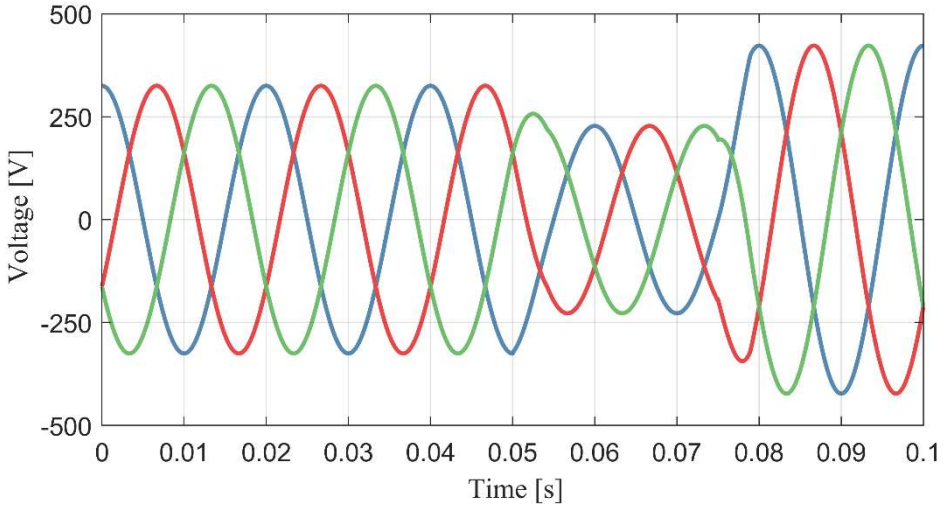


Figure 5.7 Input grid voltages phase a, b and c in blue, red ad green respectively. Voltage sag event at $t = 0.05$ seconds and swell event at $t = 0.075$ seconds.

The output load current is depicted in Figure 5.8 showing the connection of an additional load in the output phase a at $t = 0.025s$.

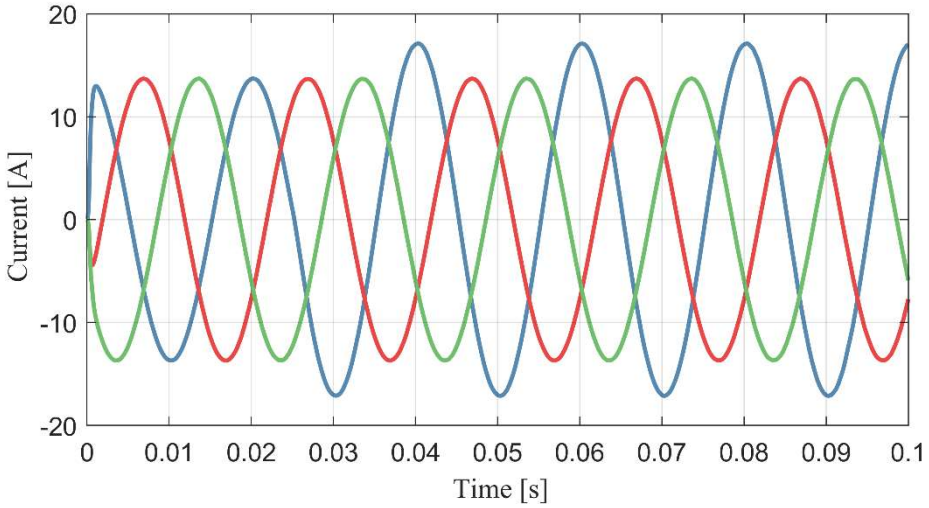


Figure 5.8 Output load current in phases a, b and c in blue, red and green respectively. Addicional load P_{a2} is connected at $t = 0.025$ seconds.

The output voltage remains regulated during all three events, as can be seen in Figure 5.9, with a voltage THD lower than 1%.

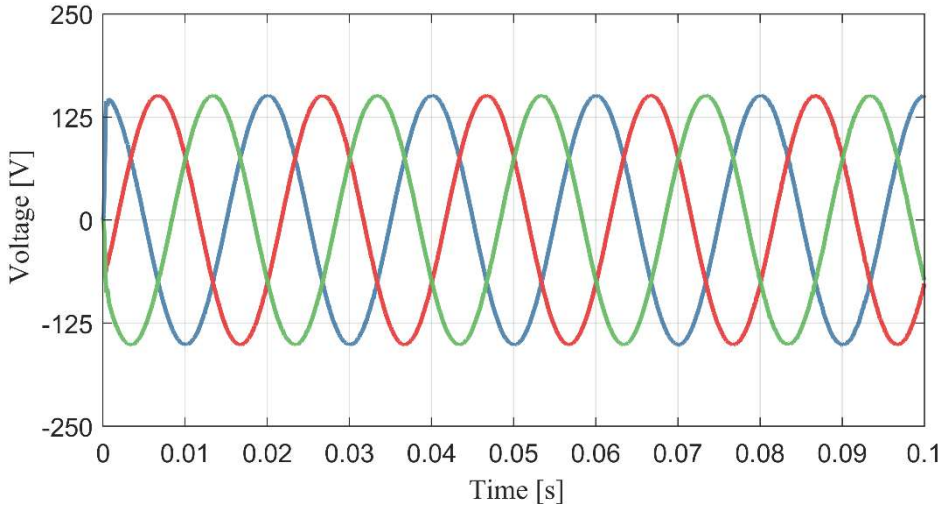


Figure 5.9 Output load voltage phase a,b and c in red, blue and green respectively.

The input grid current can be seen in Figure 5.10. Since the output grid currents are unbalanced, the active power has a 100 Hz component, introducing some deformation in the input grid currents. Nonetheless, the input reactive power remains controlled with a unitary power factor.

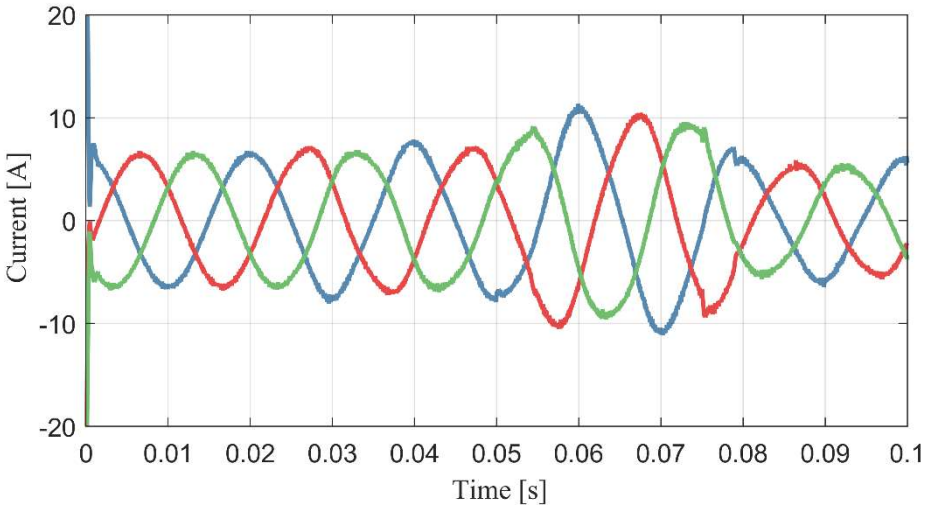


Figure 5.10 Input grid currents at phases a, b and c in blue, red and green respectively.

5.1.4 Simulation Results Discussion

The simulations performed in this document show promising results for the applicability of the proposed SST. The simulations that validate the commutation method show that the commutation can be completed in 1 to 2 μs which is within an acceptable range for a switching frequency of 35 kHz.

The modulation method was tested by controlling both the primary and secondary SST converters using a simple Venturini method to generate the references for the equivalent converter, which led to satisfactory results. The SST's ability to control the input power factor was demonstrated.

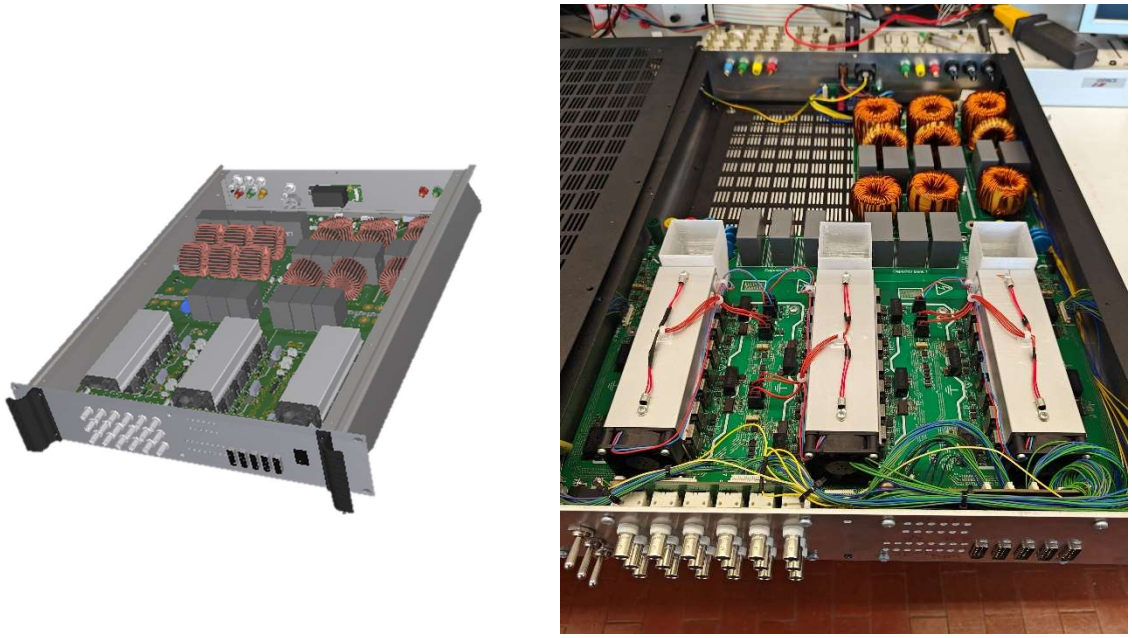
The designed controller is shown to be able to control the output voltage of an output grid in grid forming mode, mitigating the impacts of voltage sags and swells and keeping the output voltages balanced during unbalanced load conditions.

The results mentioned above were obtained using the filter sized by the proposed filter optimisation method and the transformer parameters obtained from the FEM analysis.

5.2 Experimental Results

To obtain experimental validation, a 3x4 DMC converter with SiC MOSFETs was designed, and two units were fabricated and tested. The schematic drawings and converter description

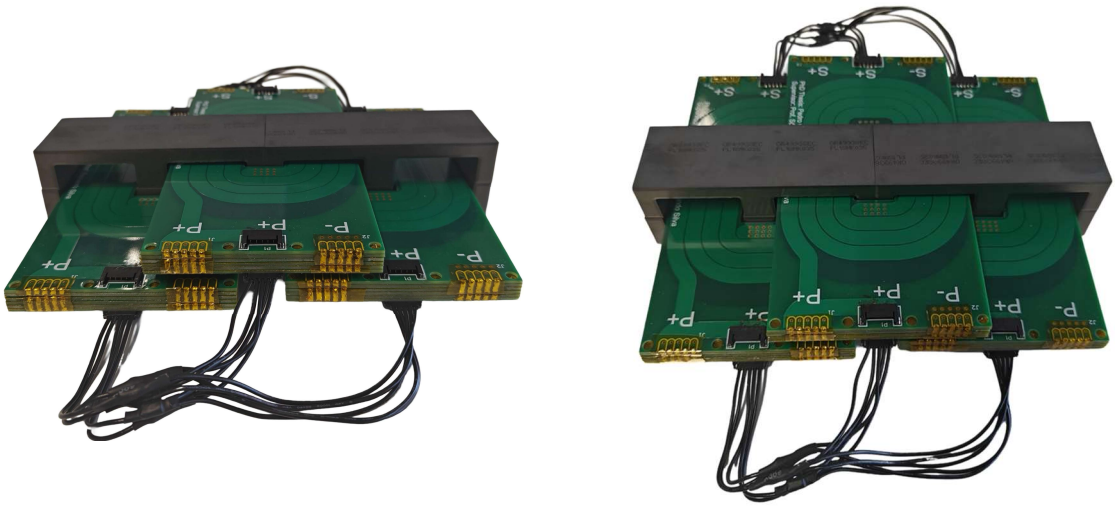
can be found in Appendix C. The depiction of the design and the built prototype for a single 3x4DMC can be seen in Figure 5.11.



a) b)

Figure 5.11 a) Depiction of the computed assisted design of the 3x4 DMC. b) Built laboratory prototype of the 3x4 DMC (without output filter).

The transformer sized in Section 4.1 was built using the already pre-selected cores and a set of PCBs whose resultant designs can be observed in Appendix F, a depiction of the planar transformer prototype can be seen in Figure 5.12.



a) b)

Figure 5.12 Planar Transformer prototype: a) front view; b) top view.

The experimental results are divided into two subsections. First the current controller in 4.3 is tested in a single 3x4 DMC (considering only the equivelant χ DMC) and the non-linear

voltage controller is added along with output capacitors; Finally both converters are connected without a transformer using only a inductor to emulate the leakage inductance[8].

The commutation process was implemented in VHDL and compiled for a Xilinx® Kintex®-7 XC7K325T FPGA. The controller and modulator were implemented in Simulink and compiled for an NXP QorlQ P5020. Both hardware platforms are inside a Dspace MicroLabBox system. A diagram of the implemented commutation method is shown in Appendix E.

5.2.1 Current and Voltage control of the equivalent χ DMC

The laboratory setup for this set of experiments can be seen in Figure 5.12. The converter is connected to the grid via an autotransformer and an isolation transformer. A set of resistors with a manual switch are used to generate sags and swells controlled by the value of the resistance.

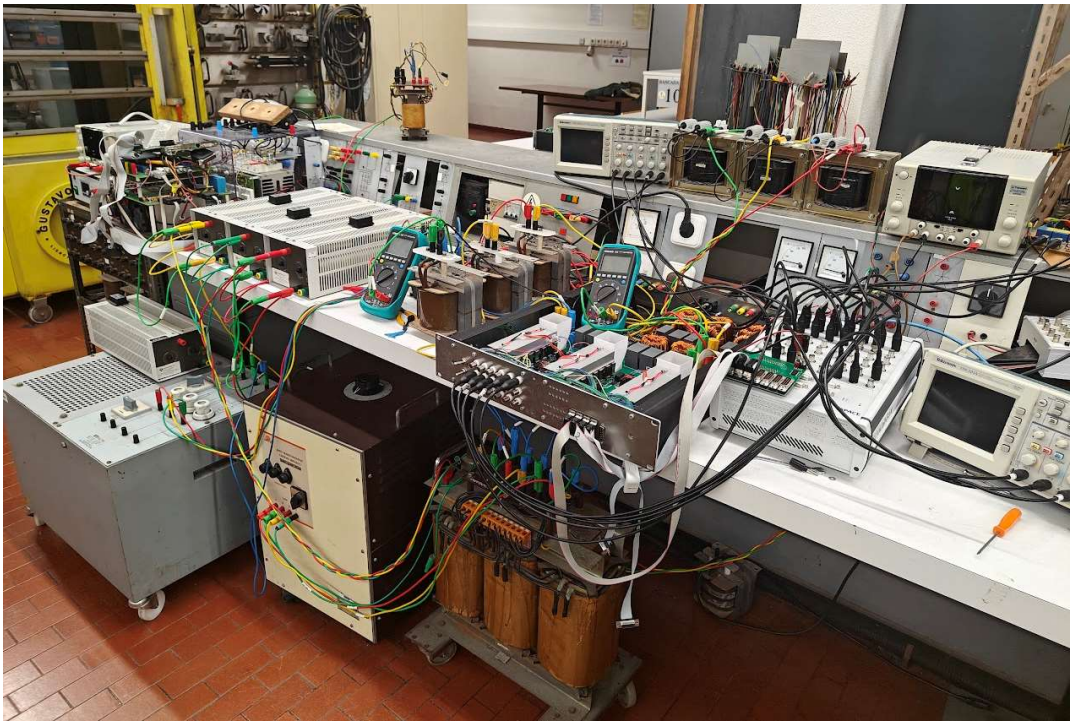
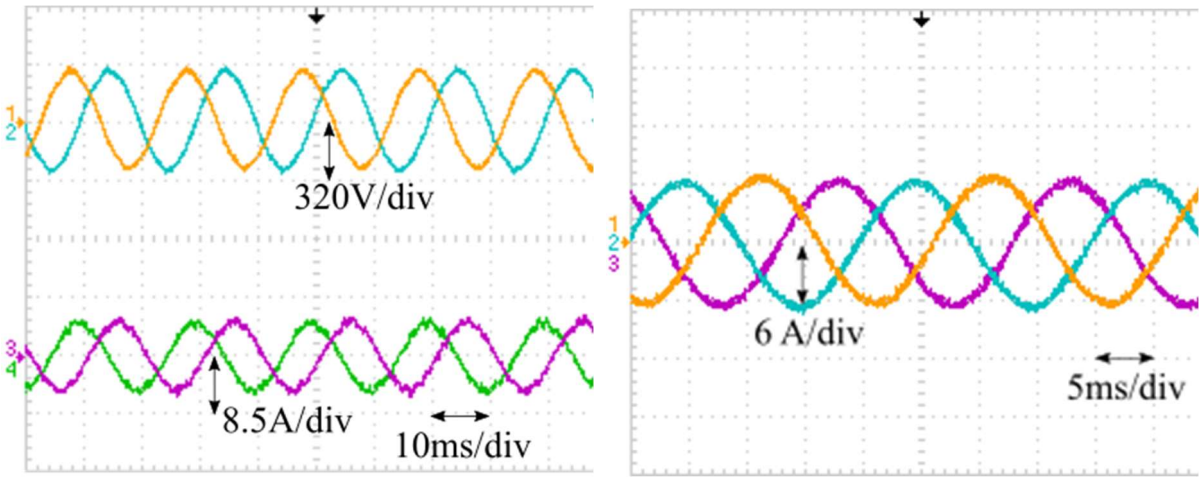


Figure 5.13 Laboratory setup with a single DMC supplying an unbalanced load.

The single DMC was first assembled without output capacitors, using only the MPC current controller and supplying an inductive load. The input voltage was set to 110V phase-to-neutral with an RL load with $R = 19\Omega$ and $L = 14\mu H$ for the output phases A and C and a load unbalance of about 25% in phase B ($R = 14.5\Omega$), the controller sample time was $17.5\mu s$. The

[8] Timming constraints on the acquisition of materials limited the available time to build and teste the planar transformer. Additional results are expected to be acquired by the time of the thesis final submission.

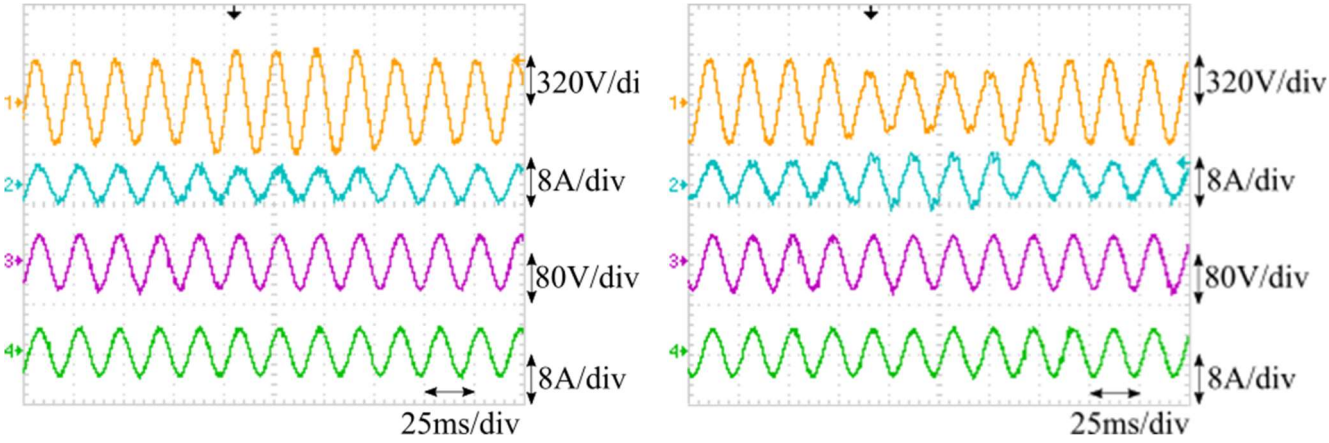
resulting waveforms are shown in Figure 5.13. Figure 5.13 a) shows the input voltages (v_{gbc} and v_{gca}) in yellow and green, respectively, and the input grid currents (i_b and i_c) in green and purple, respectively. The current controller is able to control the output currents under the load unbalanced with both sinusoidal input and output currents. The input grid voltages in the laboratory suffer from distortions on the 5th, 13th and 17th harmonics, giving them the triangular shape on the top of each phase-phase waveform. As a consequence, the peak values of the currents also suffer from a minor distortion; the current THD is still less than 5%.



a) b)

Figure 5.14 MPC current controller experimental results. a) v_{gbc} and v_{gca} input voltages in yellow and blue, respectively, and input grid currents i_{gb} and i_{gc} in green and purple, respectively. b) Output currents in output phases A, B, and C are yellow, blue, and purple, respectively.

An output capacitor was then placed after the filter inductors, and an unbalanced resistive load was supplied with the DMC with the voltage and current control loops. The input phase-to-neutral voltages were set to 110V, and the reference output phases to neutral voltages were set to 60V. In Figure 5.14, a balanced sag and swell of 30% can be observed; for both events, the grid voltage, v_{gbc} is depicted in yellow, the input grid current i_{gb} is shown in blue and the output voltage, v_{oBN}, and the output current, I_{LB}, are shown in purple and green respectively.

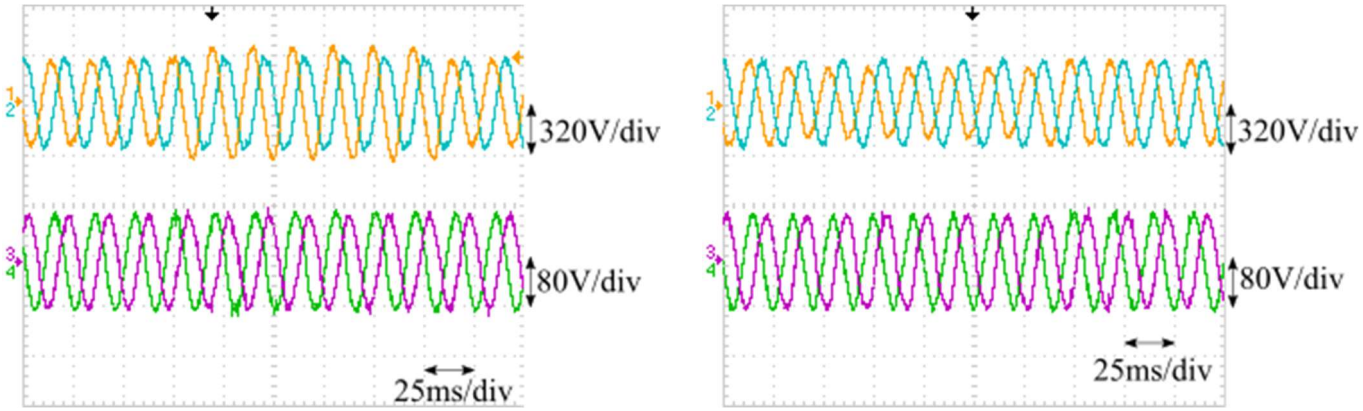


a) b)

Figure 5.15 Voltage and current control results. Input grid voltages v_{gbc}, input grid current i_{gb}, output voltage, v_{oBN} and output current i_{LB} shown respectively in yellow, blue, purple, and green. a) Balanced swell event with a duration of 4 grid periods. b) sag event with the duration of 4 grid periods.

The output voltages and currents remain unperturbed during the balanced sag and swell events.

Two additional sag and swell events are shown in Figure 5.15 this time unbalanced. For both Figure 5.15 a) and b) the input grid voltages v_{gbc} and v_{gca}, and the output voltages v_{oBN} and v_{oCN} are shown in yellow, blue, purple, and green, respectively.



a) b)

Figure 5.16 Voltage and current control results. Input grid voltages v_{gbc}, input grid voltage v_{gca}, output voltage, v_{oBN} and output voltages v_{oCN} shown respectively in yellow, blue, purple, and green. a) Unbalanced swell event during 6 grid periods. b) Unbalanced sag event during 7 grid periods.

Once again, during the sag and swell event, the output voltages remain unperturbed, showing the ability to mitigate the fault downstream.

The converter is shown operating with a 400V phase-phase input grid while the output voltages are regulated to 110V with an output load power of 3kW. This is shown in Figure 5.16, where the input grid voltage v_{gbc} is shown in yellow, the input current i_{gb} is shown in blue, the output current i_{LB} is shown in green and the output phase-to-neutral voltage v_{oBN} is shown in purple.

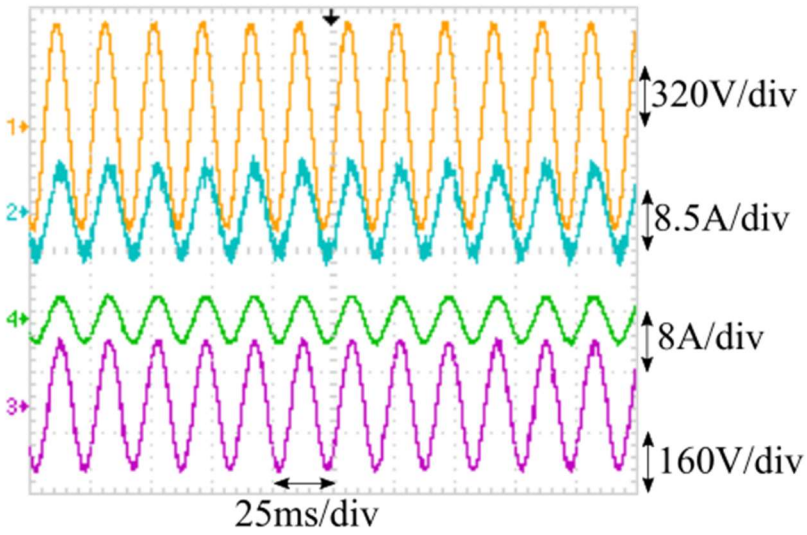
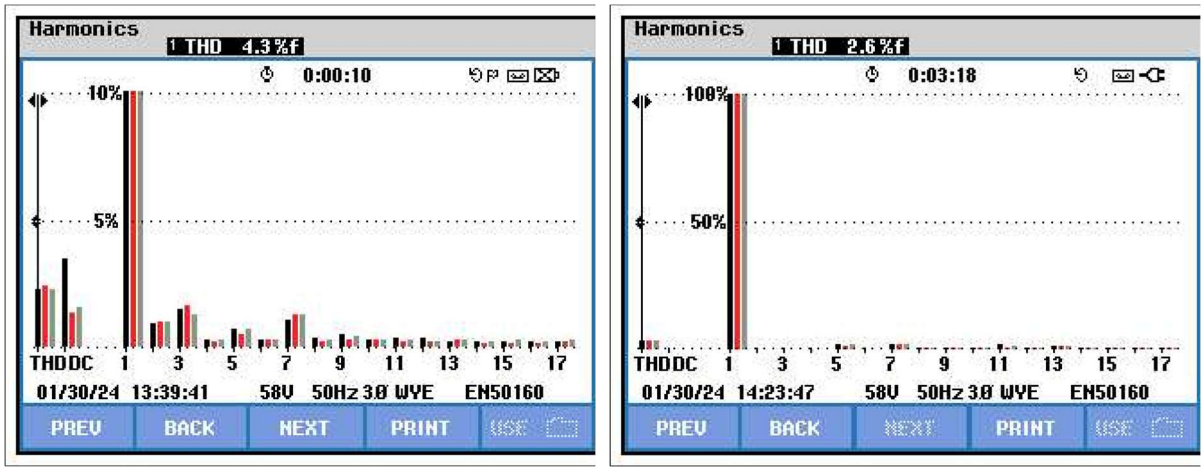


Figure 5.17 Waveforms of the converter operating with 400V Phase-to-Phase voltage with 110V of output phase to neutral voltage. Input grid voltage v_{gbc}, input current i_{gb}, output current i_{LB} and output phase-to-neutral voltage v_{oBN} are shown in blue, yellow, green and purple, respectively.

Finally, measurements of the input grid voltage and the output grid voltage THD are obtained with a power quality analyser (Fluke 423 Three-Phase Power Quality Analyzer). The results are shown in Figure 5.17. Notably, the converter is able to reduce the THD by 1.7%. The input grid THD is 4.3% while the output grid voltage THD is 2.6%, once again showing the ability of the proposed controllers to improve the downstream power quality.



a) b)

Figure 5.18 Harmonic distortion measurements with Fluke 435 Three-Phase power quality analyser.

5.2.2 Current and voltage control of the SST topology without transformer

The laboratory setup for the current and voltage control of the proposed SST topology can be seen in Figure 5.18. The 3x3 DMC and the 3x4 DMC are interconnected with three inductances of 300 nH to emulate the leakage inductance of the transformer.

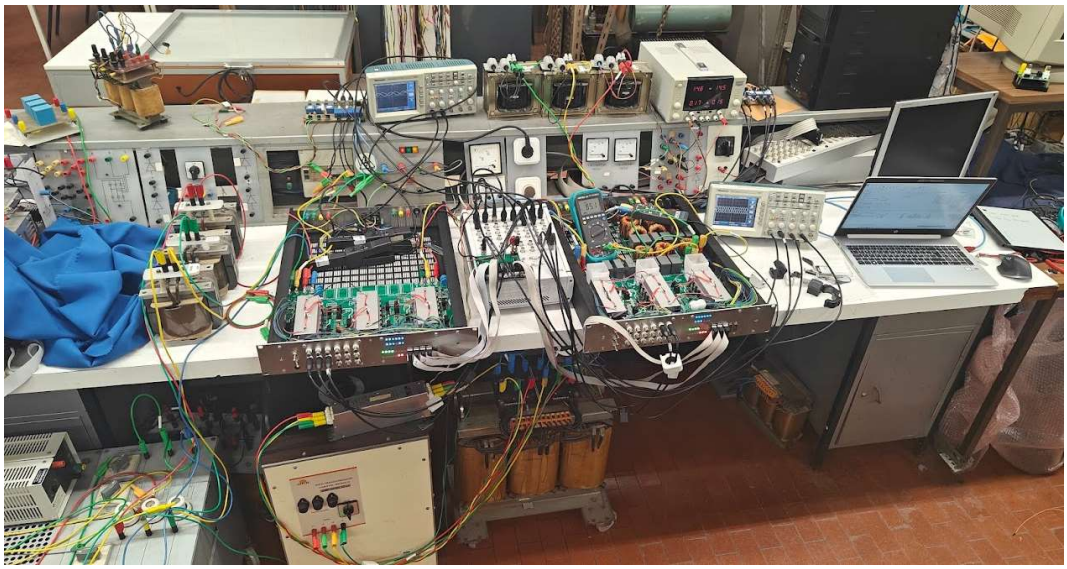
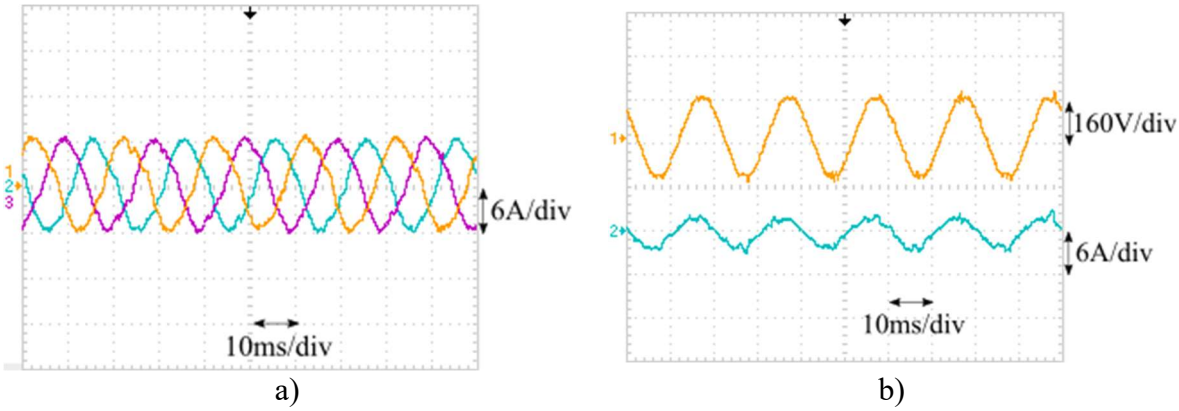


Figure 5.19 Laboratory setup with both DMCs supplying an unbalanced load (The transformer is replaced by its leakage inductance).

The planar manufacture of the transformer was delayed for reasons already highlighted; as such, preliminary results were obtained by replacing the planar transformer for its expected leakage inductance.

The SST is connected to the laboratory grid via an auto-transformer and an isolation transformer, the DQ reference frame is synchronised with the phase-to-neutral voltages at the output of the isolation transformer.

Firstly, the SST is controlled only with the predictive current controller setting the output currents to 4A RMS synchronous with the input voltages. The resulting waveforms can be seen in Figure 5.19. In Figure 5.19 a) the output currents can be observed which are controlled to be balanced despite the unbalanced load. In Figure 5.19 b) the input grid voltage and input grid current can be observed where the input current is controlled to be sinusoidal.



a) b)

Figure 5.20 Current control of the SST waveforms. a) Output currents i_{LA}, i_{LB}, i_{LC} in yellow, blue and purple, respectively. b) Input grid voltage v_{gbc} and input grid current i_{gb} in yellow and blue respectively.

Secondly, the output of the SST is connected to an LC filter ($L = 14mH$ and $C = 20\mu F$) supplying an unbalanced load. The SST is now controlled with both the current and voltage regulation. The output voltage is regulated to 50V phase-to-neutral voltage. The resulting waveforms can be observed in Figure 5.20. In Figure 5.20 a) the input grid phase-to-phase voltages, v_{gbc} and v_{gca}, can be observed along with the output phase-to-neutral voltages, v_{oB} and v_{oC}. The output voltages are regulated and controlled. Figure 5.20 b) shows the input grid voltage v_{ca} ,the input current i_{gc}; the output voltages v_{oC} and the load current i_{LC}. Figure 5.20 c) shows the output load currents, (i_{LA},i_{LB} and i_{LC}), where it is possible to observe that despite the load unbalance the output voltages are controlled to be balanced.

The results obtained show controlled output sinusoidal voltages with input sinusoidal current, validating the proposed control methodology.

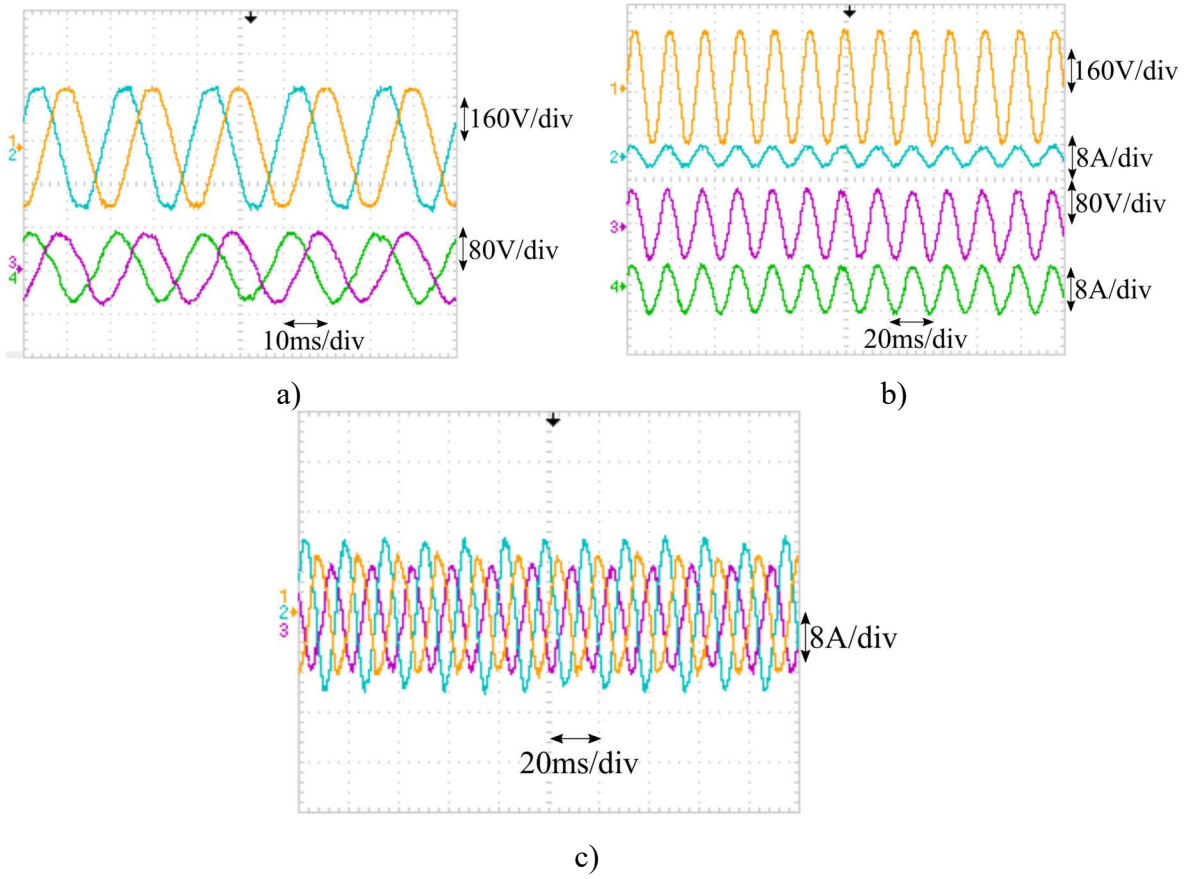


Figure 5.21 SST with voltage control experimental results. a) Input grid voltages v_{gbc} and v_{gca} and output voltages v_{oB} and v_{oC} in yellow, blue, purple and green, respectively. b) Input grid voltage v_{ca} , input current i_{gc}; output voltages v_{oC} and load current i_{LC} . in yellow, blue, purple, and green, respectively. c) output load currents i_{LA},i_{LB} and i_{LC} in yellow, blue, and purple respectively. (Scope in 4 sample average mode).

5.2.3 Current and voltage control of the full SST topology

The designed planar transformer was included in the experimental setup of Section 5.2.2 resulting in the experimental setup shown in Figure 5.22.

The obtained results are depicted in Figure 5.23. In Figure 5.23 a) the input voltages v_{bc} and v_{ca} are shown respectively in yellow and blue, while controlled output balanced sinusoidal voltages can be seen for v_{oB} and v_{oC} in purple and green, respectively. Figure 5.23 b) shows the input voltage v_{bc}, the input current i_{gb}, the output voltage v_{ob} and the output current i_{LB} in yellow, blue, purple and green respectively. Finally Figure 5.23 c) shows the primary and secondary phase to phase voltages applied to transformer, their almost squared behaviour is expected since the modulation method is continuously minimizing the timed integral of these voltages.

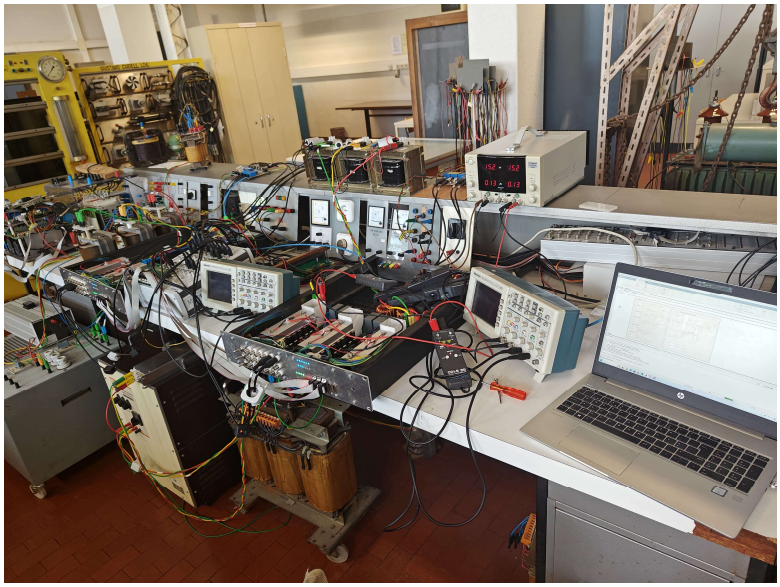


Figure 5.22 Laboratory setup with the full SST, including the planar transformer, supplying an unbalanced load

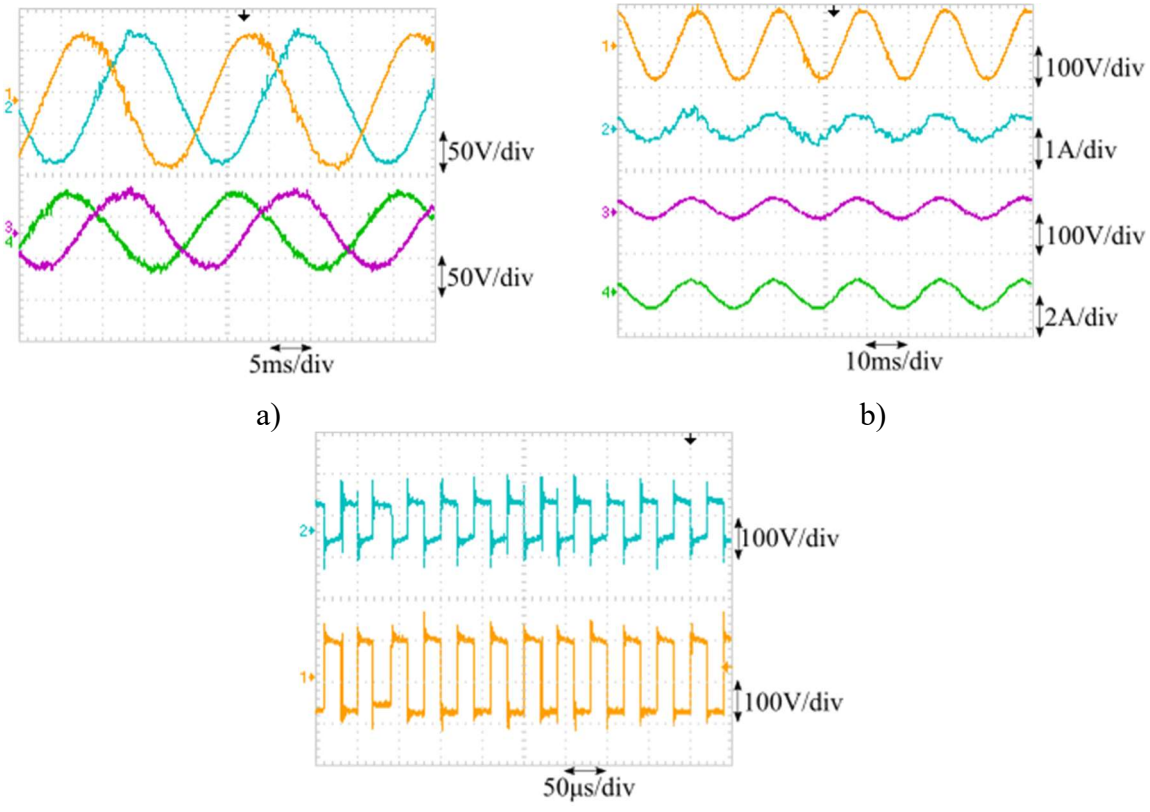


Figure 5.23 SST with voltage control experimental results. a) Input grid voltages v_{gbc} and v_{gca} and output voltages v_{oB} and v_{oC} in yellow, blue, purple and green, respectively. b) Input grid voltage v_{ca} , input current i_{gc}; output voltages v_{oC} and load current i_{LC} . in yellow, blue, purple, and green, respectively. c) Transformer voltages on the secondary v_{tAB} and on the primary v_{tab} in blue and yellow, respectively.

5.2.4 Experimental Results Discussion

The obtained results validate several of the contributions proposed in this thesis. Without the leakage tolerant commutation method, the current in the equivalent leakage inductors would not have been recirculated, which would have resulted in severe overvoltages across the semiconductors. The proposed control methodology provides a control action for a single 3x4 DMC; it is only due to the proposed modulation method that this control action can be unfolded for both DMCs. Without it, the association of both converters would not produce the obtained controlled output voltages and input currents. The obtained results using the planar transformer prototype validate the capability of the modulation method to minimize the flux in a way the converter can operate with no saturation.

Consequently, the results obtained validate the operation of the proposed methodology and the assumptions made for the development of the commutation, modulation, and control processes.

Experimental results can however be further improved. Due to unforeseen circumstances such as the global pandemic the amount of time available for the acquisition of experimental results was significantly decreased. As such and with the conditions available at the laboratory results with decreased voltage and power levels where preferred, meaning the converters where operating below their nominal power impacting the THD of the relevant voltages and currents.

Chapter 6

CONCLUSIONS AND FUTURE WORK

This chapter provides a set of considerations and conclusions extracted from the work developed for this PhD thesis. It then further extends to the expected future work that can be developed based on the models, algorithms, control and hardware developed throughout the development of this work.

6.1 Final Considerations

The aim of this work was to propose a high power density SST topology using state-of-the-art power converters along with adequate control methodologies and techniques for the proposed topology. Matrix converters were selected, given their interesting properties regarding power density and efficiency, for the SST topology presented in Figure 3.1. Along with the matrix converters' advantages, several challenges arose for their applicability to SSTs.

The first tackled challenge was to devise a modulation method that could simplify the output voltages and input currents control of the SST by abstracting the MF transformer. This was achieved by modelling the two converters and the transformer as a single matrix converter, as detailed in section 3.1. Promising results were obtained in simulation as long as the transformer parasitic components were small enough, which were taken into consideration when designing the transformer. Experimental results, although with the described limitations, proved the feasibility of the modulation methodology.

The second challenge lies deep in the topology of matrix converters, which require voltage sources at the input and current sources at the output. This posed issues for the commutation of the secondary side converter, for which, at the commutation time scale, the leakage inductance at the input behaves as a current source, and so does the output filter inductor. A novel commutation method was then devised to handle the circulation of the leakage energy in multi-phase transformers. This method was detailed in section 3.2, and some preliminary results were presented at a well-known IEEE conference [123]. Simulation results have shown the ability to

commutate the secondary side converter, with the main bottleneck being the number of intermediate steps that might be required, which consequently leads to longer commutation times. The number of intermediate steps was minimised by analysing all possible switching transitions. This resulted in a storable table in an FPGA ROM with around 100,000 positions, ensuring that the required commutation steps could be accessed in real-time. The experimental results showed that the secondary side converter was able to recirculate the leakage energy without resulting in overvoltages.

Higher-order filters were studied with the goal of further increasing the power density. Traditional high-order passive filter design methodologies for unmatched impedances of the load and source require solving sets of equations that do not always yield real values for the passive components. The problem was then formulated as an optimisation problem in which a genetic algorithm searched for a Pareto front with respect to the proximity of the filter response to an idealised frequency response and the energy stored in the filter. The obtained filter sizing showed a good response, allowing the stored filter energy to decrease by a factor of 4 when compared to a filter sizing that did not take the minimisation of the stored energy into account.

To minimise the leakage inductance, a planar transformer was designed and sized. The obtained transformer parameters were used in all the simulations presented in this thesis, showing, in a simulation environment, that the obtained parasitic components did not influence the modulation method and that the leakage inductance was within limits that enabled the converter to commutate in an appropriate timing for the selected switching frequency.

The dynamics of the selected filter topology were modelled and discretised, and a model predictive controller for the SST currents was developed. To control the output voltage, a non-linear on-load voltage controller was designed to obtain the reference output currents for the model predictive current controller. The proposed controller was tested in a simulation environment, highlighting the capability of regulating the output voltages with unbalanced loads and under sags and swell events.

Finally, two DMCs were sized, designed and built in order to attain experimental validation. The proposed controllers were tested with a single DMC, and the ability to mitigate different grid faults was shown. The experimental results obtained with the proposed topology showed promising results, validating the proposed modulation and commutation methodology.

The experimental setup was a massive challenge throughout this work, unforeseen circumstances led to a massive shortage of electronic components, increasing cost and increased lead times, this resulted in additional delays that limited the available time to obtain experimental results, by drastically increasing the required time to do once more

straightforward tasks (decreased availability of laboratory staff, electronic circuit redesigned due to non-availability of critical components).

6.2 Future Work

With the proposed modulation method, several redundant states exist for each equivalent χ converter state. These redundant states can be utilised for functions other than minimising the flux. Among them are the selection of states that minimise the number of required intermediate vectors to switch or the decrease of switching losses.

The commutation freewheeling time depends on the SST's output current, the leakage inductance, and the amplitude of the input voltages. An explicit measurement of the output currents and input voltages available on the FPGA would allow dynamic changes in the freewheeling time for each commutation, effectively reducing the commutation time.

The already developed primary controllers can be complemented with secondary and tertiary controllers to provide, e.g., reactive power grid support.

With the current experimental setup, EMC interference limits the quality of the results as well as the maximum operating voltage and current. Future improvements can include the increase of the gate driving resistors to decrease the commutation dv/dt, the inclusion of common mode filters and snubbers on bidirectional switches.

The discretised dynamics of the filter resulted in a controller model that must measure the input grid voltages and currents, the input converter currents and the output voltages and currents, as well as the intermediate filter stage currents and voltages. Approximations for these two last-mentioned measurements can be devised such that these two additional sets of measurements can be removed.

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APPENDIX A

3×4 DIRECT MATRIX CONVERTER TABLES OF STATES

Table A.1 3x4 DMC vector table (1 to 42).

№	$[S_{11}S_{12}S_{13}S_{21}S_{22}S_{23}S_{31}S_{32}S_{33}S_{41}S_{42}S_{43}]$	$\boldsymbol{v_A(t)}$	$\boldsymbol{v_B(t)}$	$\boldsymbol{v_C(t)}$	$\boldsymbol{v_N(t)}$	$\boldsymbol{i_a(t)}$	$\boldsymbol{i_b(t)}$	$\boldsymbol{i_c(t)}$
1	[1 0 0 0 1 0 0 1 0 0 1 0]	$v_a(t)$	$v_b(t)$	$v_b(t)$	$v_b(t)$	$i_A(t)$	$-i_A(t)$	0
2	[0 1 0 1 0 0 1 0 0 1 0 0]	$v_b(t)$	$v_a(t)$	$v_a(t)$	$v_a(t)$	$-i_A(t)$	$i_A(t)$	0
3	[0 1 0 0 0 1 0 0 1 0 0 1]	$v_b(t)$	$v_c(t)$	$v_c(t)$	$v_c(t)$	0	$i_A(t)$	$-i_A(t)$
4	[0 0 1 0 1 0 0 1 0 0 1 0]	$v_c(t)$	$v_b(t)$	$v_b(t)$	$v_b(t)$	0	$-i_A(t)$	$i_A(t)$
5	[0 0 1 1 0 0 1 0 0 1 0 0]	$v_c(t)$	$v_a(t)$	$v_a(t)$	$v_a(t)$	$-i_A(t)$	0	$i_A(t)$
6	[1 0 0 0 0 1 0 0 1 0 0 1]	$v_a(t)$	$v_c(t)$	$v_c(t)$	$v_c(t)$	$i_A(t)$	0	$-i_A(t)$
7	[0 1 0 1 0 0 0 1 0 0 1 0]	$v_b(t)$	$v_a(t)$	$v_b(t)$	$v_b(t)$	$i_B(t)$	$-i_B(t)$	0
8	[1 0 0 0 1 0 1 0 0 1 0 0]	$v_a(t)$	$v_b(t)$	$v_a(t)$	$v_a(t)$	$-i_B(t)$	$i_B(t)$	0
9	[0 0 1 0 1 0 0 0 1 0 0 1]	$v_c(t)$	$v_b(t)$	$v_c(t)$	$v_c(t)$	0	$i_B(t)$	$-i_B(t)$
10	[0 1 0 0 0 1 0 1 0 0 1 0]	$v_b(t)$	$v_c(t)$	$v_b(t)$	$v_b(t)$	0	$-i_B(t)$	$i_B(t)$
11	[1 0 0 0 0 1 1 0 0 1 0 0]	$v_a(t)$	$v_c(t)$	$v_a(t)$	$v_a(t)$	$-i_B(t)$	0	$i_B(t)$
12	[0 0 1 1 0 0 0 0 1 0 0 1]	$v_c(t)$	$v_a(t)$	$v_c(t)$	$v_c(t)$	$i_B(t)$	0	$-i_B(t)$
13	[0 1 0 0 1 0 1 0 0 0 1 0]	$v_b(t)$	$v_b(t)$	$v_a(t)$	$v_b(t)$	$i_C(t)$	$-i_C(t)$	0
14	[1 0 0 1 0 0 0 1 0 1 0 0]	$v_a(t)$	$v_a(t)$	$v_b(t)$	$v_a(t)$	$-i_C(t)$	$i_C(t)$	0
15	[0 0 1 0 0 1 0 1 0 0 0 1]	$v_c(t)$	$v_c(t)$	$v_b(t)$	$v_c(t)$	0	$i_C(t)$	$-i_C(t)$
16	[0 1 0 0 1 0 0 0 1 0 1 0]	$v_b(t)$	$v_b(t)$	$v_c(t)$	$v_b(t)$	0	$-i_C(t)$	$i_C(t)$
17	[1 0 0 1 0 0 0 0 1 1 0 0]	$v_a(t)$	$v_a(t)$	$v_c(t)$	$v_a(t)$	$-i_C(t)$	0	$i_C(t)$
18	[0 0 1 0 0 1 1 0 0 0 0 1]	$v_c(t)$	$v_c(t)$	$v_a(t)$	$v_c(t)$	$i_C(t)$	0	$-i_C(t)$
19	[1 0 0 1 0 0 0 1 0 0 1 0]	$v_a(t)$	$v_a(t)$	$v_b(t)$	$v_b(t)$	$i_A(t)+i_B(t)$	$i_C(t)+i_N(t)$	0
20	[0 1 0 0 1 0 1 0 0 1 0 0]	$v_b(t)$	$v_b(t)$	$v_a(t)$	$v_a(t)$	$i_C(t)+i_N(t)$	$i_A(t)+i_B(t)$	0
21	[0 1 0 0 1 0 0 0 1 0 0 1]	$v_b(t)$	$v_b(t)$	$v_c(t)$	$v_c(t)$	0	$i_A(t)+i_B(t)$	$i_C(t)+i_N(t)$
22	[0 0 1 0 0 1 0 1 0 0 1 0]	$v_c(t)$	$v_c(t)$	$v_b(t)$	$v_b(t)$	0	$i_C(t)+i_N(t)$	$i_A(t)+i_B(t)$
23	[0 0 1 0 0 1 1 0 0 1 0 0]	$v_c(t)$	$v_c(t)$	$v_a(t)$	$v_a(t)$	$i_C(t)+i_N(t)$	0	$i_A(t)+i_B(t)$
24	[1 0 0 1 0 0 0 0 1 0 0 1]	$v_a(t)$	$v_a(t)$	$v_c(t)$	$v_c(t)$	$i_A(t)+i_B(t)$	0	$i_C(t)+i_N(t)$
25	[0 1 0 1 0 0 1 0 0 0 1 0]	$v_b(t)$	$v_a(t)$	$v_a(t)$	$v_b(t)$	$i_B(t)+i_C(t)$	$i_A(t)+i_N(t)$	0
26	[1 0 0 0 1 0 0 1 0 1 0 0]	$v_a(t)$	$v_b(t)$	$v_b(t)$	$v_a(t)$	$i_A(t)+i_N(t)$	$i_B(t)+i_C(t)$	0
27	[0 0 1 0 1 0 0 1 0 0 0 1]	$v_c(t)$	$v_b(t)$	$v_b(t)$	$v_c(t)$	0	$i_B(t)+i_C(t)$	$i_A(t)+i_N(t)$
28	[0 1 0 0 0 1 0 0 1 0 1 0]	$v_b(t)$	$v_c(t)$	$v_c(t)$	$v_b(t)$	0	$i_A(t)+i_N(t)$	$i_B(t)+i_C(t)$
29	[1 0 0 0 0 1 0 0 1 1 0 0]	$v_a(t)$	$v_c(t)$	$v_c(t)$	$v_a(t)$	$i_A(t)+i_N(t)$	0	$i_B(t)+i_C(t)$
30	[0 0 1 1 0 0 1 0 0 0 0 1]	$v_c(t)$	$v_a(t)$	$v_a(t)$	$v_c(t)$	$i_B(t)+i_C(t)$	0	$i_A(t)+i_N(t)$
31	[1 0 0 0 1 0 1 0 0 0 1 0]	$v_a(t)$	$v_b(t)$	$v_a(t)$	$v_b(t)$	$i_A(t)+i_C(t)$	$i_B(t)+i_N(t)$	0
32	[0 1 0 1 0 0 0 1 0 1 0 0]	$v_b(t)$	$v_a(t)$	$v_b(t)$	$v_a(t)$	$i_B(t)+i_N(t)$	$i_A(t)+i_C(t)$	0
33	[0 1 0 0 0 1 0 1 0 0 0 1]	$v_b(t)$	$v_c(t)$	$v_b(t)$	$v_c(t)$	0	$i_A(t)+i_C(t)$	$i_B(t)+i_N(t)$
34	[0 0 1 0 1 0 0 0 1 0 1 0]	$v_c(t)$	$v_b(t)$	$v_c(t)$	$v_b(t)$	0	$i_B(t)+i_N(t)$	$i_A(t)+i_C(t)$
35	[0 0 1 1 0 0 0 0 1 1 0 0]	$v_c(t)$	$v_a(t)$	$v_c(t)$	$v_a(t)$	$i_B(t)+i_N(t)$	0	$i_A(t)+i_C(t)$
36	[1 0 0 0 0 1 1 0 0 0 0 1]	$v_a(t)$	$v_c(t)$	$v_a(t)$	$v_c(t)$	$i_A(t)+i_C(t)$	0	$i_B(t)+i_N(t)$
37	[1 0 0 1 0 0 1 0 0 0 1 0]	$v_a(t)$	$v_a(t)$	$v_a(t)$	$v_b(t)$	$-i_N(t)$	$i_N(t)$	0
38	[0 1 0 0 1 0 0 1 0 1 0 0]	$v_b(t)$	$v_b(t)$	$v_b(t)$	$v_a(t)$	$i_N(t)$	$-i_N(t)$	0
39	[0 1 0 0 1 0 0 1 0 0 0 1]	$v_b(t)$	$v_b(t)$	$v_b(t)$	$v_c(t)$	0	$i_N(t)$	$-i_N(t)$
40	[0 0 1 0 0 1 0 0 1 0 1 0]	$v_c(t)$	$v_c(t)$	$v_c(t)$	$v_b(t)$	0	$i_N(t)$	$-i_N(t)$
41	[0 0 1 0 0 1 0 0 1 1 0 0]	$v_c(t)$	$v_c(t)$	$v_c(t)$	$v_a(t)$	$i_N(t)$	0	$-i_N(t)$
42	[1 0 0 1 0 0 1 0 0 0 0 1]	$v_a(t)$	$v_a(t)$	$v_a(t)$	$v_c(t)$	$-i_N(t)$	0	$i_N(t)$

Table A.2 3x4 DMC vector table (43 to 81).

Nº	$[S_{11}S_{12}S_{13}S_{21}S_{22}S_{23}S_{31}S_{32}S_{33}S_{41}S_{42}S_{43}]$	$v_A(t)$	$v_B(t)$	$v_C(t)$	$v_N(t)$	$i_a(t)$	$i_b(t)$	$i_c(t)$
43	[1 0 0 1 0 0 0 0 1 0 1 0]	$v_a(t)$	$v_a(t)$	$v_c(t)$	$v_b(t)$	$i_A(t)+i_B(t)$	$i_N(t)$	$i_C(t)$
44	[0 1 0 0 1 0 0 0 1 1 0 0]	$v_b(t)$	$v_b(t)$	$v_c(t)$	$v_a(t)$	$i_N(t)$	$i_A(t)+i_B(t)$	$i_C(t)$
45	[0 1 0 0 1 0 1 0 0 0 0 1]	$v_b(t)$	$v_b(t)$	$v_a(t)$	$v_c(t)$	$i_C(t)$	$i_A(t)+i_B(t)$	$i_N(t)$
46	[0 0 1 0 0 1 1 0 0 0 1 0]	$v_c(t)$	$v_c(t)$	$v_a(t)$	$v_b(t)$	$i_C(t)$	$i_N(t)$	$i_A(t)+i_B(t)$
47	[0 0 1 0 0 1 0 1 0 1 0 0]	$v_c(t)$	$v_c(t)$	$v_b(t)$	$v_a(t)$	$i_N(t)$	$i_C(t)$	$i_A(t)+i_B(t)$
48	[1 0 0 1 0 0 0 1 0 0 0 1]	$v_a(t)$	$v_a(t)$	$v_b(t)$	$v_c(t)$	$i_A(t)+i_B(t)$	$i_C(t)$	$i_N(t)$
49	[1 0 0 0 0 1 1 0 0 0 1 0]	$v_a(t)$	$v_c(t)$	$v_a(t)$	$v_b(t)$	$i_A(t)+i_C(t)$	$i_N(t)$	$i_B(t)$
50	[0 1 0 0 0 1 0 1 0 1 0 0]	$v_b(t)$	$v_c(t)$	$v_b(t)$	$v_a(t)$	$i_N(t)$	$i_A(t)+i_C(t)$	$i_B(t)$
51	[0 1 0 1 0 0 0 1 0 0 0 1]	$v_b(t)$	$v_a(t)$	$v_b(t)$	$v_c(t)$	$i_B(t)$	$i_A(t)+i_C(t)$	$i_N(t)$
52	[0 0 1 1 0 0 0 0 1 0 1 0]	$v_c(t)$	$v_a(t)$	$v_c(t)$	$v_b(t)$	$i_B(t)$	$i_N(t)$	$i_A(t)+i_C(t)$
53	[0 0 1 0 1 0 0 0 1 1 0 0]	$v_c(t)$	$v_b(t)$	$v_c(t)$	$v_a(t)$	$i_N(t)$	$i_B(t)$	$i_A(t)+i_C(t)$
54	[1 0 0 0 1 0 1 0 0 0 0 1]	$v_a(t)$	$v_b(t)$	$v_a(t)$	$v_c(t)$	$i_A(t)+i_C(t)$	$i_B(t)$	$i_N(t)$
55	[1 0 0 0 0 1 0 0 1 0 1 0]	$v_a(t)$	$v_c(t)$	$v_c(t)$	$v_b(t)$	$i_A(t)$	$i_N(t)$	$i_B(t)+i_C(t)$
56	[0 1 0 0 0 1 0 0 1 1 0 0]	$v_b(t)$	$v_c(t)$	$v_c(t)$	$v_a(t)$	$i_N(t)$	$i_A(t)$	$i_B(t)+i_C(t)$
57	[0 1 0 1 0 0 1 0 0 0 0 1]	$v_b(t)$	$v_a(t)$	$v_a(t)$	$v_c(t)$	$i_B(t)+i_C(t)$	$i_A(t)$	$i_N(t)$
58	[0 0 1 1 0 0 1 0 0 0 1 0]	$v_c(t)$	$v_a(t)$	$v_a(t)$	$v_b(t)$	$i_B(t)+i_C(t)$	$i_N(t)$	$i_A(t)$
59	[0 0 1 0 1 0 0 1 0 1 0 0]	$v_c(t)$	$v_b(t)$	$v_b(t)$	$v_a(t)$	$i_N(t)$	$i_B(t)+i_C(t)$	$i_A(t)$
60	[1 0 0 0 1 0 0 1 0 0 0 1]	$v_a(t)$	$v_b(t)$	$v_b(t)$	$v_c(t)$	$i_A(t)$	$i_B(t)+i_C(t)$	$i_N(t)$
61	[1 0 0 0 1 0 0 0 1 1 0 0]	$v_a(t)$	$v_b(t)$	$v_c(t)$	$v_a(t)$	$i_A(t)+i_N(t)$	$i_B(t)$	$i_C(t)$
62	[1 0 0 0 1 0 0 0 1 0 1 0]	$v_a(t)$	$v_b(t)$	$v_c(t)$	$v_b(t)$	$i_A(t)$	$i_B(t)+i_N(t)$	$i_C(t)$
63	[1 0 0 0 1 0 0 0 1 0 0 1]	$v_a(t)$	$v_b(t)$	$v_c(t)$	$v_c(t)$	$i_A(t)$	$i_B(t)$	$i_C(t)+i_N(t)$
64	[1 0 0 0 0 1 0 1 0 1 0 0]	$v_a(t)$	$v_c(t)$	$v_b(t)$	$v_a(t)$	$i_A(t)+i_N(t)$	$i_C(t)$	$i_B(t)$
65	[1 0 0 0 0 1 0 1 0 0 1 0]	$v_a(t)$	$v_c(t)$	$v_b(t)$	$v_b(t)$	$i_A(t)$	$i_C(t)+i_N(t)$	$i_B(t)$
66	[1 0 0 0 0 1 0 1 0 0 0 1]	$v_a(t)$	$v_c(t)$	$v_b(t)$	$v_c(t)$	$i_A(t)$	$i_C(t)$	$i_B(t)+i_N(t)$
67	[0 1 0 1 0 0 0 0 1 1 0 0]	$v_b(t)$	$v_a(t)$	$v_c(t)$	$v_a(t)$	$i_B(t)+i_N(t)$	$i_A(t)$	$i_C(t)$
68	[0 1 0 1 0 0 0 0 1 0 1 0]	$v_b(t)$	$v_a(t)$	$v_c(t)$	$v_b(t)$	$i_B(t)$	$i_A(t)+i_N(t)$	$i_C(t)$
69	[0 1 0 1 0 0 0 0 1 0 0 1]	$v_b(t)$	$v_a(t)$	$v_c(t)$	$v_c(t)$	$i_B(t)$	$i_A(t)$	$i_C(t)+i_N(t)$
70	[0 1 0 0 0 1 1 0 0 1 0 0]	$v_b(t)$	$v_c(t)$	$v_a(t)$	$v_a(t)$	$i_C(t)+i_N(t)$	$i_A(t)$	$i_B(t)$
71	[0 1 0 0 0 1 1 0 0 0 1 0]	$v_b(t)$	$v_c(t)$	$v_a(t)$	$v_b(t)$	$i_C(t)$	$i_A(t)+i_N(t)$	$i_B(t)$
72	[0 1 0 0 0 1 1 0 0 0 0 1]	$v_b(t)$	$v_c(t)$	$v_a(t)$	$v_c(t)$	$i_C(t)$	$i_A(t)$	$i_B(t)+i_N(t)$
73	[0 0 1 1 0 0 0 1 0 1 0 0]	$v_c(t)$	$v_a(t)$	$v_b(t)$	$v_a(t)$	$i_B(t)+i_N(t)$	$i_C(t)$	$i_A(t)$
74	[0 0 1 1 0 0 0 1 0 0 1 0]	$v_c(t)$	$v_a(t)$	$v_b(t)$	$v_b(t)$	$i_B(t)$	$i_C(t)+i_N(t)$	$i_A(t)$
75	[0 0 1 1 0 0 0 1 0 0 0 1]	$v_c(t)$	$v_a(t)$	$v_b(t)$	$v_c(t)$	$i_B(t)$	$i_C(t)$	$i_A(t)+i_N(t)$
76	[0 0 1 0 1 0 1 0 0 1 0 0]	$v_c(t)$	$v_b(t)$	$v_a(t)$	$v_a(t)$	$i_C(t)+i_N(t)$	$i_B(t)$	$i_A(t)$
77	[0 0 1 0 1 0 1 0 0 0 1 0]	$v_c(t)$	$v_b(t)$	$v_a(t)$	$v_b(t)$	$i_C(t)$	$i_B(t)+i_N(t)$	$i_A(t)$
78	[0 0 1 0 1 0 1 0 0 0 0 1]	$v_c(t)$	$v_b(t)$	$v_a(t)$	$v_c(t)$	$i_C(t)$	$i_B(t)$	$i_A(t)+i_N(t)$
79	[1 0 0 1 0 0 1 0 0 1 0 0]	$v_a(t)$	$v_a(t)$	$v_a(t)$	$v_a(t)$	0	0	0
80	[0 1 0 0 1 0 0 1 0 0 1 0]	$v_b(t)$	$v_b(t)$	$v_b(t)$	$v_b(t)$	0	0	0
81	[0 0 1 0 0 1 0 0 1 0 0 1]	$v_c(t)$	$v_c(t)$	$v_c(t)$	$v_c(t)$	0	0	0

APPENDIX B

USEFUL TRANSFORMS

B1. $\alpha\mathbf{B}\gamma$ Transform

An abc reference frame can be transformed to a $\alpha\beta\gamma$ reference frame, in a power invariant manner, by using the Concordia transformation in (1.2) by the relation in (1.1).

$$X_{\alpha\beta\gamma} = \mathbf{C}^T X_{abc} \tag{1.1}$$

$$\mathbf{C} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{1.2}$$

Similarly, an $\alpha\beta\gamma$ reference frame can be transformed into an abc reference frame by using the inverse of the Concordia transformation in (1.4) by the relation in (1.3).

$$X_{abc} = \left(\mathbf{C}^{-1}\right)^T X_{\alpha\beta\gamma} \tag{1.3}$$

$$\mathbf{C}^{-1} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \end{bmatrix} \tag{1.4}$$

B2. Dq0 Transform

A $\alpha\beta\gamma$ reference frame can be transformed to a $dq0$ reference frame, by using the Park transformation in (1.6) by the relation in (1.5).

$$X_{dq0} = \mathbf{D}^T X_{\alpha\beta\gamma} \tag{1.5}$$

$$\mathbf{D} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) & 0 \\ \sin(\omega t) & \cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{1.6}$$

Similarly, a $dq0$ reference frame can be transformed to an $\alpha\beta\gamma$ reference frame, by using the inverse Park transformation in (1.8) by the relation in (1.7).

$$X_{\alpha\beta\gamma} = \left(\mathbf{D}^{-1}\right)^T X_{dq0} \tag{1.7}$$

$$\mathbf{D}^{-1} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) & 0 \\ -\sin(\omega t) & \cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{1.8}$$

APPENDIX C

MATRIX CONVERTER DESIGN

This appendix collects the schematic drawings with respective component values as well as the PCB layers design for the developed PCB boards. They are comprised of the following PCBs: Matrix Converter (3x4 DMC with 12 bidirectional switches, gate drivers, temperature sensing, input voltage and output current measurements and polarity signals); Input filter (Filter components, temperature sensing, input current and voltage measurement); IO Interface 1 (Interface for all analogical signals); IO interface 2 (Interface for all digital signals and light indications); AC/DC Converter (AC/DC converter from 230VAC to 24VDC to supply all boards); Signal Matching (Interface with Dspace MiroLabBox).

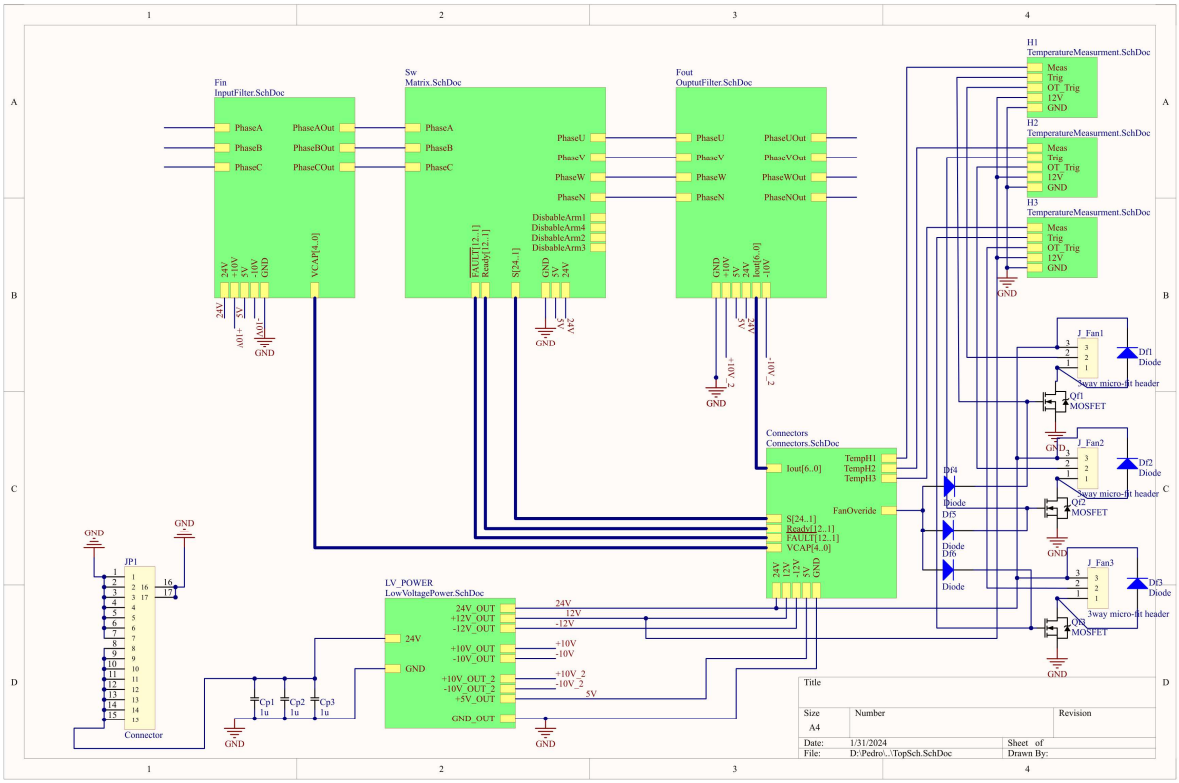

Figure C.1 Matrix Converter: Top schematic with input/output measurements, matrix converter, temperature measurements and cooling triggers.

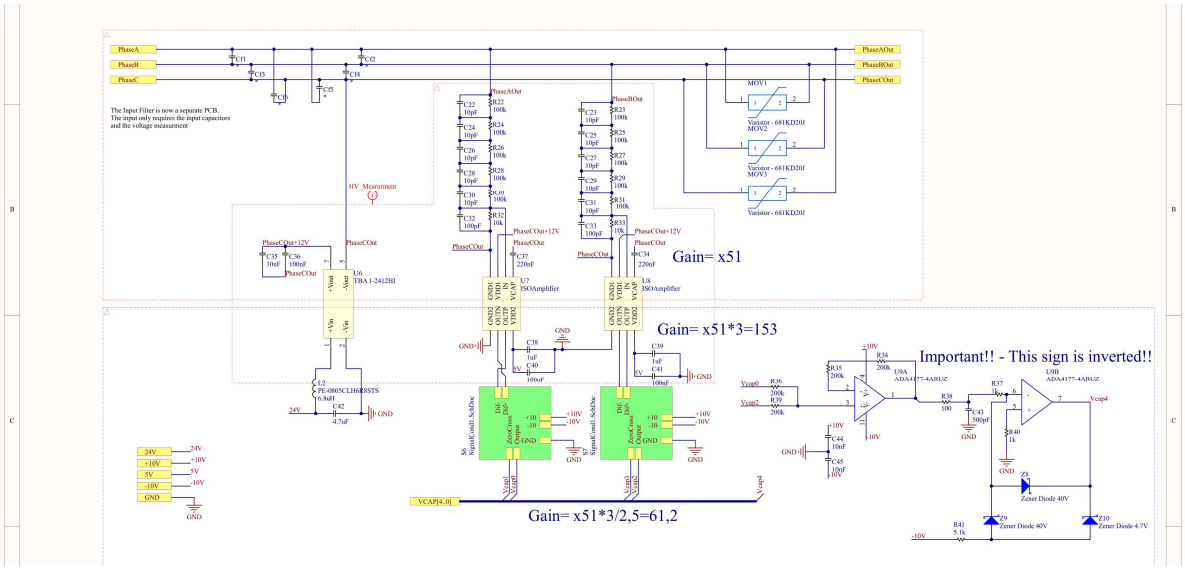

Figure C.2 Matrix Converter: Input voltage and current measurements and polarity signal generation.

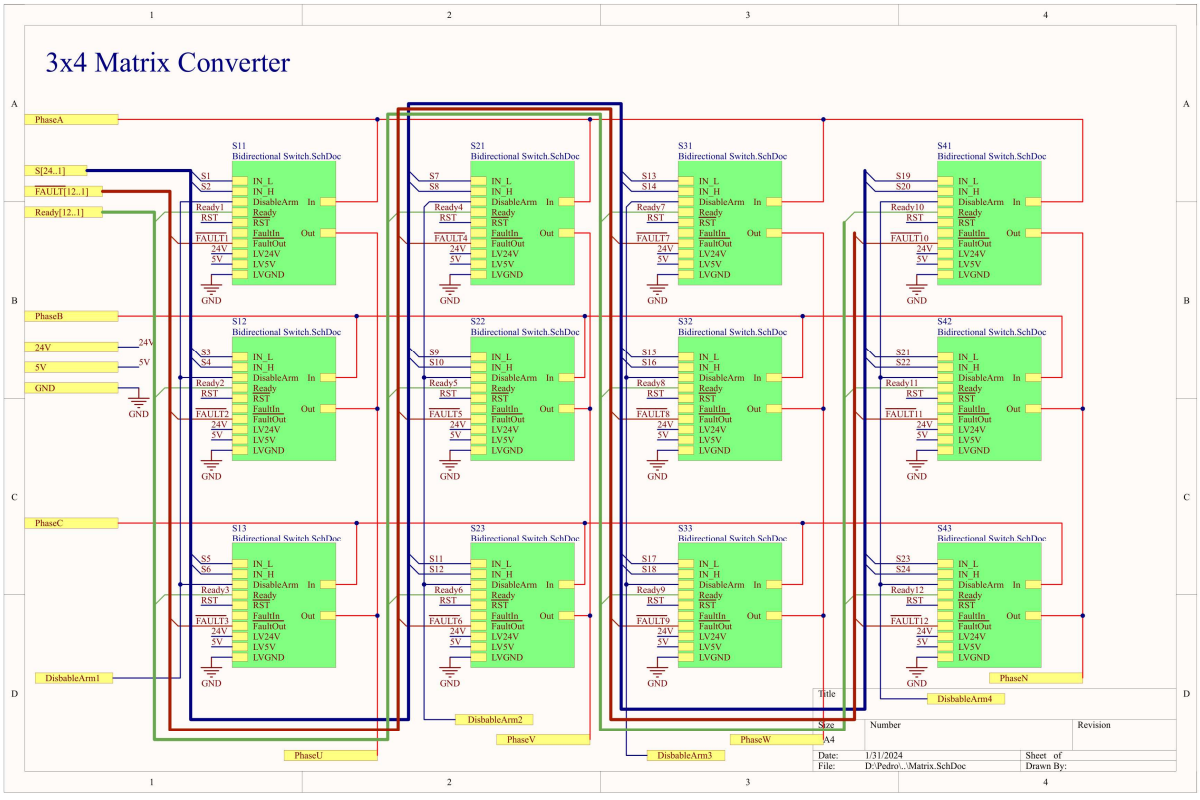

Figure C.3 Matrix Converter: Interconnection of the 12 bidirectional switches trigger and protection signals.

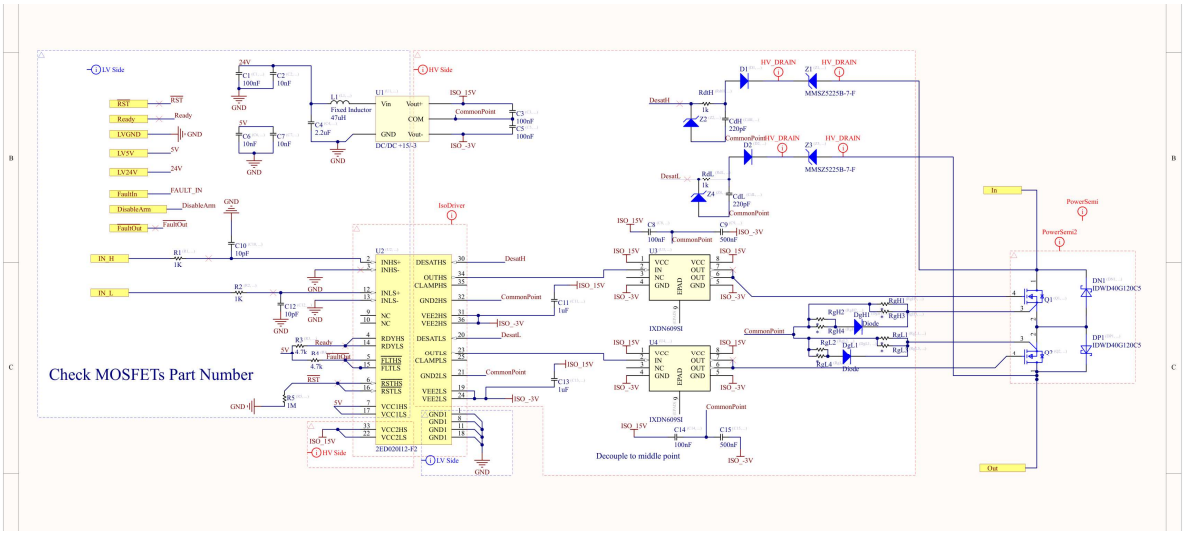

Figure C.4 Matrix Converter: Gate driver and protection schematics

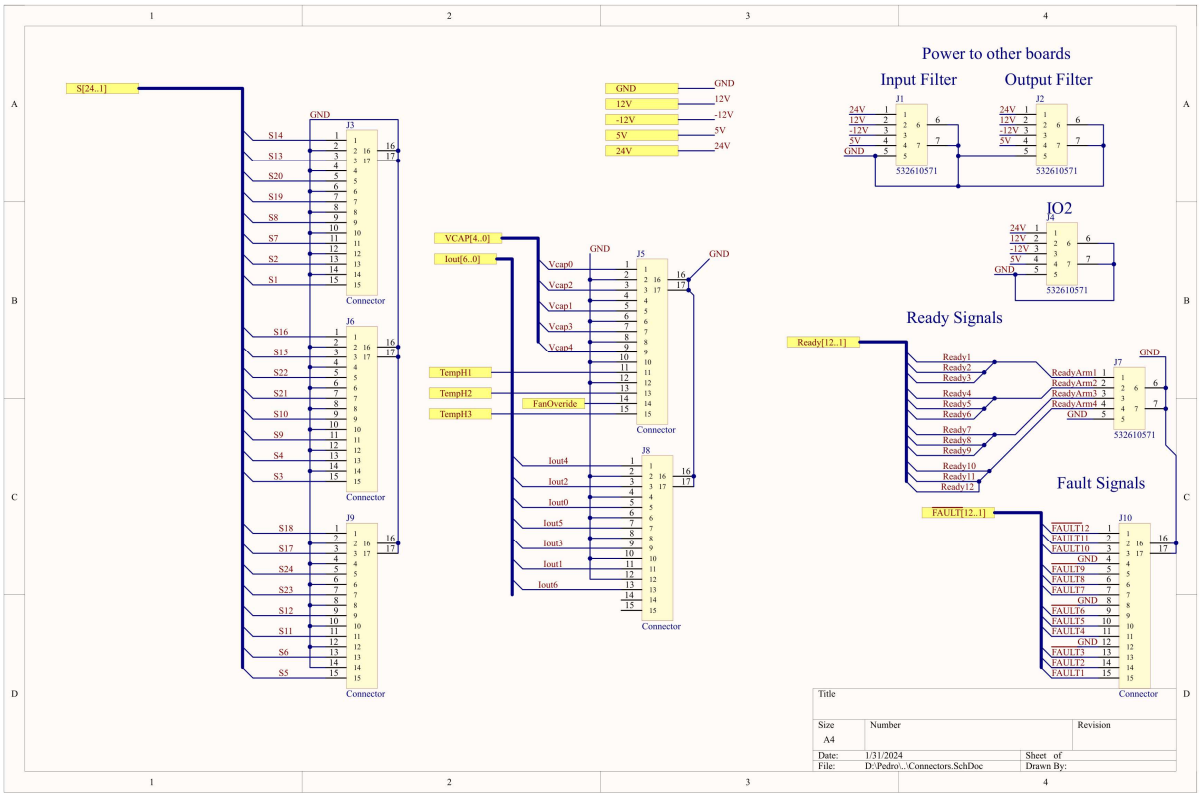

Figure C.5 Matrix Converter: Connections for the IO1, IO2, Input filter and supply boards.

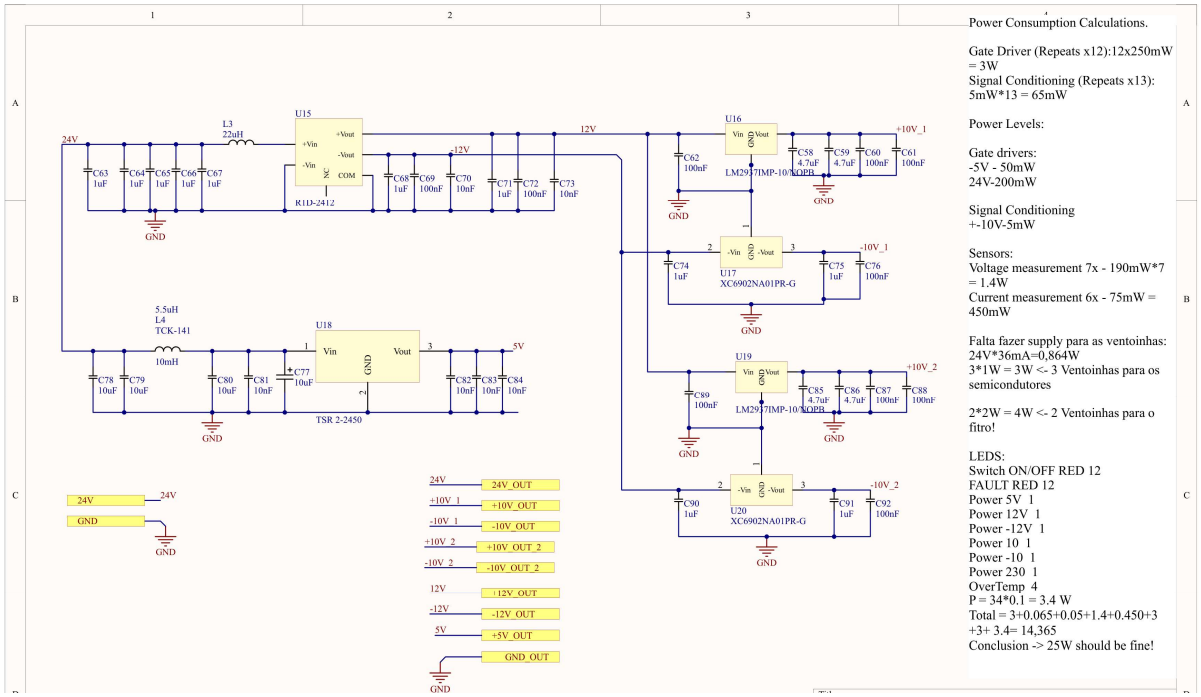

Figure C.6 Matrix Converter: Power distribution schematic 24V to - +12V/-12V, +10V/-10V, 5V.

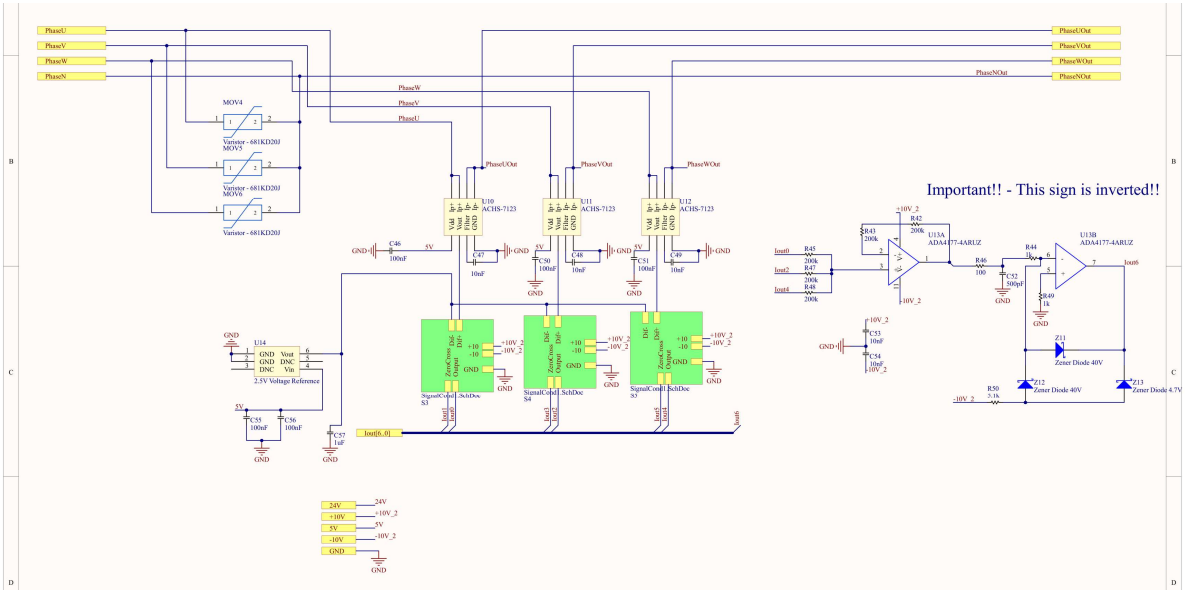

Figure C.7 Matrix Converter: Output current measurements and polarity signal generation schematic.

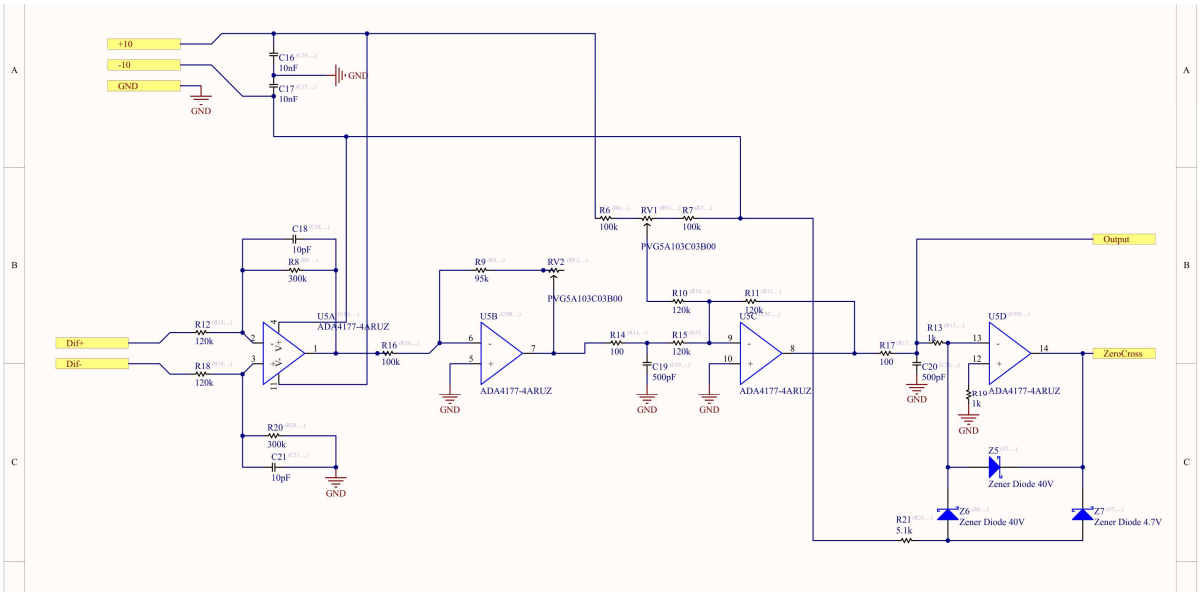

Figure C.8 Matrix Converter: Signal conditioning circuit schematic with gain and offset control.

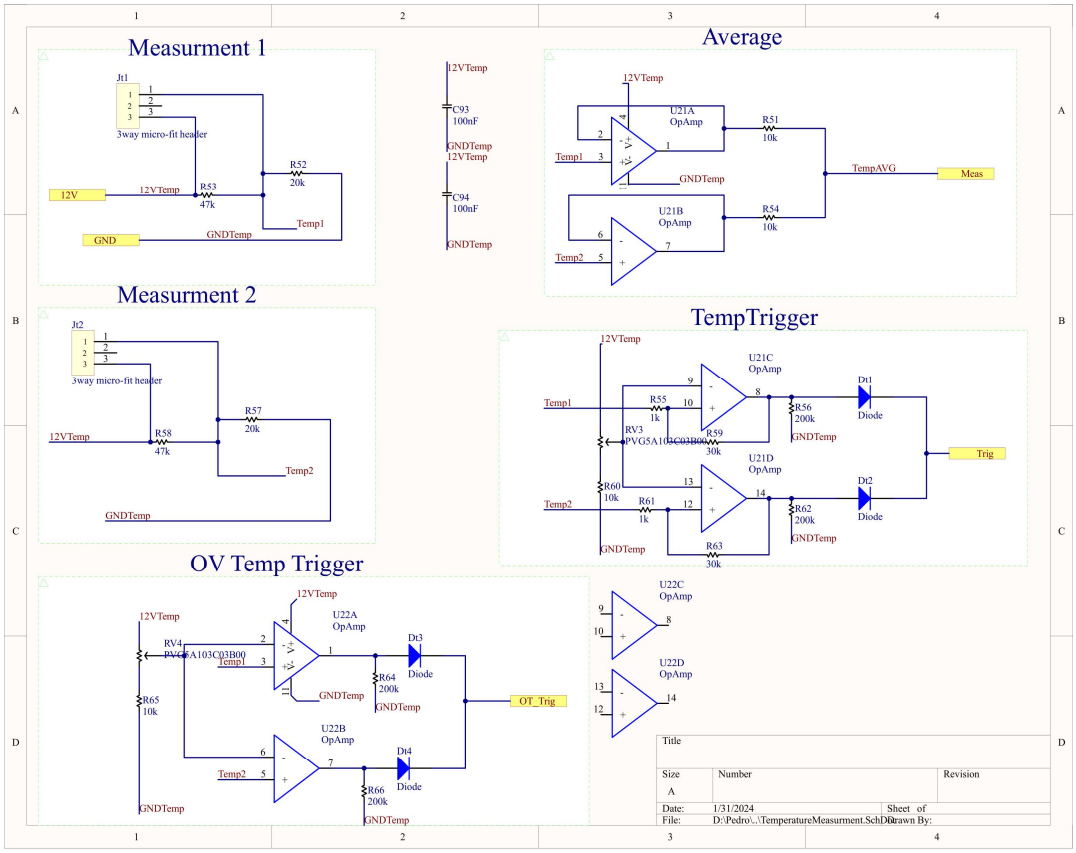

Figure C.9 Matrix Converter: Temperature measurements and triggers for overtemperature and fan turn-on schematic.

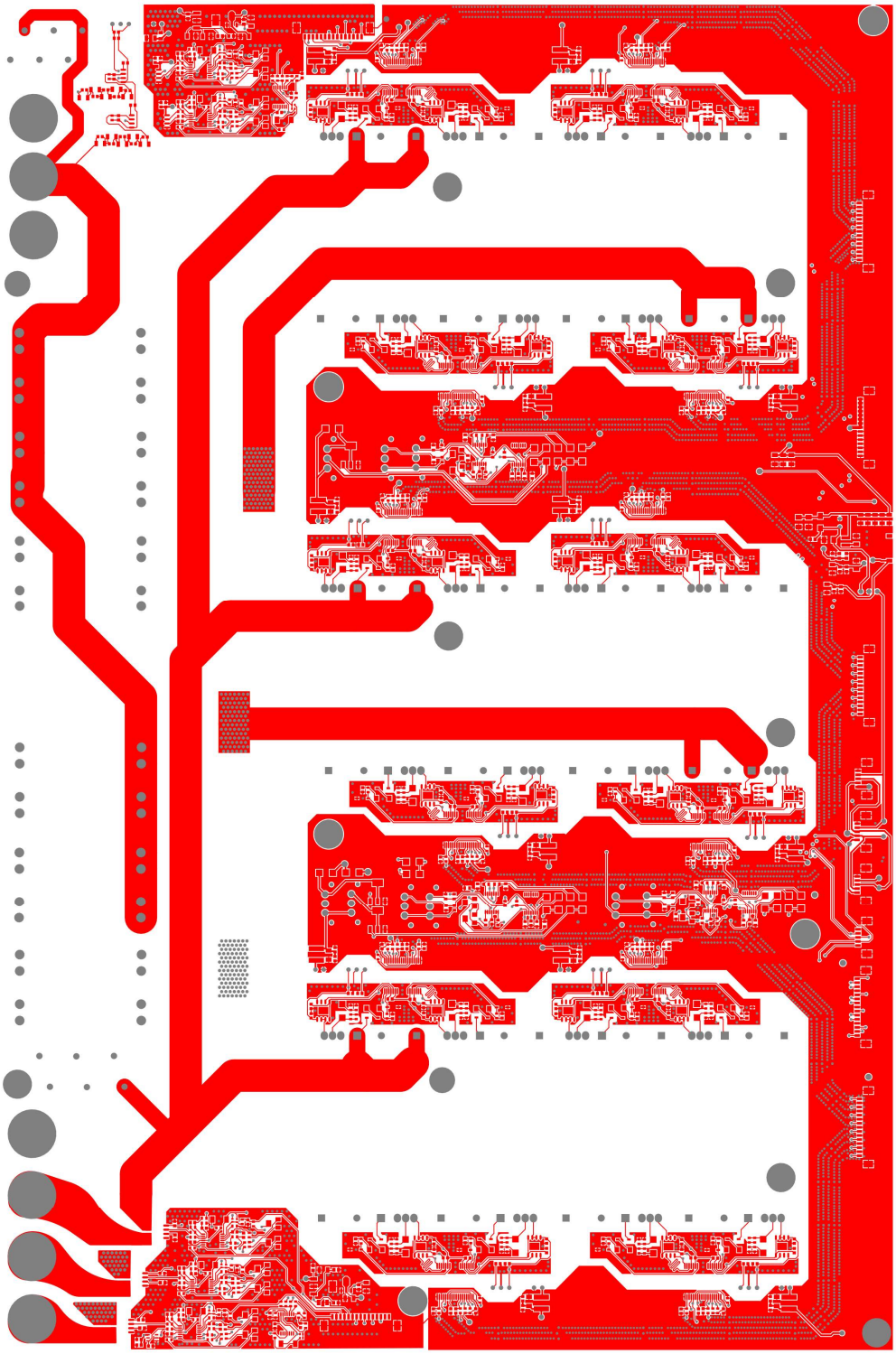

Figure C.10 Matrix Converter PCB: Top layer schematic

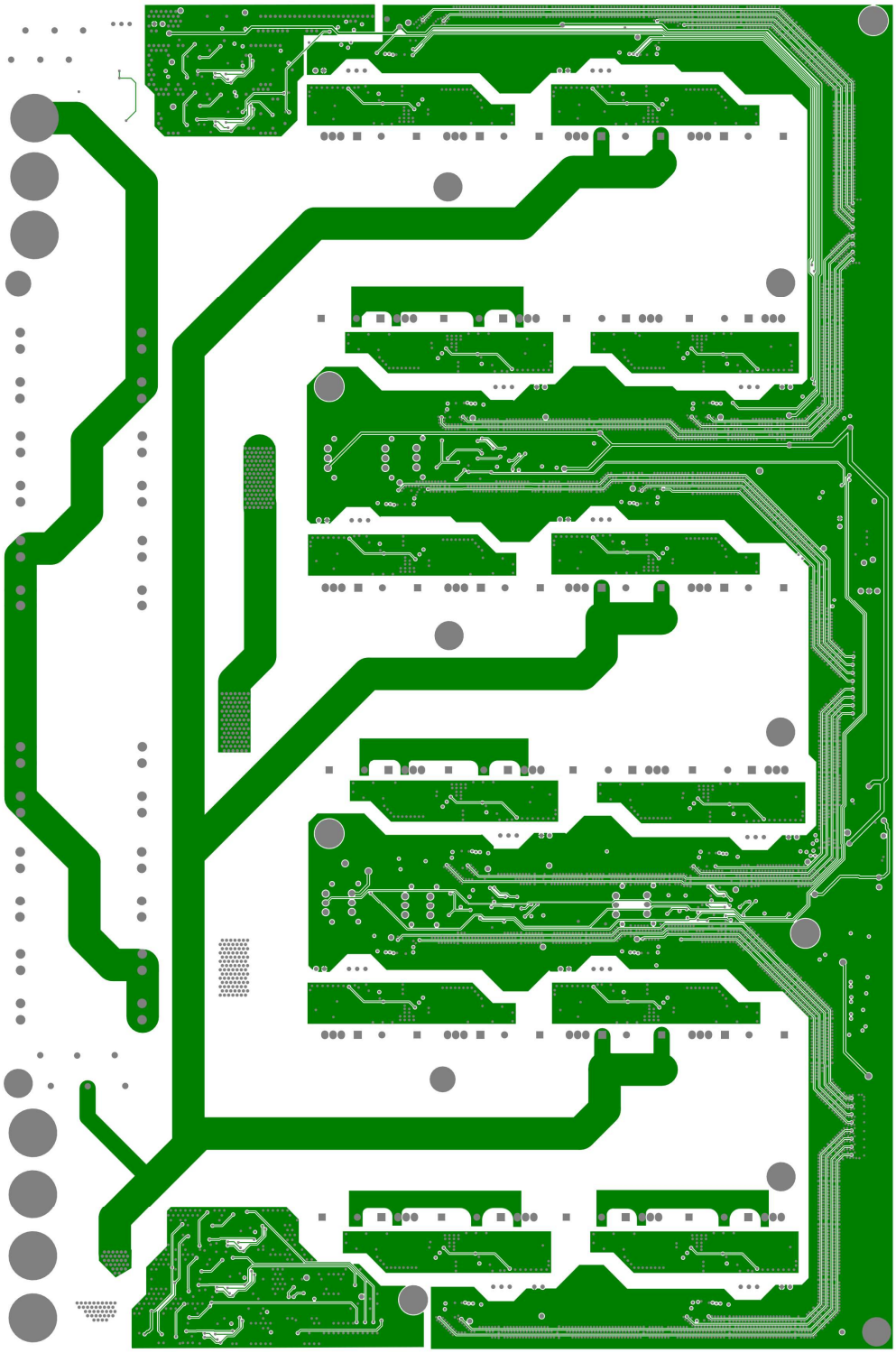

Figure C.11 Matrix Converter PCB: Inner layer 1 schematic

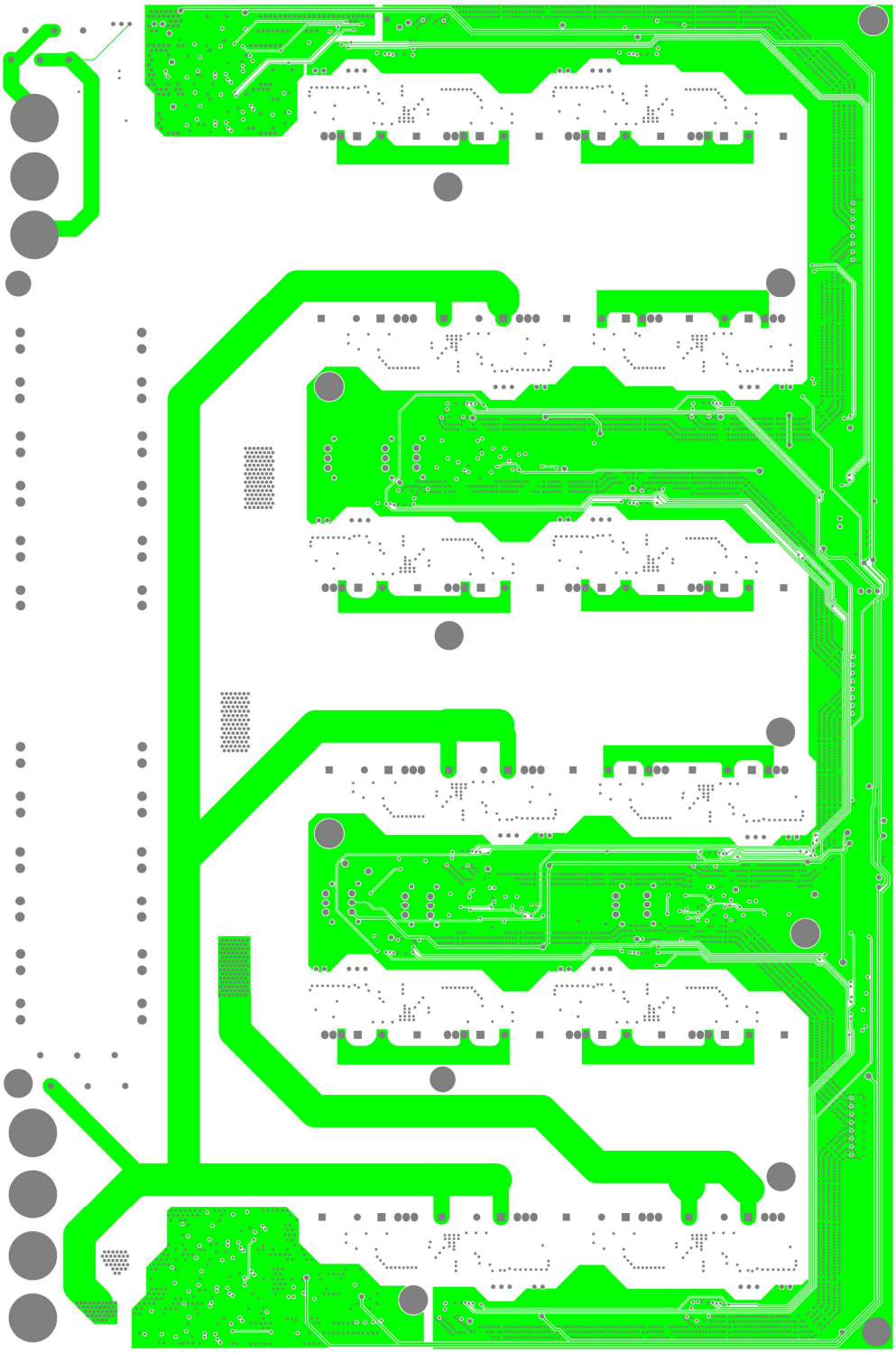

Figure C.12 Matrix Converter PCB: Inner layer 2 schematic

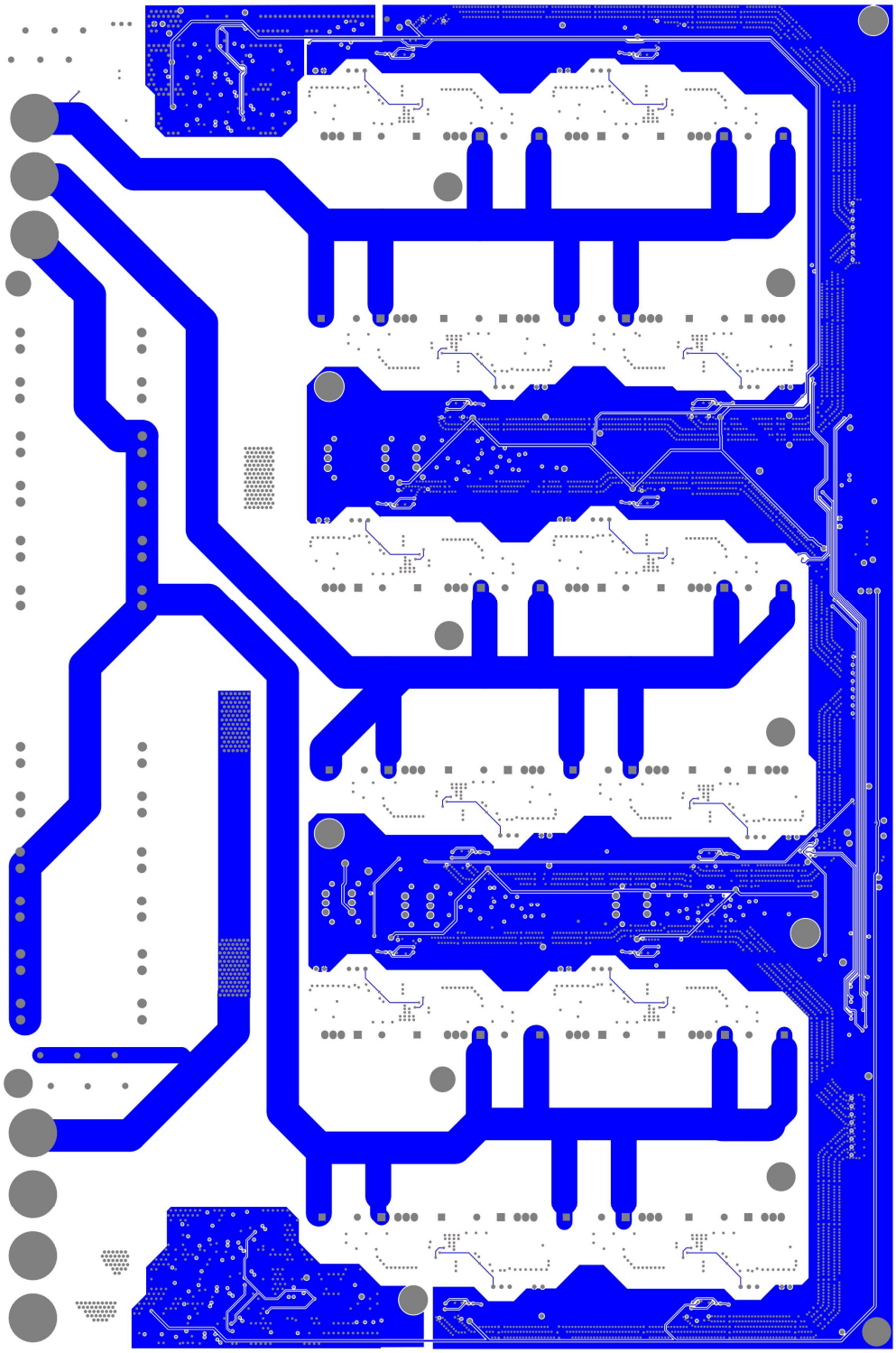

Figure C.13 Matrix Converter PCB: Bottom layer schematic.

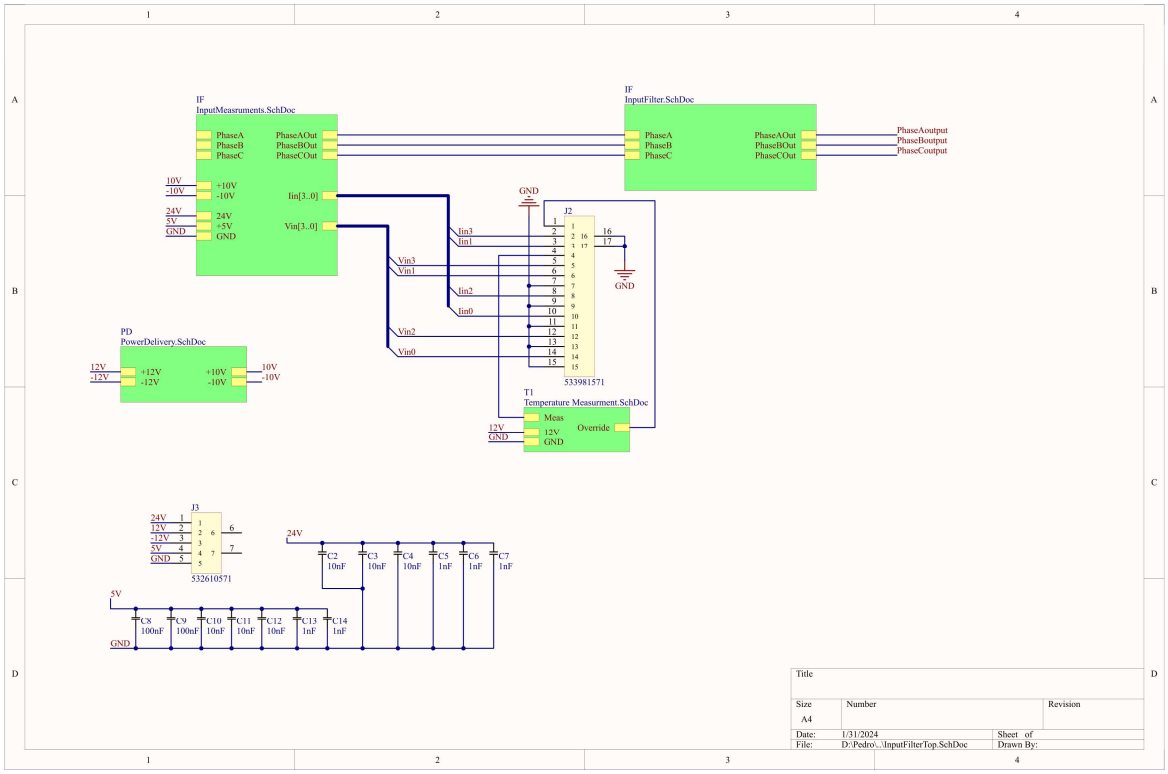

Figure C.14 Input Filter: Input filter top schematic.

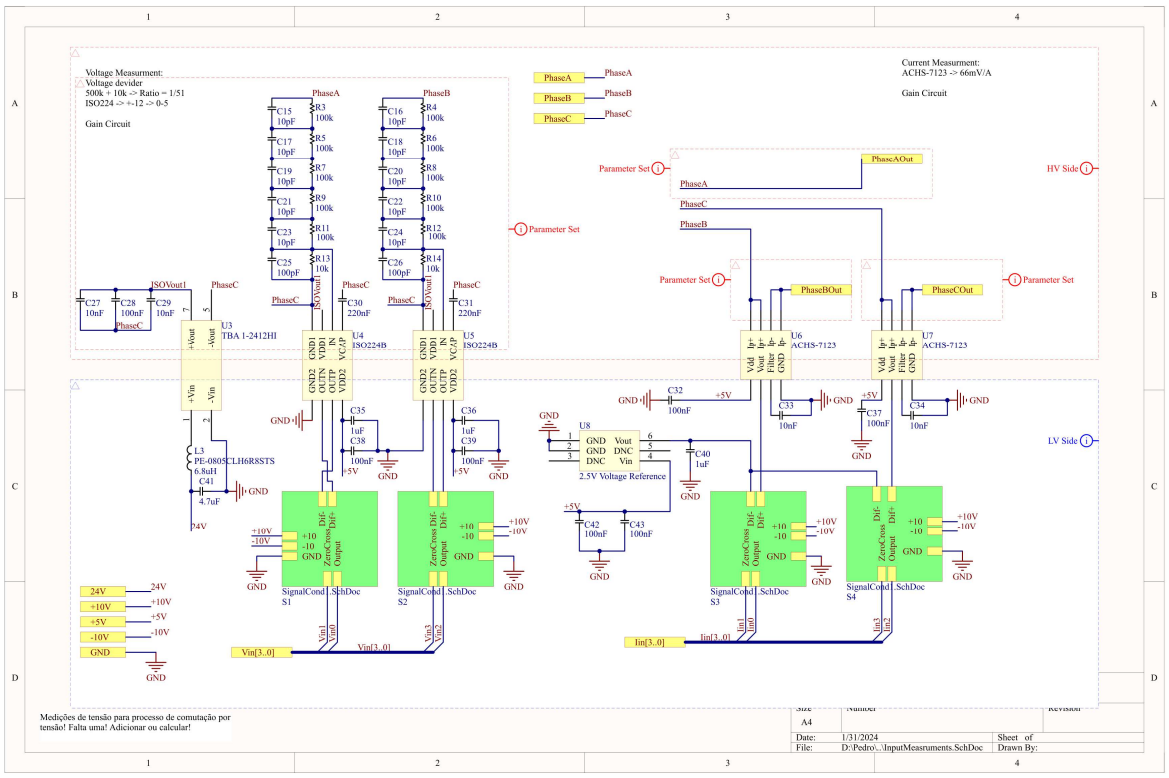

Figure C.15 Input Filter: Input voltage and current measurements.

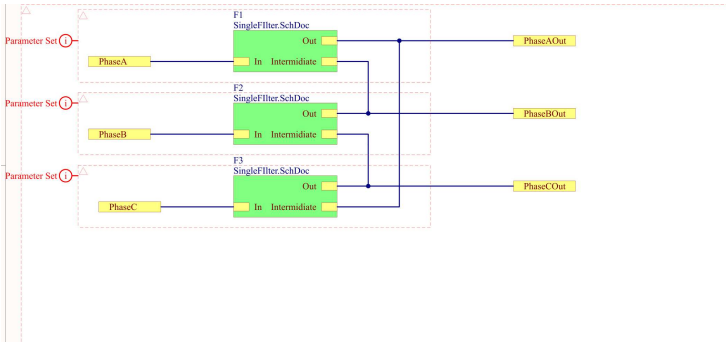

Figure C.16 Input Filter: Input filter connection schematic.

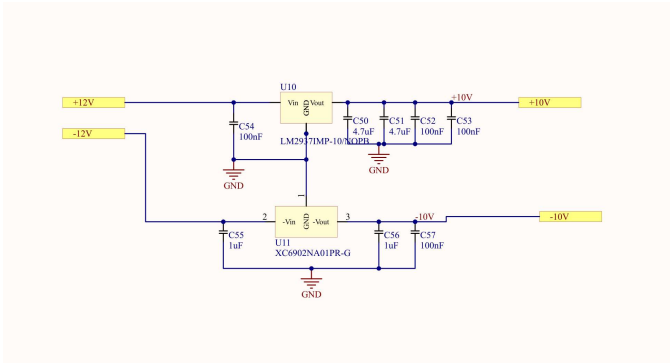

Figure C.17 Input Filter: Power conditioning schematic for the +10V/-10V generation.

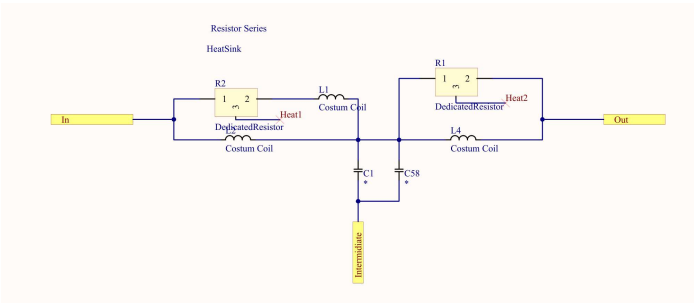

Figure C.18 Input Filter: Connections of the passive filter components.

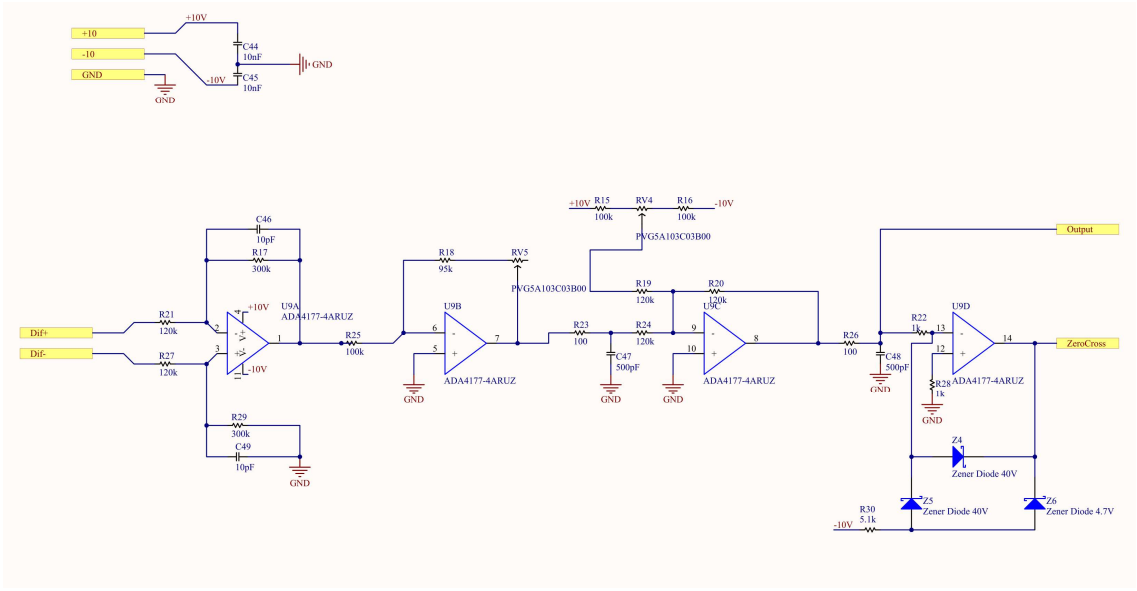

Figure C.19 Input Filter: Signal conditioning schematic..

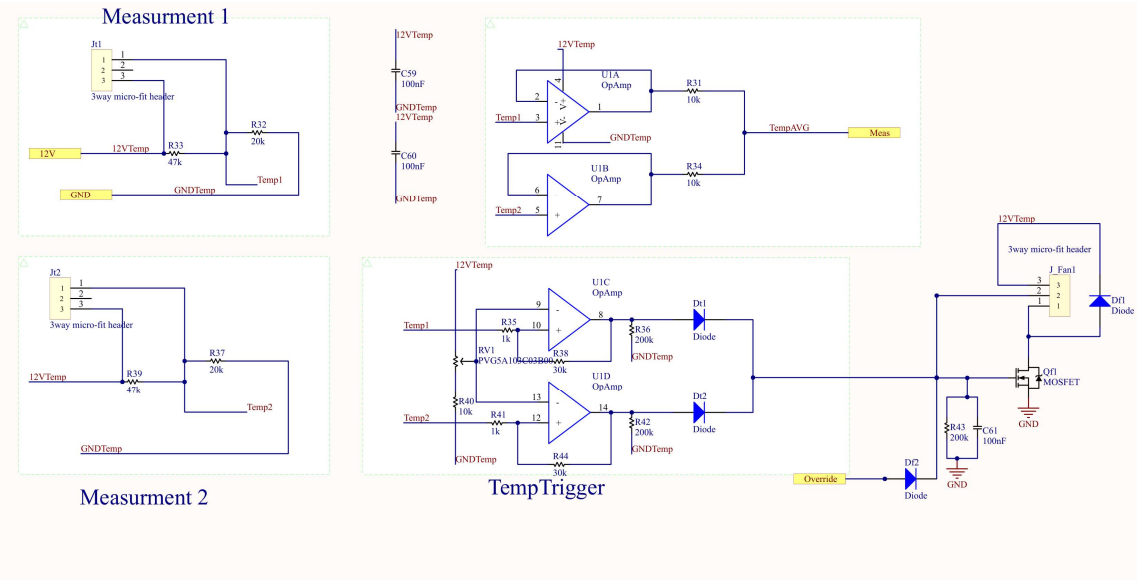

Figure C.20 Input Filter: Temperature measurement and fan triggers schematic.

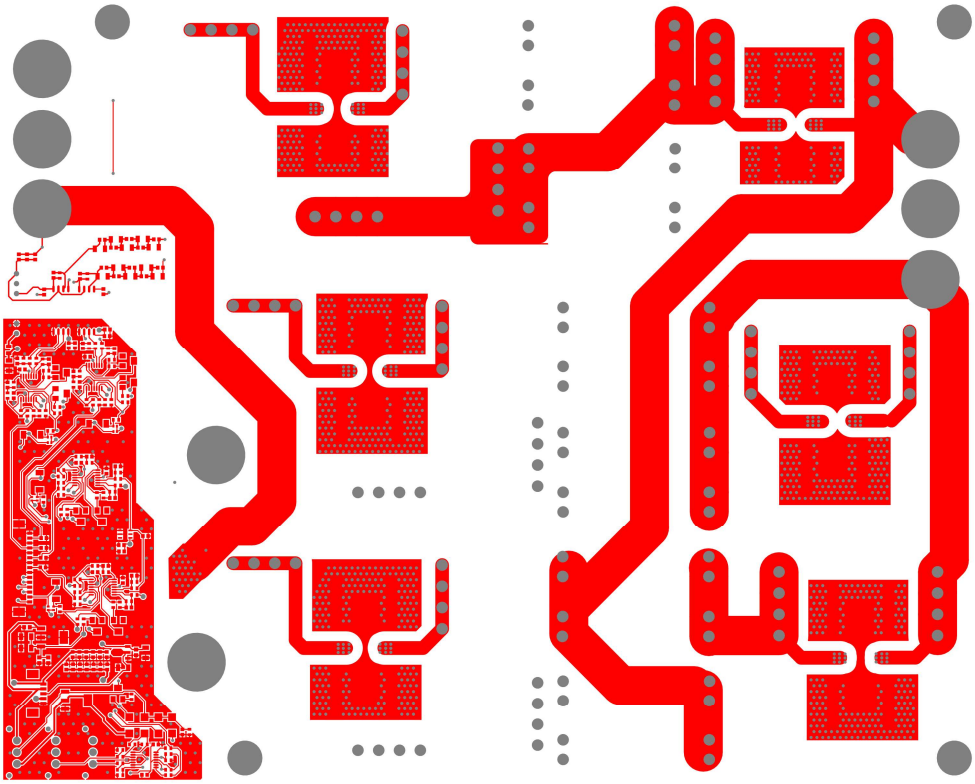

Figure C.21 Input Filter PCB: Top layer schematic.

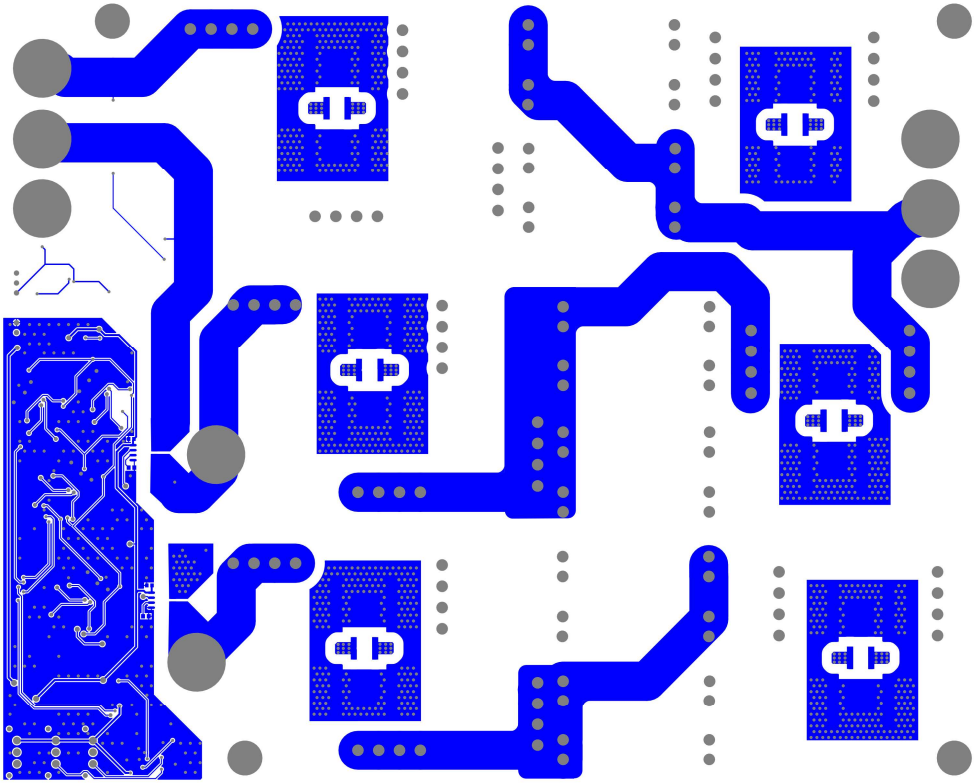

Figure C.22 Input Filter PCB: Bottom layer schematic.

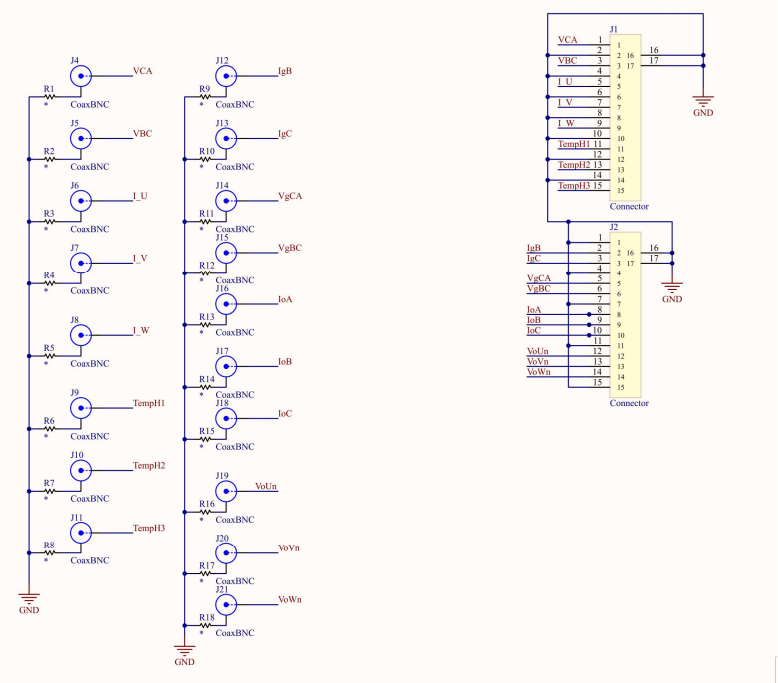

Figure C.23 Input/Output Interface 1: BNC connectors schematic.

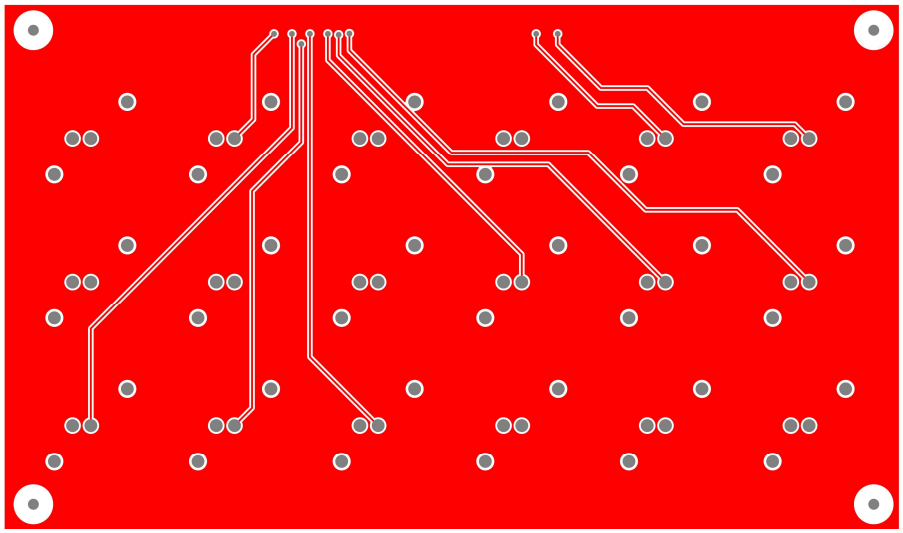

Figure C.24 Input/Output Interface 1 PCB: Top Layer.

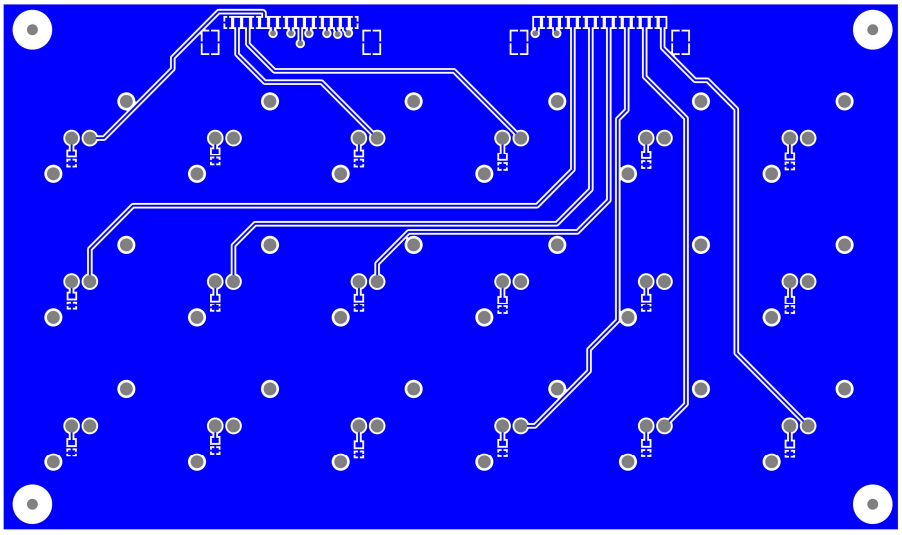

Figure C.25 Input/Output Interface 1 PCB: Bottom Layer.

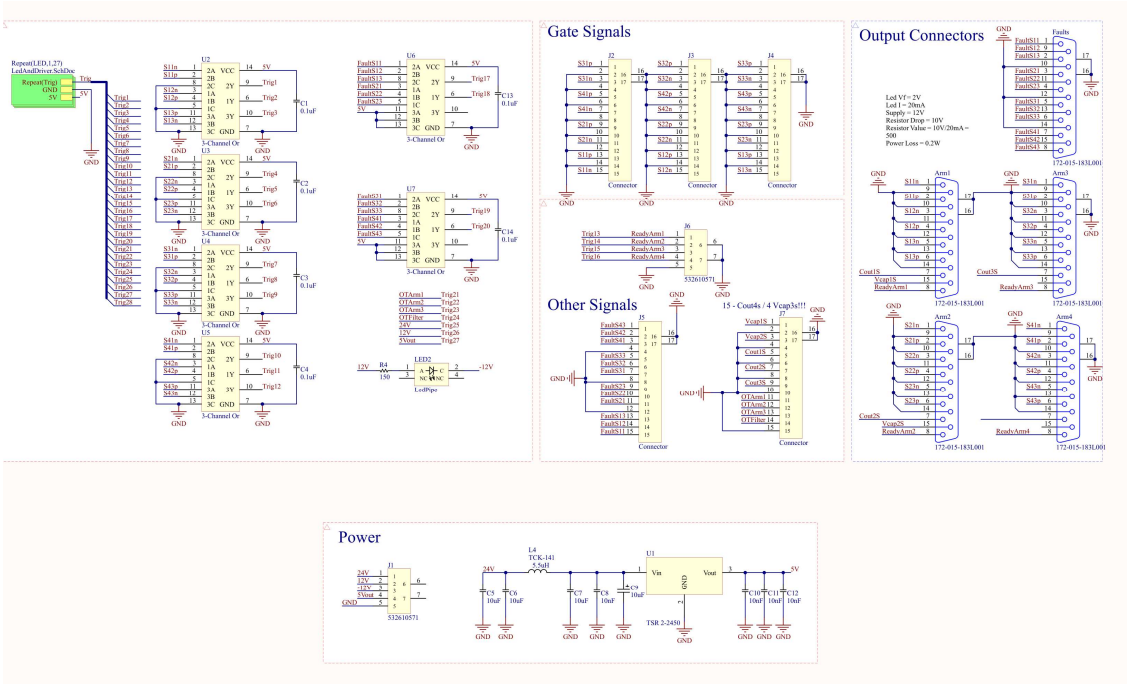

Figure C.26 Input/Output Interface 2: Top Schematic of interconnections and light indicators.

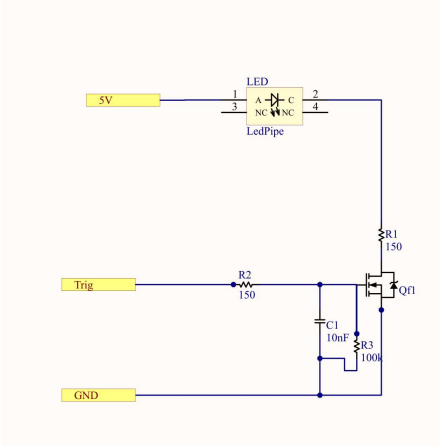

Figure C.27 Input/Output Interface 2: LED and driver c.

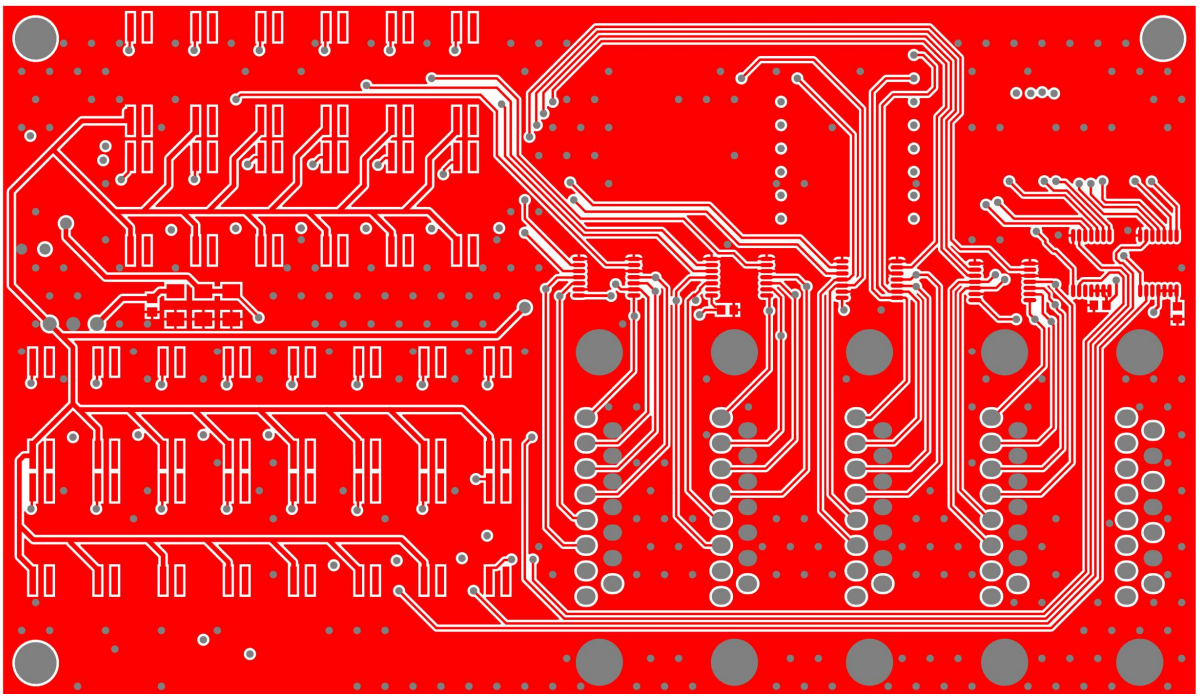

Figure C.28 Input/Output Interface 2 PCB: Top Layer Schematic.

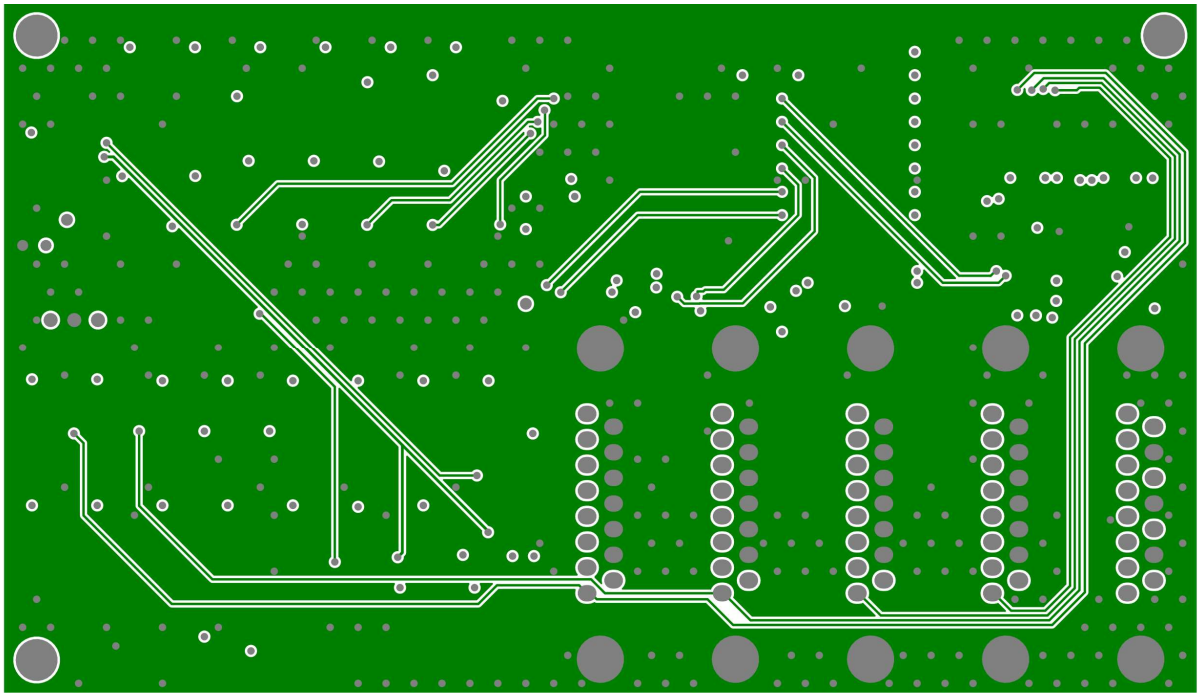

Figure C.29 Input/Output Interface 2 PCB: Intermediate Layer 1 schematic.

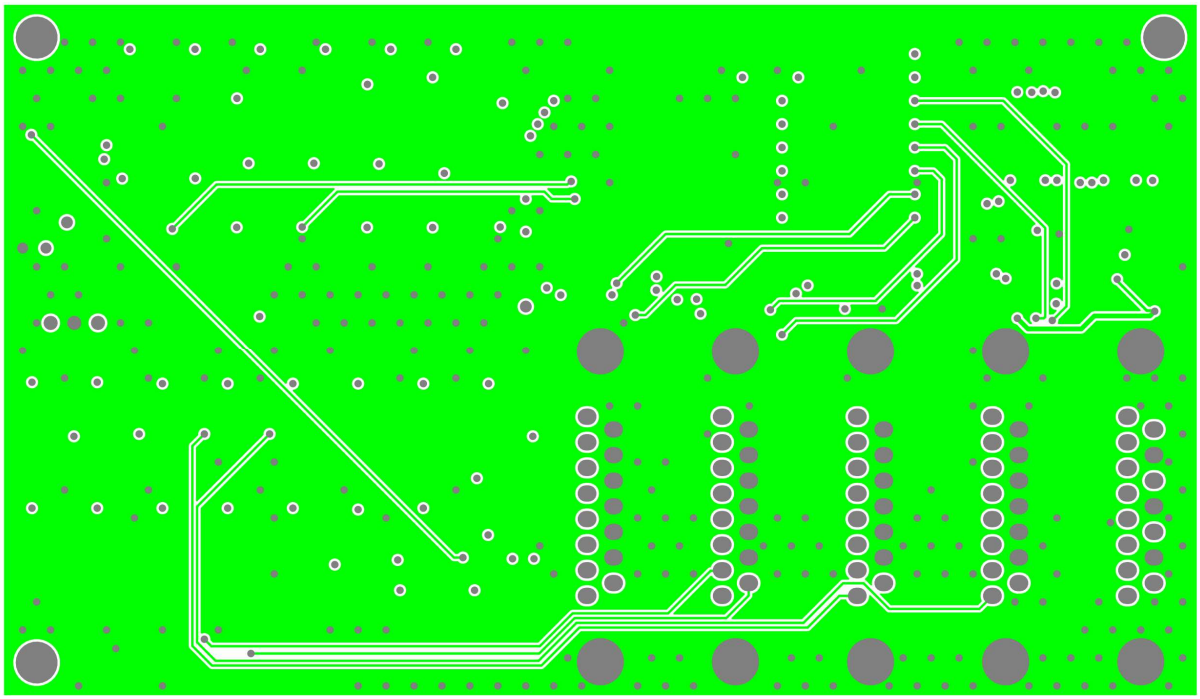

Figure C.30 Input/Output Interface 2 PCB: Intermediate Layer 2 schematic.

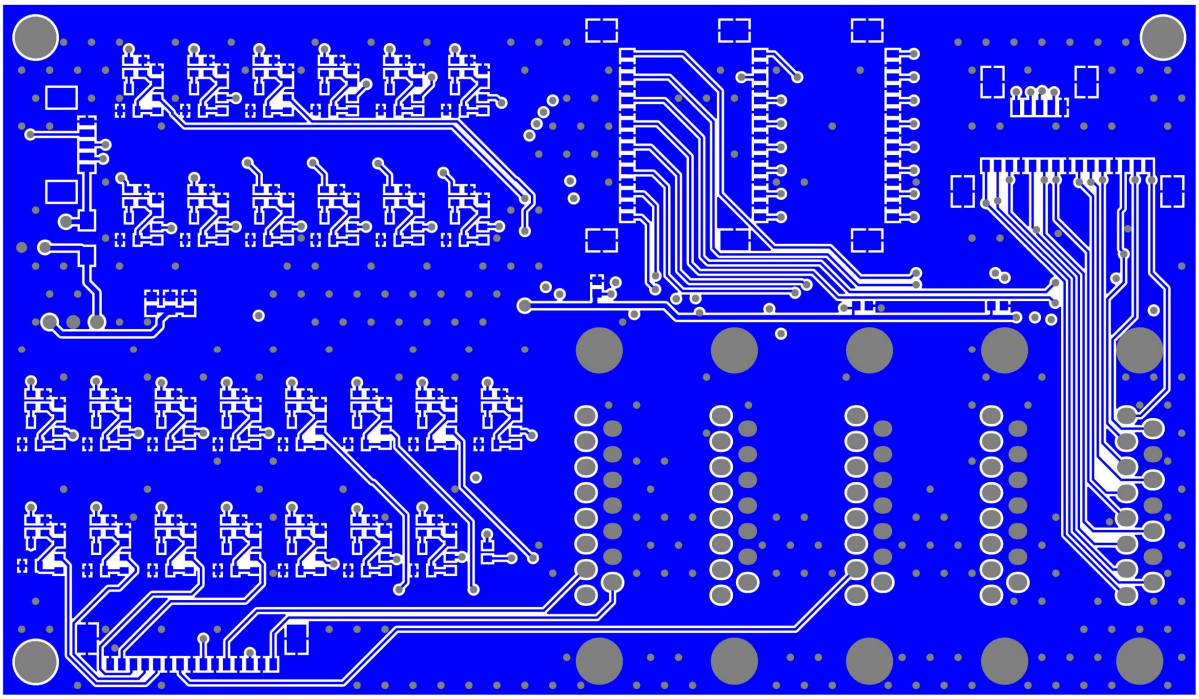

Figure C.31 Input/Output Interface 2 PCB: Bottom Layer schematic.

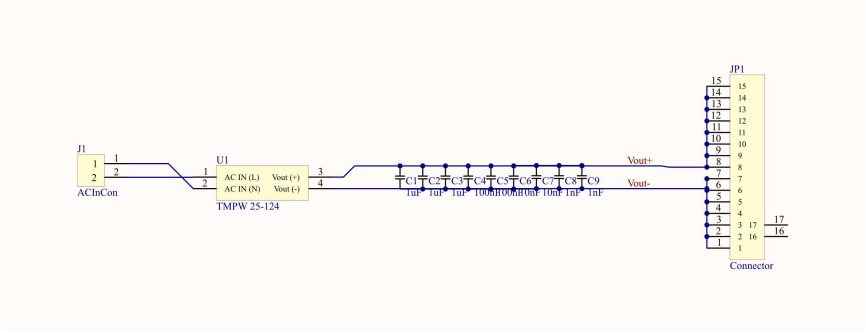

Figure C.32 AC/DC control and logic supply : Schematic.

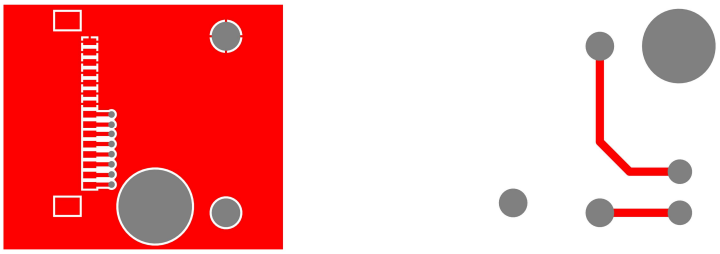

Figure C.33 AC/DC control and logic supply PCB : Top Layer schematic.

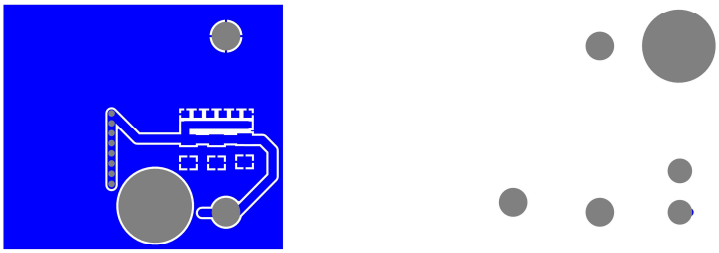

Figure C.34 AC/DC control and logic supply PCB : Bottom Layer schematic.

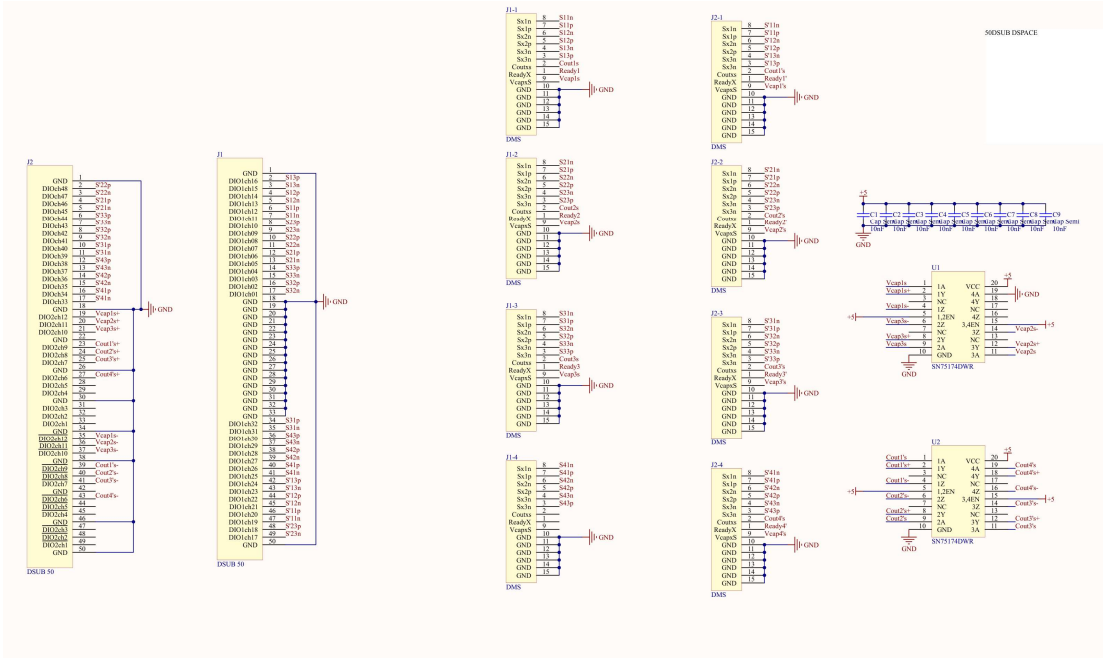

Figure C.35 DSpace Signal Interface Board : Interconnection schematic.

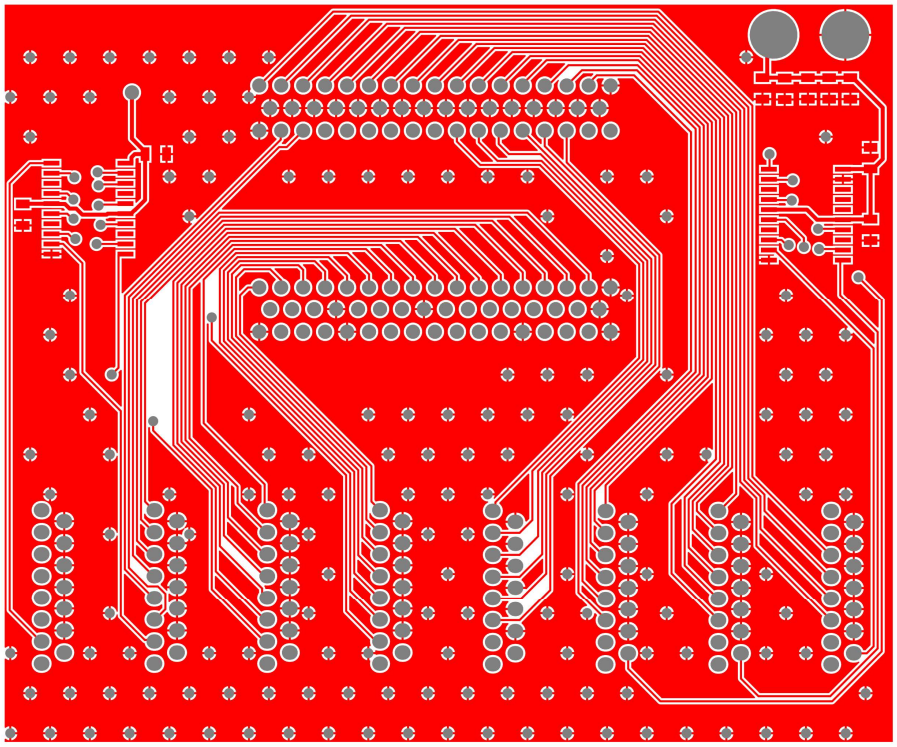

Figure C.36 DSpace Signal Interface Board PCB: Top Layer Schematic.

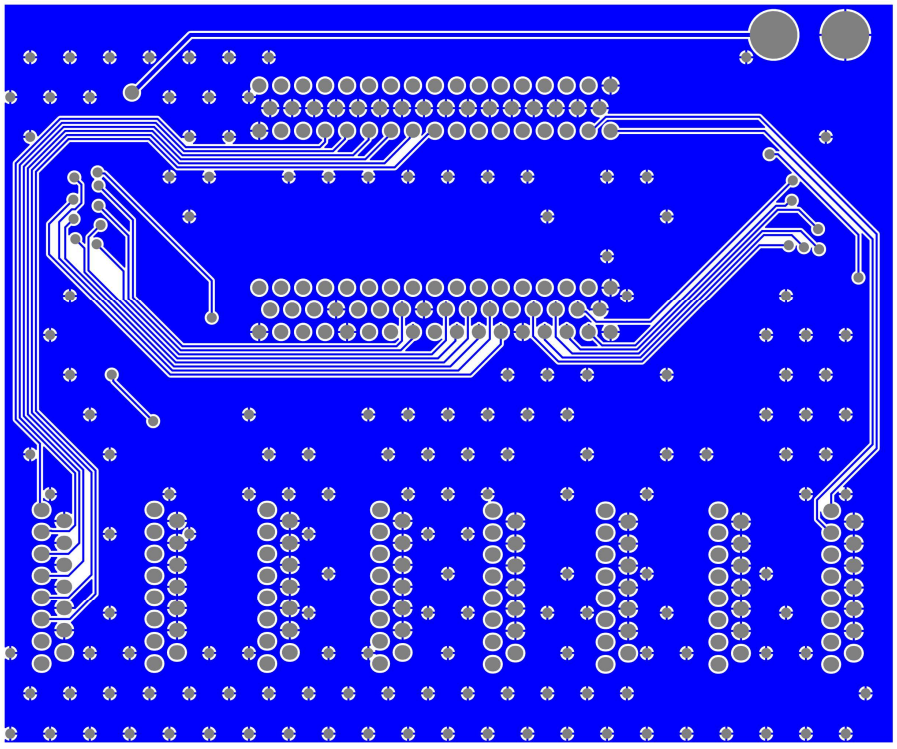

Figure C.37 DSpace Signal Interface Board PCB: Bottom Layer Schematic.

APPENDIX D

A COMMON SOURCE BIDIRECTIONAL GATE DRIVER WITH SOURCE SENSING PIN

The matrix converter was designed with common source bidirectional switches. This design requires more isolated DC/DC converters as opposed to common drain bidirectional switches. However, it is advantageous in terms of routing and power integrity since each DC/DC converter can be very close to each gate driver.

The selected SiC MOSFET semiconductors have what is known as a source sensing pin. Effectively, this acts as a second pin that is wire bounded to the gate and is not expected to carry the load currents. As such, it does not suffer from the voltage variations caused by the parasitic inductances and the di/dt of the source current.

The traditional gate drivers with common source would result in a diagram as depicted in Figure D.1, since the isolated DC/DC power supply is shared between both drivers the source sensing pin of both semiconductors would be connected. This means that part of the switch current would be conducted via this pin, ultimately damaging it.

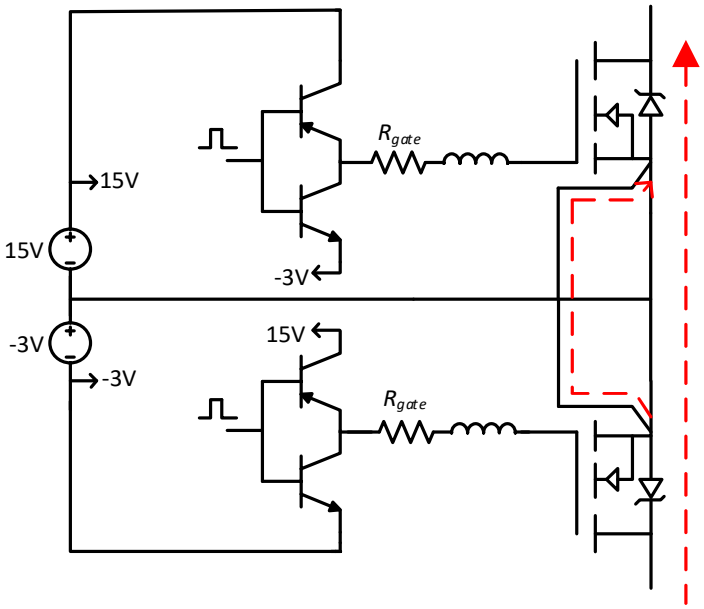

Figure D.1 Diagram of a bidirectional common source MOSFET switch with common source sensing pin.

As a solution, the gate driving resistors were placed in the source sensing path, between the source sensing pin and the source. As depicted in Figure D.2. In this configuration the impedance across the source sensing pin is significantly increased, LT Spice simulation showed that the circulating current in this pin was sufficiently low so as not do damage the semiconductor.

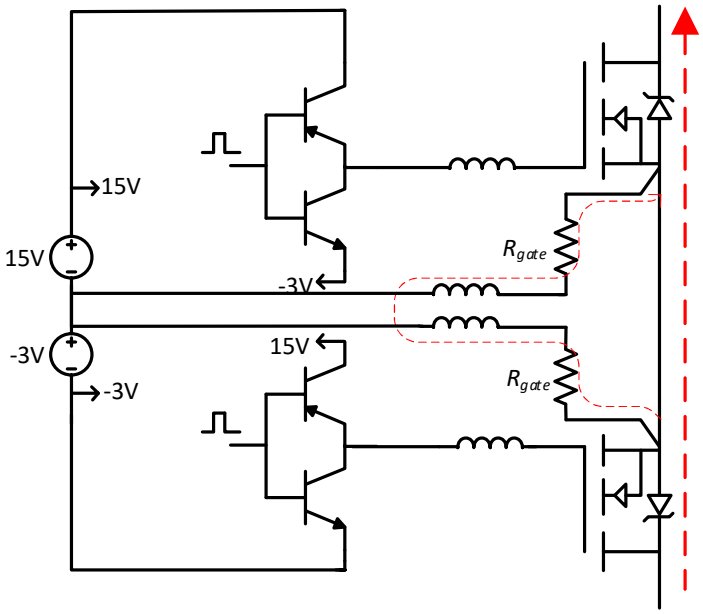

Figure D.2 Diagram of a bidirectional common source MOSFET switch with common source sensing pin.

APPENDIX E
LEAKAGE TOLERANT COMMUTATION STATE MACHINE

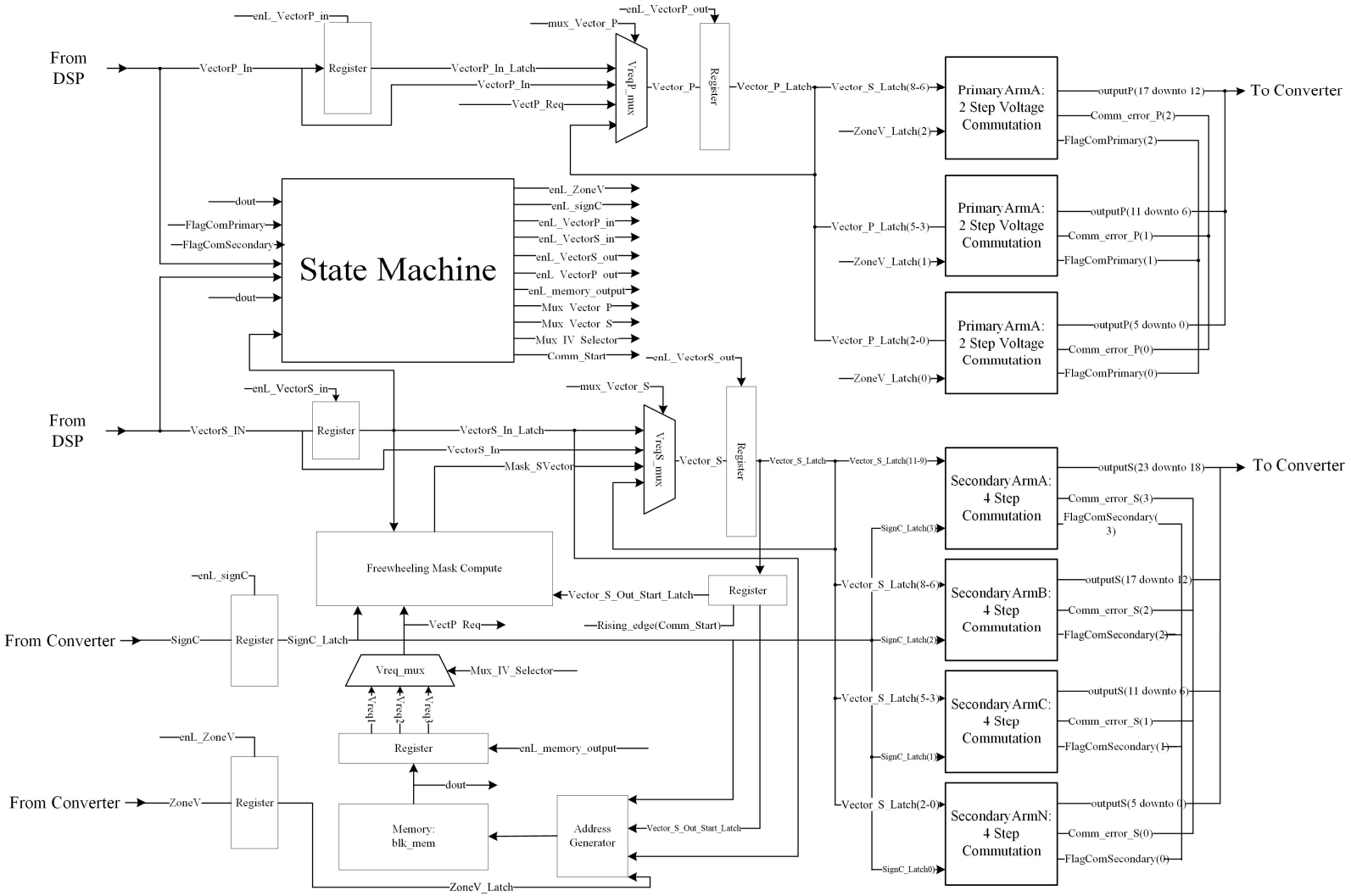

Figure E.1 Leakage tolerant commutation implementation schematic

APPENDIX F

PLANAR TRANSFORMER DESIGN

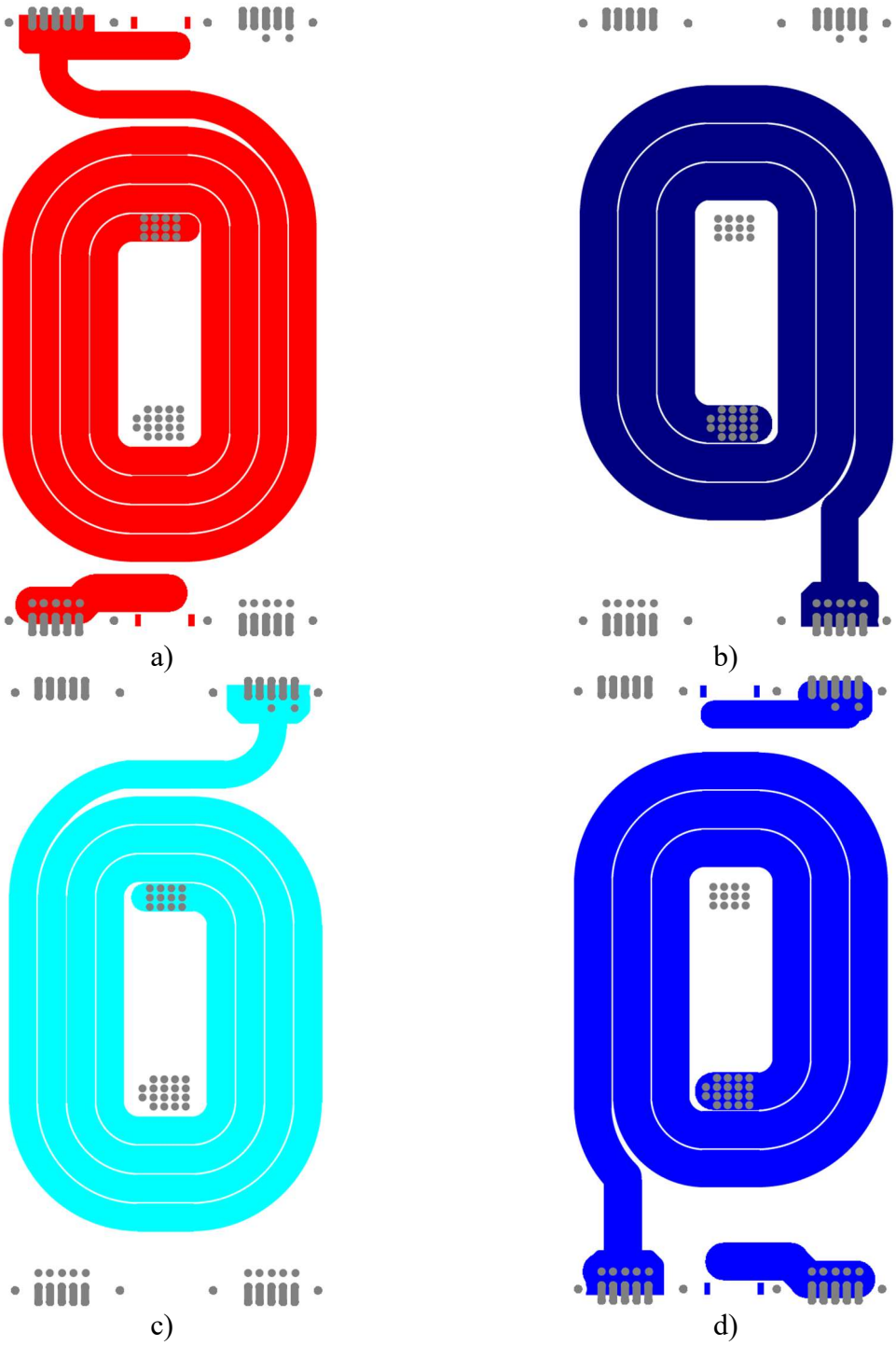

Figure F.1 Type 1 Planar Transformer PCB design: a) Top Layer; b) Inner Layer 1; c) Inner Layer 2; d) Bottom Layer.

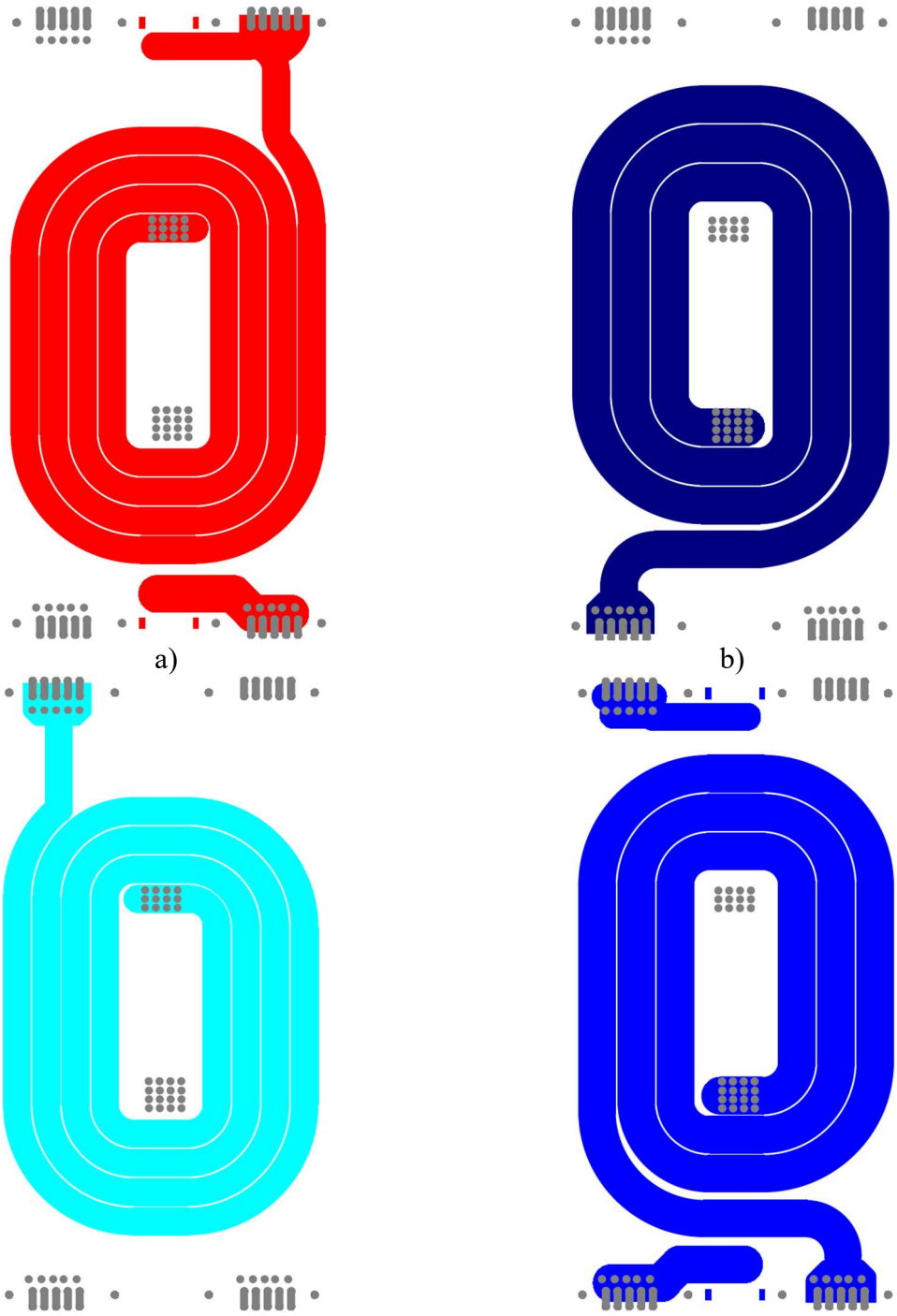

Figure F.2 Type 1 Planar Transformer PCB design: a) Top Layer; b) Inner Layer 1; c) Inner Layer 2; d) Bottom Layer.