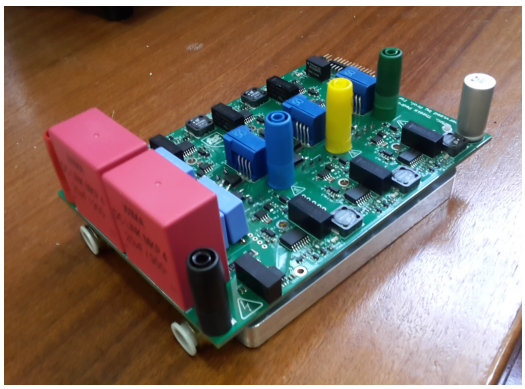
TÉCNICO LISBOA



# Compact Three-Phase SiC Inverter for the IST Formula Student Prototype

**Pedro Miguel Batista de Sousa Correia da Costa**

Thesis to obtain the Master of Science Degree in

## Electrical and Computer Engineering

Supervisor(s): Prof. José Fernando Alves da Silva

### Examination Committee

Chairperson: Prof. Rui Manuel Gameiro de Castro
Supervisor: Prof. José Fernando Alves da Silva
Member of the Committee: Prof. Hiren Canacsinh

**November 2018**

Dedicated to my family.

## Declaration

I declare that this document is an original work of my own authorship and that it fulfills all the requirements of the Code of Conduct and Good Practices of the Universidade de Lisboa

# Acknowledgments

First and foremost, I have to thank my supervisor Prof. José Silva for the continuous support, for the incredibly availability, for the thrust deposited in me to do the experimental tests and for all the counselling without whom it would not be possible to do this work,

Secondly I have to thank my family, in particular to my Mother and Father which ever since I joined Formula Student supported me in this adventure even at the cost of seeing their son considerably less.

I also would like to thank Sofia Nunes. Without her continuous support this work would have been so much more difficult. Thank you for cooking dinner late to me, just so that I could stay on the Laboratory a few more hours, thank you for opening me the door late at night when I had to stay working late hours, just to make sure I would woke up early the next day. Thank you for all the Love.

To the powertrain team: André Agostinho, Bruno Figueiredo, Bruno Fernandes, Miguel Machado, Miguel Sousa, Mariana Cunha, Filipa Neves it was a pleasure to work with you.

To João Sarrico whose work was an inspiration for this thesis, and whose friendship knows no bounds, thank you.

To my dear friend André Santos for all the help with the cooling plate design and manufacturing, thank you.

To all the FST 06e and FST 07e team members who I had the pleasure to work with.

A word of appreciation to the FST 08e team and in particular to Henrique Karas, the team leader of FST 08e and the soon to come FST 09e, for the continuous investment in research and development for the team.

To my fellow thesis writers who kept me company while writing their own thesis, Pedro Mateus and Miguel Duarte, always available to provide their insight on this work.

A special word of appreciation to Rui Miranda, Daniel Pinho, Manuel Ferreira, Bruno Santos and Miguel Figueiroa that mentored me in my early times in formula student.

A second word of appreciation to Daniel Pinho for all the hard desoldering work I put you trough, his help was invaluable for the conclusion of the prototype.

To Mr. Duarte Batista and Mr. João Paulo for all the help in the Laboratory, always available to help build my experiments.

# Resumo

Esta tese tem como objectivo o desenvolvimento de um protótipo de inversor trifásico, circuitos de comando e instrumentação, usando novas tecnologias de semicondutores disponíveis no mercado, para utilização num veículo elétrico de competição da equipa de Formula Student do IST. É igualmente desenvolvida a fundamentação teórica e são desenvolvidos procedimentos experimentas para a obtenção de estimações das perdas de semicondutores.

Retrata-se, numa fase inicial, o estado da arte do desenvolvimento dos semicondutores wide bandgap para utilização em conversores de potência, tendo sido escolhidos dois dispositivos promissores, MOSFET de Carbeto de Silício e HEMT de Nitreto de Gálio, de dois fabricantes líderes na produção destes dispositivos, sobre os quais se realizaram diversos testes experimentais. Foram selecionados os MOSFETs e Diodos de Schottky de Carbeto de Silício que, após avaliação, se consideram melhor adequar à utilização em inversores para motorização de veículos de corrida.

Pela via experimental foram caracterizadas as perdas de comutação e de condução em ambos os dispositivos escolhidos em montagens inversoras. Os resultados obtidos experimentalmente foram comparados com valores obtidos por simulação recorrendo a modelos SPICE disponibilizados pelos fabricantes. Adicionalmente os dados experimentais foram utilizados para a formulação de novos modelos que permitem determinar as perdas em regime dinâmico, indo assim, ao encontro das necessidades reais de operação do protótipo de Formula Student.

No decurso da tese, o funcionamento do protótipo do inversor foi testado usando uma carga indutiva e um motor trifásico, tendo o mesmo evidenciado resultados vantajosos tanto em eficiência como em densidade de potência.

**Palavras-chave:** Inversor, Wide Bandgap, SiC MOSFET, GaN HEMT, Formula Student

# Abstract

This thesis has as primary objective the development of a prototype for a three-phase inverter, driving circuits and instrumentation, using new semiconductor technologies available in the market, to be implemented in a competition electric vehicle of the IST Formula Student team. Furthermore, a theoretical basis and a set of experimental procedures was proposed in order to estimate the semiconductor losses in inverter operation.

In a preliminary analysis the state of the art on the development of wide bandgap semiconductors for use in power converters is depicted. Two promising devices, Silicon Carbide MOSFET and Gallium Nitride HEMT, were chosen from two leading manufacturers in the production of these devices, and for each several experimental tests were performed. At the light of the test results the MOSFETs and Silicon Carbide Schottky Diodes were selected as the most suited technology to be used in inverters for motorization of racing vehicles.

The switching and conduction losses for both chosen devices were characterized in an inverter configuration. The obtained experimental results were compared with values obtained by simulations using SPICE models available by the manufacturers. In addition, the experimental data was used to formulate new models that allow the determination of losses in dynamic conditions, thus meeting the real needs of the Formula Student prototype.

During the execution of the thesis the operation of the inverter prototype was tested using an inductive load and a three-phase motor, showing prominent results both in power density as in efficiency.



**Keywords:** Inverter, Wide Bandgap, SiC MOSFET, GaN HEMT, Formula Student

# Contents


Acknowledgments . . . . . vii
Resumo . . . . . ix
Abstract . . . . . xi
List of Tables . . . . . xvii
List of Figures . . . . . xix
Nomenclature . . . . . xxiii
Glossary . . . . . xxvii

**1 Introduction** **1**
1.1 Motivation . . . . . 1
1.2 Topic Overview . . . . . 2
1.2.1 Silicon Semiconductors . . . . . 3
1.2.2 Silicon Carbide Semiconductors . . . . . 3
1.2.3 Gallium Nitride Semiconductors . . . . . 4
1.2.4 Materials . . . . . 5
1.3 Objectives . . . . . 5
1.4 Thesis Outline . . . . . 6

**2 Theoretical Background and Loss Analysis** **7**
2.1 Formula Student Competition . . . . . 7
2.2 Three-Phase Voltage Inverter . . . . . 9
2.3 3-Phase Inverter Losses . . . . . 11
2.3.1 IGBT . . . . . 11
2.3.2 MOSFET . . . . . 12
2.3.3 HEMT . . . . . 13
2.4 System Definition . . . . . 14
2.5 Results . . . . . 16
2.6 Thermal Model . . . . . 17
2.6.1 Steady State Analysis . . . . . 18
2.6.2 Transient Analysis . . . . . 18

**3 Experimental Determination of Semiconductor Losses** **21**
3.1 Methodology . . . 21
3.2 Calibration . . . 26
3.2.1 GaN HEMT Calibration Results . . . 27
3.2.2 SiC Calibration Results . . . 29
3.3 Test Results . . . 30
3.3.1 GaN Test Results . . . 31
3.3.2 SiC Test Results . . . 34
3.4 Error analysis . . . 38
3.5 Verification and Validation . . . 39
3.6 Experimental Conclusions . . . 41
3.7 Dynamic Model for Loss Analysis . . . 41
3.7.1 Temperature Dependent Models . . . 42

**4 3 Phase Inverter Design and Manufacturing** **45**
4.1 Semiconductor Selection . . . 45
4.2 Gate Driver Design . . . 47
4.3 DC Link capacitance . . . 49
4.4 Voltage, Current and Temperature Sensing . . . 50
4.5 PCB Design . . . 52
4.6 Cooling Plate . . . 53
4.7 PCB Manufacturing . . . 56
4.8 Final Assembly . . . 57

**5 3 Phase Inverter Testing** **59**

**6 Conclusions** **67**
6.1 Achievements . . . 68
6.2 Future Work . . . 68

**Bibliography** **71**

**A Altium Schematics** **75**
A.1 Top Schematic . . . 75
A.2 Inverter Schematic . . . 76
A.3 Semiconductor Schematic . . . 77
A.4 Gate Driver Schematic . . . 78
A.5 Current Sensing Schematic . . . 79
A.6 Voltage Sensing Schematic . . . 80
A.7 Low Voltage Power Supply Schematic . . . 81
A.8 Input/Output Schematic . . . 82

**B Printed Circuits Boards Drawings** **83**

B.1 Altium PCB Layers . . . . . 83

B.2 Top Layer . . . . . 83

B.3 Bottom Layer . . . . . 84

B.4 Inner Layer 1 . . . . . 85

B.5 Inner Layer 2 . . . . . 86

B.6 Inner Layer 3 . . . . . 87

B.7 Inner Layer 4 . . . . . 88

**C Technical Datasheets** **89**

C.1 Technical Drawings . . . . . 89

C.2 Cooling Plate . . . . . 89

# List of Tables


1.1 Si, SiC and GaN material properties . . . . . 5

2.1 FST 07e General Powertrain Parameters . . . . . 14
2.2 Total losses per semiconductor in cases A, B and C . . . . . 17

3.1 Parameters of the GaN and SiC transistors used in the evaluation boards . . . . . 25
3.2 Example of calibration data acquired during a SiC MOSFET evaluation board calibration . 27
3.3 Example of acquired data for GaN HEMT evaluation board experiment . . . . . 34
3.4 Example of data acquired during SiC MOSFET evaluation board experiments . . . . . 36

4.1 Parameters of the most relevant SiC MOSFET discrete devices . . . . . 46
4.2 Parameters of the most relevant SiC Schottky Diodes discrete devices . . . . . 46
4.3 Parameters of the most relevant SiC 3 Phase Legs power modules . . . . . 47
4.4 Parameters for cooling plate thermal conductive calculation . . . . . 53
4.5 Comparison of power density's of different inverter solutions . . . . . 58

5.1 Example of acquired data for a set of efficiency measurements . . . . . 63
5.3 Weighted Total harmonic distortion for the first 50 harmonics . . . . . 65

# List of Figures


1.1 FST 06e Team in Formula Student Italy Competition . . . . . 2
1.2 Commercial Inverters used by the team . . . . . 2

2.1 Formula Student Dynamic Events, Courtesy of Formula Student UK . . . . . 8
2.2 Simulation of vehicle output power over a track . . . . . 9
2.3 IGBT 3 Phase 2 Level Inverter . . . . . 10
2.4 GaN HEMT Double Inverter configuration for open-winding motor . . . . . 13
2.5 Examples of SiC Packagings . . . . . 17
2.6 Thermal model of semiconductor layers using Cauer Model . . . . . 19
2.7 Thermal model of semiconductor layers using Foster Model . . . . . 20

3.1 Double Pulse Test Setup . . . . . 22
3.2 Double Pulse Test Setup . . . . . 22
3.3 GaN Evaluation Board with detail on Shunt Resistor . . . . . 23
3.4 Evaluation Boards Simplified Schematics . . . . . 24
3.5 Half Bridge Inverter topology with capacitive middle point . . . . . 25
3.6 Examples of temperature measurements with a thermal camera . . . . . 25
3.7 Example of temperature measurement with thermocouples . . . . . 26
3.8 Calibration Test Setup for the SiC devices . . . . . 27
3.9 GaN HEMT Channel Resistance variation with temperature . . . . . 28
3.10 GaN HEMT Evaluation Board temperature to dissipated power . . . . . 28
3.11 SiC MOSFET Channel Resistance variation with temperature . . . . . 29
3.12 SiC MOSFET Channel Resistance variation with temperature . . . . . 30
3.13 Total, conduction and switching dissipated powers . . . . . 32
3.14 Typical $Ciss$, $Coss$ and $C_{rss}$ vs $V_{ds}$, courtesy of GaN Systems . . . . . 33
3.15 Switching Energy vs Current . . . . . 33
3.16 Half Bridge Inverter topology with on laboratory built power supply . . . . . 35
3.17 Experimental setup with on laboratory built power supply . . . . . 35
3.18 Turn on and turn off under 600 V DC link Voltage . . . . . 36
3.19 Total, conduction and switching dissipated powers . . . . . 37
3.20 Switching Energies against output current for SiC MOSFET . . . . . 37

3.21 Spice schematic representing the GaN Evaluation Board . . . 39
3.22 Simulated vs Experimental GaN HEMT Switching Losses Measurement . . . 40
3.23 Simulated vs Experimental SiC MOSFET Switching Losses Measurement . . . 40
3.24 Simulink model for the GaN HEMT . . . 42
3.25 Simulink subsystem for $E_{on}$ calculation . . . 43
3.26 Simulink subsystem for $E_{off}$ calculation . . . 43
3.27 Simulink subsystem for $R_{DS_{on}}$ calculation . . . 44
3.28 Simulink subsystem for diode forward voltage, $V_f$, calculation . . . 44

4.1 Short Circuit protection circuit . . . 48
4.2 Current Sensor schematic, Courtesy of LEM[49] . . . 50
4.3 Voltage Sensing Schematic . . . 51
4.4 Voltage and current sensing in the PCB . . . 51
4.5 Temperature sensing placement on the cooling plate . . . 52
4.6 Altium Designer renders of PCB design files . . . 52
4.7 Cooling plate finite element analysis simulations . . . 55
4.8 Computer drawing renders and actual manufactured cooling plate . . . 55
4.9 PCB manufacturing process . . . 56
4.10 Transistors and capacitors on the bottom side of the PCB . . . 56
4.11 Assembly process of the cooling plate . . . 57
4.12 Complete Inverter Assembly . . . 57

5.1 Modulator output waveforms . . . 60
5.2 Inverter testing against a RL Load . . . 60
5.3 First Test Setup with the inverter controlling an induction motor . . . 61
5.4 Second Test Setup . . . 61
5.5 Cooling circuit and power measurement setup . . . 62
5.6 Test setup for efficiency measurement . . . 62
5.7 Measured efficiency at 150,300 and 600 V . . . 63
5.8 Waveform of phase to phase voltages and output current on one of the phases . . . 64
5.9 Waveforms of output currents at 300 V DC link voltage . . . 64

A.1 Top Schematic . . . 75
A.2 Inverter Shematic . . . 76
A.3 Semiconductors Shematic . . . 77
A.4 Gate Driver Shematic . . . 78
A.5 Current Sensing Shematic . . . 79
A.6 Voltage Sensing Shematic . . . 80
A.7 Low Voltage Power Supply Shematic . . . 81
A.8 Input/Output Shematic . . . 82

B.1 Top Layer . . . . . 83
B.2 Bottom Layer . . . . . 84
B.3 Inner Layer 1 . . . . . 85
B.4 Inner Layer 2 . . . . . 86
B.5 Inner Layer 3 . . . . . 87
B.6 Inner Layer 4 . . . . . 88

C.1 Cooling Plate . . . . . 89

.

# Nomenclature

### Greek symbols

| | |
|---|---|
| $\alpha$ | Thermal Diffusion. |
| $\eta$ | Dynamic Viscosity. |
| $\Gamma$ | Fundamental Frequency. |
| $\omega$ | Angular Frequency. |
| $\rho$ | Density. |
| $\upsilon$ | Kinematic Viscosity. |
| $\varphi$ | Phase Angle. |

### Roman symbols

| | |
|---|---|
| $\Delta i_0$ | Ripple Current. |
| $C_{iss}$ | Input capacitance. |
| $C_{oss}$ | Output capacitance. |
| $C_{rss}$ | Reverse transfer capacitance. |
| $E_{off}$ | Turn-off energy. |
| $E_{on}$ | Turn-on energy. |
| $f$ | Frequency. |
| $h$ | Thermal Convection Coefficient. |
| $I_o$ | Phase current amplitude. |
| $I_{avg}$ | Average Current. |
| $I_{DC}$ | Average Current of the DC link. |
| $I_{S_{max}}$ | Maximum current across transistor $S$. |
| $I_{S_{rms}}$ | Root Mean Square current across transistor $S$. |

$I_{S_{tail}}$ Tail current.

$k$ Thermal Conduction Coefficient.

$k_e$ Motor Voltage Constant.

$k_t$ Motor Torque Constant.

$m$ Modulation factor.

$P_C$ Conduction power losses.

$P_S$ Switching power losses.

$P_{Coss}$ Output capacitance power losses.

$P_{off}$ Turn off power losses.

$P_{on}$ Turn on power losses.

$Q$ Volumentric Flow Rate.

$R_d$ Diode forward resistance.

$R_g$ Gate Resistance.

$R_{DS_{on}}$ Drain to Source on resistance.

$R_{on}$ On resistance of a transistor.

$t_{OFF}$ Turn Off time.

$t_{ON}$ Turn On time.

$t_{rr}$ Reverse recovery time.

$t_{tail}$ Duration of tail currents flow.

$V_{cc}$ Input Voltage.

$V_{CE}$ Collector-Emitter voltage.

$V_D$ Diode threshold voltage.

**Subscripts**

$a, b, c$ Phase a,b and c.

# Glossary

| | |
|---|---|
| **2DEG** | Two Dimensional Electron Gas |
| **DC** | Direct Current |
| **ESL** | Equivalent Series Inductance |
| **ESR** | Equivalent Series Resistance |
| **EV** | Electric Vehicle |
| **FRD** | Fast Response Diode |
| **FSAE** | Formula Society of Automotive Engineers |
| **FST Lisboa** | Formula Student team from University of Lisbon |
| **GaN** | Gallium Nitrate |
| **HEMT** | High Electron Mobility Transistor |
| **IC** | Integrated Circuit |
| **IGBT** | Insulated Gate Bipolar Transistor |
| **MOSFET** | Metal Oxide Semiconductor Field Effect Transistor |
| **OEM** | Original Equipment Manufacturer |
| **PCB** | Printed Circuit Board |
| **PWM** | Pulse Width Modulation |
| **RMS** | Root Mean Square |
| **SBD** | Schottky Barrier Diode |
| **SiC** | Silicon Carbide |
| **Si** | Silicon |

# Chapter 1

# Introduction

## 1.1 Motivation

Alternative vehicle powertrain solutions for typical internal combustion engines are gaining more and more attention from costumers, automakers and governments, propelled by fuel economy and stricter emissions regulations [1].

State of the art alternatives such as Hybrid Electric Vehicle (EV), Battery EV or Fuel Cell EV make use of electric motors, where the first two topologies already have a respectable and growing market share of consumer vehicles[1, 2].

An important part of such powertrain is the Electric Motor Drives, or Inverters. Since stored energy comes in the form of a DC voltage, an Inverter must be used in order to generate the required waveforms that allow for the control of the motors torque and speed.

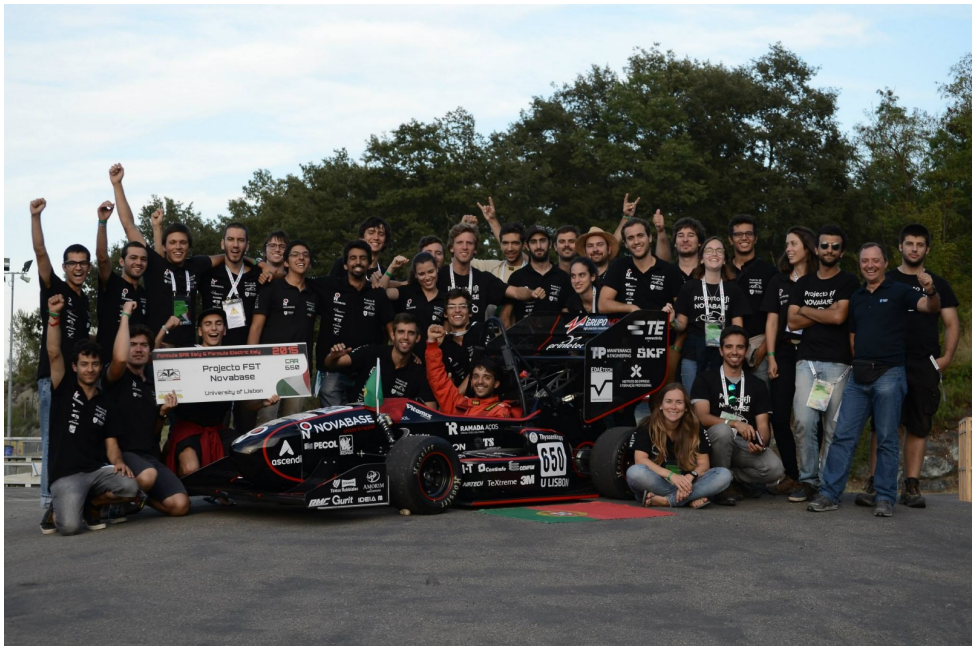
In the Formula Student competition, students are challenged to design, build and test a race car according to a specific set of rules stated by Formula Society of Automotive Engineers (FSAE). The Formula Student Team of Técnico Lisboa (FST Lisboa) has been developing cars for this competition since 2001. More recently, since 2011, the team is dedicating their efforts into building Formula Student Cars with an Electric Powertrain. FST 04e was the first one and since then, 4 more (FST 05e, FST 06e, FST 07e and FST 08e) were built, tested and taken to competitions across Europe, Figure 1.1 show the team at the italian competition in 2015.

With each developed car the team grows (in size and in knowledge). It is important to understand that such competition is an Engineering competition and the motivation behind it is to provide practical knowledge to future engineers. For this reason the team is trying to develop and build almost every part of the vehicle. As an example, there is the high voltage lithium polymer battery that has been self developed since FST 04e and improvements have been done throughout the years. Still the rest of the powertrain (Motor and Inverter) have been commercial solutions. Nevertheless efforts have been done, starting with the FST 07e team in R&D for Motors and Inverters. Motors, in particularly, saw their first version in 2017 through a Master Thesis of João Sarrico[3].

To sum up motivations, Power Electronics for Electric Vehicles is an exciting and growing field with

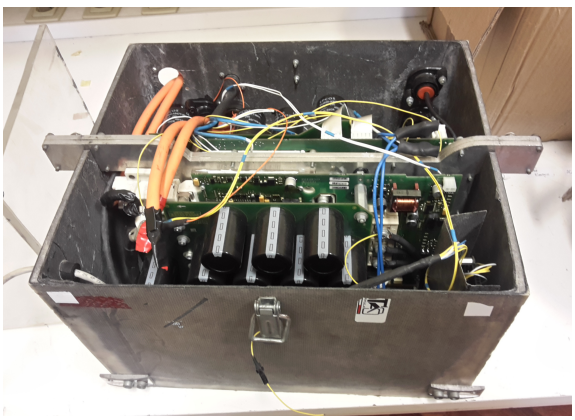
new technologies such as wide bandgap semiconductors, that will change the mobility in the coming years. Increasing this knowledge and investigation inside the FST Lisboa team will allow to better fulfill the true objectives of Formula Student, Learning.

Figure 1.1: FST 06e Team in Formula Student Italy Competition

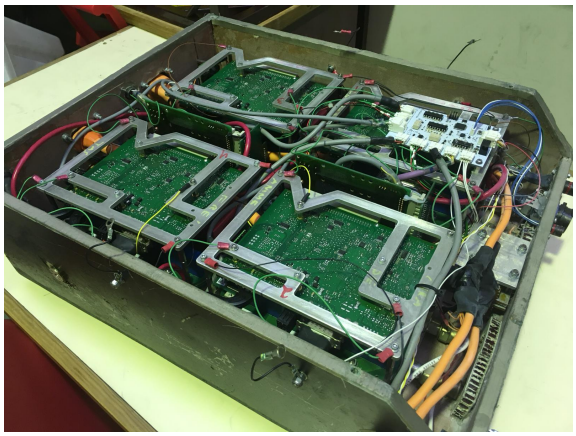



## 1.2 Topic Overview

Formula Student Electric Vehicles are typically powered by a Lithium Polymer Battery limited to a maximum voltage of 600 V by regulations. The last 4 prototypes of the team all used a 2 level inverter topology with Insulated Gate Bipolar Transistors (IGBTs) and freewheeling Silicon Diodes. In the first two, a commercial solution from Siemens[4] was used and in the last two a commercial solution from AMK[5]. Pictures of this inverters can be found in Figure 1.2.



(a) FST05e / FST06e



(b) FST07e / FST08e

Figure 1.2: Commercial Inverters used by the team

Having developed their own battery pack, as well as motors, the only part left to provide a fully in house developed powertrain system is the inverters pack. Though most of teams are now developing their own batteries and even some of them develop their motors, only few teams by this date develop their own set of inverters. For a racing electric prototype the development of a tailored inverter may come with a great set of advantages, namely more integration with new solutions, as for example super capacitors, a light weight and high efficient design, as well as the ability to adapt to future cars.

A special remark must be given to the efficiency where using transistors manufactured with wide bandgap material can bring significant advantages when compared to current commercial inverters which for this range of input voltages mostly are using Silicon IGBTs.

Even though silicon semiconductors have dominated the power electronics industry for quite some time, new insurgent technologies are showing incredible advantages. A review on the silicon semiconductors technology and attractive alternatives follows.

### 1.2.1 Silicon Semiconductors

Typical silicon Metal Oxide Semiconductor Field Effect Transistors, MOSFETs, do not suite well in voltages above 600 V conditions due to their critical breakdown field. To actually make a MOSFET device suited for blocking voltages of 900 V and beyond, the thickness of the device mus be substantially increased. As a consequence an increase of the on-state resistance, as well as an increase in parasitic capacitance that increases the switching losses when compared to devices with lower voltage ratings. For reference, at high breakdown voltages, the on state resistance, $R_{DS_{on}}$, increases approximately with the square of the drain-source breakdown voltage [6].

Therefore Silicon IGBTs are used in almost every high voltage power converter. They combine the simple gate driving characteristics of the Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) with the high current capabilities of bipolar transistors.

The IGBT has some particularities/drawbacks:

- To reduce $R_{on}$ minority carriers are injected into the drift region, which generates tail currents when turning off, increasing switching losses;
- The additional PN junction (comparing to MOSFETs) blocks reverse flow. This makes the need for the freewheeling diode;
- More switching losses means lower switching frequency than MOSFETs.

Even so, given the high breakdown voltages and the capacity to handle very high currents, the Si-IGBT is the most used semiconductor in power systems (with the exception of diodes).

### 1.2.2 Silicon Carbide Semiconductors

Silicon Carbide, SiC, is a compound semiconductor composed of silicon and carbon. Silicon Carbide semiconductors are an attractive solution to replace typical Silicon semiconductors since they providesabout ten times the dielectric breakdown field strength and three times the thermal conductivity.

These properties make SiC an attractive material from which to manufacture power MOSFET's in the range of 600 to 1200 V (where silicon IGBTs previously were the most dominant solution).

**MOSFETs**

Main advantages of SiC-MOSFETs

- MOSFET devices have almost no tail currents;
- MOSFET by itself provides less switching losses, which can enable the use of higher frequencies;
- Less gate charge and capacitance due to smaller size packaging;
- Lower on resistance at high temperatures;
- Higher noise immunity, since the gate works at a high voltage range (-5 V to 20 V);
- 90% less losses during turn off due to no tail currents;
- Higher switching frequency implies a downsizing of passive components;
- SiC MOSFETs' body diodes have extremely fast recovery characteristics.

**Schottky Barrier Diodes**

Main advantages of SiC-SBDs compared to Fast Recovery Diodes (FRDs):

- Lower recovery time;
- Positive temperature coefficients;
- Less temperature dependency;
- Lower switching losses;
- Considerable less dependency of forward current (less ringing).

SiC-SBDs perform better in almost every way when compared even with ultra fast recovery diodes. Low temperature dependency is certainly one of the most prominent advantages. For reference a FRD $t_{rr}$ can double with only a 40 °C increase in temperature.

SiC-SBDs have already penetrated the industrial power electronics market and are commonly used as a freewheeling diode for the IGBTs, reducing system losses when compared to FRD.

### 1.2.3 Gallium Nitride Semiconductors

Very much like SiC, GaN provides a high critical field when compared to Si. The major advantage on GaN over SiC is the higher electron mobility that will result in higher performance for higher frequencies. Still GaN provides a lower thermal conductivity which theoretically places SiC devices in front for high power density designs.

While most semiconductor topologies are structured vertically, the power GaN Transistors that are available on market today are High Electron Mobility Transistors (HEMT), which relies on a horizontal structure. Horizontal structures tend to be limited in their operating voltage capabilities because large electric fields must be sustained across the surface of the device [7, 8].

HEMTs take advantage of 2 Dimensional Electron Gas (2DEG) which is created at the AlGaN/GaN heterojunction. The 2DEG is confined at the heterojunction and free to move parallel to the channel, resulting in a higher electron mobility.

Up to this point, commercially available GaN HEMTs can only block up to 650 V. Such blocking voltages are at most suited for a biased operation voltage up to 400 V. Therefore to use this device in a 600 V power converter multi level topologies must be considered. Still research and development is currently pushing for 1200 V GaN technologies[9].

### 1.2.4 Materials

The technological differences are obviously highly related to the intrinsic differences between the semiconductor materials. Table 1.1 places side by side some of the main properties of these materials[10].

The name wide bandgap semiconductor materials is given to semiconductor materials that have a relatively large bandgap when compared to typical semiconductors like silicon.

Most of these materials show significantly better electrical properties when compared to silicon. The higher the bandgap of the material the higher the breakdown voltage and the ability to operate at higher ambient temperatures.

Table 1.1: Si, SiC and GaN material properties

| **Materials Properties** | **Si** | **4H-SiCi** | **GaN** |
|---|---|---|---|
| Bandgap ($eV$) | 1.12 | 3.26 | 3.39 |
| Critical Field ($MV/cm$) | 0.23 | 2.2 | 3.3 |
| Electron Mobility ($cm^2/Vs$) | 1400 | 950 | 1700 |
| Electron Saturation Velocity ($10^6 cm/s$) | 10 | 22 | 25 |
| Thermal Conductivity ($W/cmK$) | 1.5 | 3.8 | 1.3 |

An important note to make is related with the differences in respect to thermal conductivity where SiC takes the lead.

## 1.3 Objectives

Keeping in mind the overview presented above, the following objectives are defined:

- Estimate current system efficiencies;
- Use models and experiments to evaluate efficiencies for SiC MOSFET and GaN HEMT systems;
- Compare both SiC MOSFET and Gan HEMT solutions;

- Design the electronic sub systems for supply and command of the semiconductors;
- Design a PCB with reduced parasitic effects;
- Design the cooling components of the inverter;
- Build and Test the inverter;
- Provide knowledge and documentation for future development of this solution.

Such objectives were defined with the main goal of empowering the FST team with knowledge and an Inverter prototype so that it could be further improved in the near future.

## 1.4 Thesis Outline

In chapter 2 a background on the Formula Student competition, the general operation of a 3 Phase Inverter and simple thermal models for semiconductors are presented. The current system efficiency is also calculated using the semiconductor parameters from which an estimation of losses is provided. A similar analysis is made for SiC MOSFET and GaN HEMT devices.

Chapter 3 provides further analysis for SiC MOSFET and GaN HEMT devices by experiments means and real measurements using evaluation boards from 2 different manufacturers. The results are compared against results obtained by LTSpice simulations using LTSpice models from the suppliers. Simulink models that allow to use the acquired data obtained during the experiments to dynamically calculate the losses are presented.

In chapter 4 a comparison between SiC MOSFET and a GaN HEMT based inverter is presented, and a device is selected for the inverter prototype. Within the technology selected a range of devices is compared to each other in order to select the device model that fits best the application in hands. Having selected the device, a gate driver is designed and all other elements of the inverter are sized, DC Link capacity, Current and Voltage measurements, Temperature measurements etc. The manufacturing process of all components of the Inverter are also described.

Chapter 5 shows the experimental testing and results of the developed prototype.

In chapter 6 conclusions about the developed work are given along with a track of the fulfilled objectives and suggestions for future work.

# Chapter 2

# Theoretical Background and Loss Analysis

In this chapter a mathematical formulation for the losses in a semiconductor working in a three phase inverter system is presented in order to provide an analytical loss analysis that compares losses among the current semiconductors used in the team's commercial inverter and two alternatives, a state of the art SiC MOSFET and a state of the art GaN HEMT.

A brief introduction on the formula student competition is given before, as well as a set of typical average vehicle parameters that provide a set of load cases for which losses are calculated and compared.

As a final note, a formulation is presented for thermal models of semiconductors given their importance in the design of a compact power converter, where heat management is a challenge.

## 2.1 Formula Student Competition

The Formula Student competition is an engineering competition that challenges students from universities across the world to design, build and compete with a small formula style racing car, where competition is divided in static and dynamic events. Static events include the evaluation of the design of the car, cost and sustainability of the project and a business presentation involving the car concept in a profitable company project. Dynamic events is where cars show their actual track performance in a total of five events:

- **Skid-Pad**, The car must follow a track delimited by two pairs of concentric circles in a figure of eight pattern;
- **Acceleration**, The car must follow a course of 75 meters in a straight line;
- **Autocross**, A 1 km track composed of several corners and straights;
- **Endurance**, A 22km course in a closed lap circuit;

- **Efficiency**, A ponderation between the energy spent on the Endurance Event and the elapsed time.

A depiction of those events is presented in Figure 2.1, apart from the efficiency event that occurs simultaneously to the endurance event.

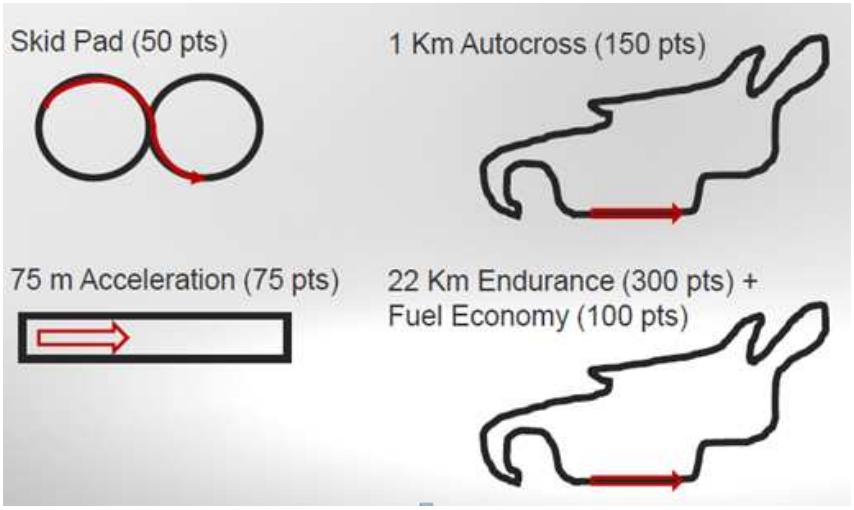



Figure 2.1: Formula Student Dynamic Events, Courtesy of Formula Student UK

To be able to compete in dynamic events the car must fulfill a vast set of rules that are checked for compliance in a technical inspection in the beginning of the completion. Only cars that are accepted at the rigorous technical inspection are allowed to participate in the dynamic events.

Since FST 07e, the team is using an all wheel powertrain drive achieved with 4 independent motors (one at each wheel), which means that each prototype has a total of 4 independent inverters.

In what concerns the loss calculations it is clear that they differ from one event to another: Acceleration event will yield the maximum power that will be drawn by the motor as well as the time of this peak power; Endurance Event will yield an average power required during the longest continuous operating time of the vehicle, that was considered to be around 22 to 25 minutes from past team experience; Autocross will also lead to an average power requirement, but with the difference that it is only required during a time period of about 60 seconds.

The average power required during the autocross track will be higher than the one required on the endurance, which put emphasis on the importance to have a higher efficiency in the Endurance profile, furthermore better efficiency during the endurance event means a better score at the Efficiency Event.

The power profiles (torque and velocity across each point of the track) for each of these events are a courtesy of the Vehicle Dynamics department of FST Lisboa that achieves such values using a simulator of the vehicle behavior across a given track. An example of this can be seen in Figure 2.2, where the total vehicle power is depicted over a track.

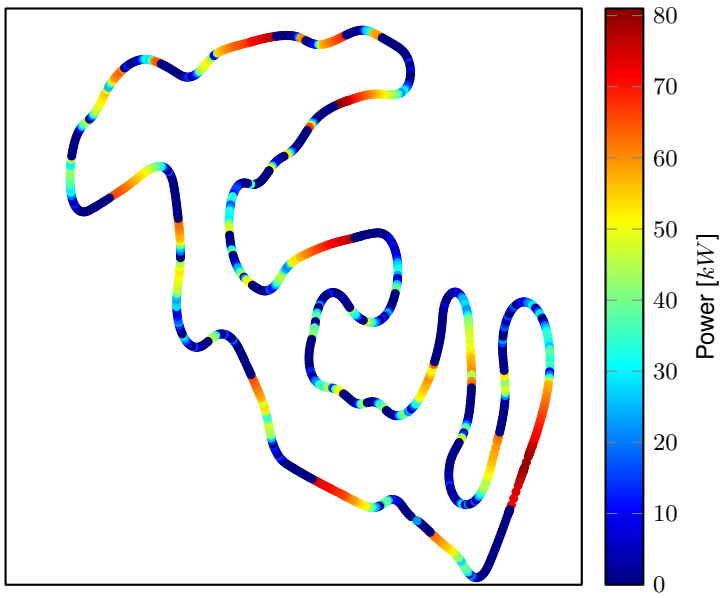



Figure 2.2: Simulation of vehicle output power over a track

## 2.2 Three-Phase Voltage Inverter

The three phase voltage source inverter is widely used in many power converter systems such as variable speed ac drives, uninterrutible power supplies, grid-connected systems, among many others.

In a general manner these inverters are controlled using Pulse Width Modulation (PWM) techniques.

Figure 2.3 shows a 2 Level voltage source inverter using IGBTs. If the DC-link voltage ripple is neglected and a linear modulation range is assumed, then voltages at phases can be expressed in the following way:

$$\begin{cases} u_A = mU\cos(\vartheta) \\ u_B = mU\cos(\vartheta + \frac{2\pi}{3}) \\ u_C = mU\cos(\vartheta + \frac{4\pi}{3}) \end{cases} \tag{2.1}$$

where $\vartheta = \omega t$, $\omega$ is the fundamental angular frequency ($\omega = 2\pi f$), and $m$ is the inverter modulation index representing the amplitude of the fundamental output voltage at the phase normalized by the dc supply voltage.

Furthermore, if a balanced load is considered and the output current ripple is neglected, the currents are expressed as:

$$\begin{cases} i_A = I_0\cos(\vartheta - \varphi) \\ i_B = I_0\cos(\vartheta + \frac{2\pi}{3} - \varphi) \\ i_C = I_0\cos(\vartheta + \frac{4\pi}{3} - \varphi) \end{cases} \tag{2.2}$$

where $I_0$ is the current amplitude and $\varphi$ is the phase angle between the voltage and current.

Using a power balance between the input DC power and the power in each phase and neglecting

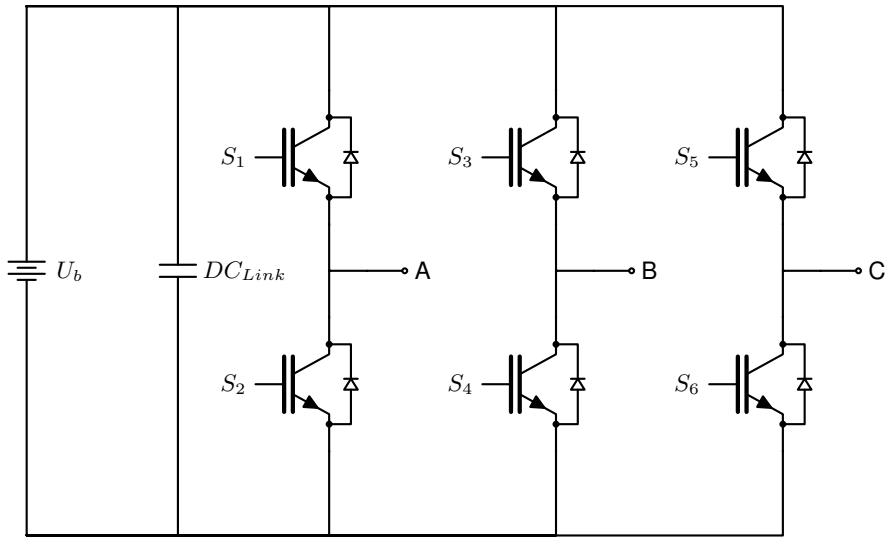



Figure 2.3: IGBT 3 Phase 2 Level Inverter

the power losses in the inverter, it is possible to use equations 2.1 and 2.2 to derive an average input current:

$$I_{DC} = \frac{3}{2} m I_0 \cos(\varphi) \tag{2.3}$$

Despite the transistor technologies used, it is possible to create relations between the output current and the current at the transistors. This relation is important for loss calculations on the transistors themselves. It is also important to note that the transistors switching losses are highly dependent on the instantaneous current that flows through the transistor at the switching moment. This way those relations are important not only for the calculation of losses but also for the semiconductor selection.

The RMS current on the transistors in function of the current on the phase can be obtained by:

$$I_{S_{rms}} = \frac{I_{Phase_{RMS}}}{\sqrt{2}} \tag{2.4}$$

The maximum current that the transistor will be subjected to is intuitively given by:

$$I_{S_{max}} = I_{Phase_{RMS}} \cdot \sqrt{2} + \Delta i_0 \tag{2.5}$$

where $\Delta i_0$ is the maximum ripple current.

A closer look at the currents on the semiconductors is done for this topology given the importance it has on the semiconductor losses, where a great part of the efforts on this thesis are placed, with particular emphasis on the loss calculation for sinusoidal current outputs that differs from loss values typically provided in manufacturers datasheets. More equations describing the voltages at phases and the switches possible states exist[11] but with less focus on this thesis, since a special focus is given to the semiconductor operation parameters instead of the characteristics at the load.

## 2.3 3-Phase Inverter Losses

On this section classical losses equations are introduced for 3 types of transistors:

- IGBT
- MOSFET
- HEMT

For each one of these transistor technologies, the equations for the freewheeling diodes losses are also included when needed. HEMT transistors do not require a freewheeling diode, while for MOSFET the freewheeling diode serves mainly for the dead time since the channel, when active, conducts in both directions (channel resistance derating for reverse conduction is not considered though it exists [12, 13]). For IGBTs the freewheeling diodes are mandatory given the inherent incapability of reverse conduction.

### 2.3.1 IGBT

For these transistors losses can be divided into two categories:

- Conduction Losses - This losses relate to the RMS current that flows through the transistor channel which obviously as a resistance;
- Switching Losses - This losses relate to the energy necessary to create and destroy the conductive channel that the transistor provides.

The instantaneous conduction power loss of the IGBT is given by:

$$P_{Cigbt} = v(t) \cdot i(i) = (V_{CE} + R_{on} i(t)) i(t) = V_{CE} i(t) + R_{on} i(t)^2 \tag{2.6}$$

Therefore the average conduction losses across a switching period can be given by:

$$P_{Cigbt_{avg}} = \frac{1}{T} \int_0^T v(t) i(t) = \int_0^T V_{CE} i(t) + R_{on} i(t)^2 = V_{CE} I_{avg} + R_{on} I_{rms}^2 \tag{2.7}$$

The switching losses are typically given by[11]:

$$P_{Sigbt} = V_{CE} i(t) \frac{t_{S_{ON}} + t_{S_{OFF}}}{2T} + (V_{CE} I_{tail} \frac{t_{tail}}{2T}) \tag{2.8}$$

Where $t_{S_{ON}}$ and $t_{S_{OFF}}$ are the turn on and turn off times of the device, $I_{tail}$ and $t_{tail}$ are the tail currents and the time associated with such current respectively.

Still most manufacturers do not supply the necessary parameters of the transistor in order to use equation 2.8. They do however supply the Energy loss during turn on, $E_{on}$, and during the turn off, $E_{off}$, of the semiconductor at a given voltage and current. At that particular voltage and current one can write the following simplified expression:

$$P_{Sigbt} = \frac{E_{on} + E_{off}}{T} \tag{2.9}$$

Still this is not useful if one is working outside the voltage and current where the manufacturer measured the switching energies, therefore a normalization must be done. Looking at equation 2.8, one can claim there should be a linear variation with voltage and current applied at the semiconductor during the switching event, therefore we can re-write 2.9:

$$P_{Sigbt} = \frac{E_{on} + E_{off}}{T} \cdot \frac{U}{U_{nom}} \cdot \frac{I}{I_{nom}} \tag{2.10}$$

where $U$ and $U_{nom}$ are respectively the actual voltage applied to the semiconductor and the voltage specified by the manufacturer, and similarly $I$ and $I_{nom}$ are respectively the actual current during the switching and the current specified by the manufacturer. It is still important to keep in mind that this is a far from ideal manner of calculating the semiconductor losses. Equation 2.10 will be the equation used for the calculation of IGBT losses of the current team's inverter.

The freewheeling diode conduction losses have a quite similar approach:

$$P_{Cdiode} = \frac{1}{T}\int_0^T v(t)i(t) = \int_0^T V_D\, i(t) + R_d\, i(t)^2 = V_D I_{avg} + R_d I_{rms}^2 \tag{2.11}$$

where $V_D$ and $R_d$ are the forward voltage and forward resistance of the diode, respectively.

### 2.3.2 MOSFET

Unlike the IGBT, the MOSFET provides a conduction channel with no threshold voltage, and as far as conduction losses go the resistance of the channel, $R_{ds_{on}}$ is the dominant parameter. As a result the instantaneous conduction power losses, $P_{Cmosfet}$, can be given by:

$$P_{Cmosfet} = R_{ds_{on}} i(t)^2 \tag{2.12}$$

Averaging for a switching period, it can be written:

$$P_{Cmosfet_{avg}} = \int_0^T R_{ds_{on}} i(t)^2 = R_{ds_{on}} I_{rms}^2 \tag{2.13}$$

The switching losses for the MOSFET can be split into 3 components, turn-on losses ($P_{on}$), turn-off losses ($P_{off}$) and the losses related to the charging and discharging of the output capacitance ($P_{Coss}$). Having the turn on, $T_{s_{on}}$, and turn off, $T_{s_{off}}$, times of the MOSFET the switching losses are calculated as follow:

$$P_{on} = \frac{1}{2} T_{s_{on}} V_{dd} I_d \frac{1}{T} \tag{2.14}$$

$$P_{off} = \frac{1}{2} T_{s_{off}} V_{dd} I_d \frac{1}{T} \tag{2.15}$$

$$P_{Coss} = \frac{1}{2} Coss V_{ds}^2 \frac{1}{T} \tag{2.16}$$

And the total switching losses, $P_{Smosfet}$, become:

$$P_{Smosfet} = P_{on} + P_{off} + P_{Coss} \tag{2.17}$$

The freewheeling diode conduction losses is identical to equation 2.11

### 2.3.3 HEMT

HEMT conduction losses are quite similar to the MOSFET in the sense that they depend on the resistance of the channel created for conduction. Although the properties of such channel are quite different since they rely on a 2 Dimensional Electron Gas, a channel so thin that electrons travel with very few collisions [14], hence the high mobility. Such channel creation and destruction is a rather complex process. Analytical equations exist for the switching losses though they use an extensive number of transistor parameters not supplied by the manufacturers (dimensional parameters, material properties, electron material densities ...).

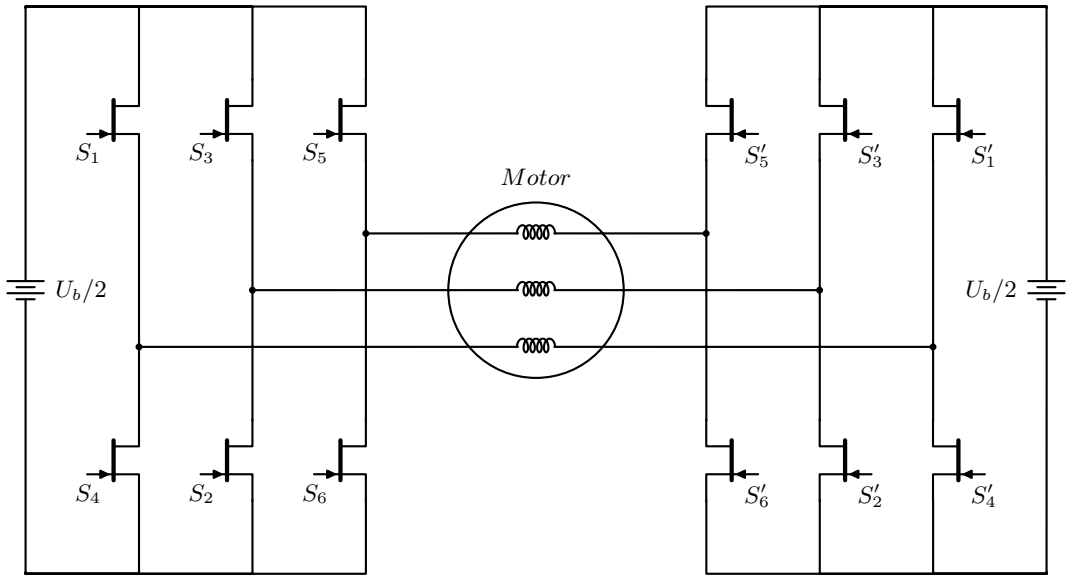



Figure 2.4: GaN HEMT Double Inverter configuration for open-winding motor

Taking the above into consideration, the conduction losses approach will be similar to the MOSFET, equation 2.13 and as far as switching losses is concerned the $E_{on}$ and $E_{off}$ parameters from the manufacturer are used resorting to equation 2.10.

On the particular case of GaN HEMT, as of this day the maximum voltage rating of the market available transistors is not higher than 650 V, though it is theoretically possible to reach much higher voltages [9]. This makes them unsuitable to use in a 2 Level 3-Phase inverter with an input voltage of 600 V, remembering that a margin must be given for transient voltage overshoots, typically at least 50% of the input voltage.

However, it is possible to use different configurations, namely a 3 Level Open Winding inverter where the required hold-off voltage is half of $U_b$, basically this new configuration is composed of 2 inverters that

supply an open-winding motor as per Figure 2.4.

The loss calculation for HEMT will take in consideration a double inverter for open-winding inverters. Although control complexity increases, this configuration allows the same benefits as for a three Level Inverter, having more control vectors with a resulting reduction in harmonic distortion when compared to a normal 2 Level Inverter [15]. The same apply as well in terms of reducing current and torque ripple and an increase in efficiency [16].

This configuration is quite interesting specially taking into consideration that the motors are now developed by the team, providing a new design variable that can be further explored in the future.

## 2.4 System Definition

The powertrain on a race vehicle is highly dynamic, constantly changing the velocity and torque applied. Actually rare are the conditions when a race vehicle has a constant velocity. That creates challenges in many areas of the powertrain development, specially as far as losses estimation goes. A first approach of the estimation of losses is to use average velocities and torque values supplied by the Vehicle Dynamics department of the FST Lisboa team.

The current powertrain system used on FST 07e and FST 08e specifications can be seen on table 2.1.

Table 2.1: FST 07e General Powertrain Parameters

| **Parameter** | **Symbol** | **Value** |
|---|---|---|
| Battery Voltage Min | $U_{min}$ | 450 V |
| Battery Voltage Maximum | $U_{max}$ | 600 V |
| Battery Voltage Nominal | $U_{nom}$ | 500 V |
| Maximum Power | $P_{max}$ | 80 kW |
| Number of Motors | | 4 |
| Maximum Power per Motor | $P_{m_{av}}$ | 25 kW |
| Typical Average Power | $P_{av}$ | 28 kW |
| Maximum Average Power (1 min) | $P_{av_{max}}$ | 60 kW |
| Maximum Current DC | $I_{U_{max}}$ | 160 A |
| Maximum motor current RMS (1,24s) | $I_{max}$ | 100 A |
| AMK Inverter Switching Frequency | $f_{sw}$ | 8 kHz |
| Motor Frequency at Maximum Speed | $f_o$ | 1.6 kHz |
| Rated Motor Current | $I_n$ | 41 Arms |
| Rated Motor Voltage | $U_n$ | 350 V |
| Average Current per phase | $I_{av}$ | $\frac{41\sqrt{2}}{2\sqrt{3}}$ |
| RMS Current per phase | $I_{RMS}$ | $\frac{41}{\sqrt{3}}$ |
| Maximum Speed | $N_{max}$ | 20000 RPM |
| Motor Number of Poles | $p$ | 10 |
| Quadrature Axis Inductance, | $L_q$ | 0.54 mH |
| Direct Axis Inductance | $L_d$ | 0.44 mH |
| Rotor time constant | $T_r$ | 0.01 s |
| Maximum Torque | $M_{max}$ | 21 Nm |
| Torque constant | $k_t$ | 0.26 $Nm/A_{rms}$ |
| Voltage constant | $k_e$ | 18.8 $V/kRPM$ |

The presented set of parameters will be used to calculate the expected losses in the inverter.

The maximum output frequency, $f_e$, is defined by the maximum speed of the motor, $N$, as well as its number of poles, $p$. The synchronous electrical speed of a synchronous AC machine is given by[17]:

$$N = \frac{120 f_e}{p} \tag{2.18}$$

Therefore,

$$f_e = \frac{Np}{120} = 1666.(6)\, Hz \approx 1.67\, kHz \tag{2.19}$$

This value will influence the switching frequency of the inverter, since it is desirable to have a pulse index that not only is odd to ensure wave symmetry (in a variable frequency driver this implies automatically a variable switching frequency) but also is much higher than the output frequency $f_s >> f_{out}$ [18].

Since the provided values for the car load profile come in the form of torques and speeds, relations must be created in order to obtain the root mean square of the physical quantities necessary for the losses calculations.

One of those relations is the relation between torque and current where one can use the motor torque constant $k_t$ [17]:

$$I_{phase_{RMS}} = \frac{Torque}{k_t} \tag{2.20}$$

The other relation is between the back electromotive force, $V_{EMF}$, and the motor velocity [17]:

$$V_{EMF} = k_e \cdot MotorSpeed \tag{2.21}$$

These relations will allow to extract approximate currents that will allow loss calculations for each event.

Losses will be calculated for 3 load cases:

- **Case A**: Maximum Torque;
- **Case B**: Average Torque of 5 Nm per Motor;
- **Case C**: Average Torque of 9 Nm per Motor.

Case A will be very close to an acceleration event. Case B uses the average torque of an endurance event. Case C uses the average torque of an autocross event.

Using equation 2.20 one can derive the average RMS currents of the motors:

$$\begin{cases} I_{A_{rms}} = \frac{21}{k_t} \approx 80\, A & \text{, For Case A} \\ I_{A_{rms}} = \frac{5}{k_t} \approx 34\, A & \text{, For Case B} \\ I_{A_{rms}} = \frac{9}{k_t} \approx 19\, A & \text{, For Case C} \end{cases} \tag{2.22}$$

These currents are the RMS currents at the phases. Making use of equation 2.5 and equation 2.4 respectively, the maximum and RMS current at the transistors can be calculated.

The average speed on an endurance event is near 60 km/h and slightly higher on the autocross. For the used power during an event it is easier to use actual track data of the measured energy during these events, where the team can supply average times for the endurance and autocross as well as the energies spent on both events.

Calculation for losses analysis use a switching frequency of 8 kHz since this is the current switching frequency of the FST 07e Inverter.

## 2.5 Results

The loss equations on sections 2.3.1, 2.3.2 and 2.3.3 are here applied to the load cases presented on the previous section.

The current FST 07e inverter uses a 6-pack IGBT with an included body diode from Infineon, FS200R12PT4[19]. As a SiC MOSFET contester a state of the art solution from Wolfspeed is considered, C2M0025120D [20]. Similarly for GaN a state of the art device is also selected, this time a GaN Systems device, GS66516T [21]. The required parameters for losses calculation are supplied by the data sheets of these devices.

Using the presented equations is quite trivial with a small exception of the switching losses given that, they depend on the instantaneous currents during the switching time, since the currents are not constant. However, given that the switching frequency is considerably higher than the output frequency during most of the inverter operation, and if symmetry is considered, then it is possible to average the value of such current during half a period. This can be shown considering the definition of average power during half a period as:

$$P_{avg} = \frac{1}{\Gamma/2}\int_0^{\Gamma/2} P_{sw}(t)dt = \frac{1}{\Gamma/2}\int_0^{\Gamma/2} V_{cc} i(t)\frac{t_{son}+t_{soff}}{2T}dt \tag{2.23}$$

where $\Gamma$ is the period of the output current wave. Given that the current is the only variable that changes, and again resorting to the definition of average power:

$$P_{avg} = \frac{V_{cc}(t_{son}+t_{soff})}{2T}\frac{1}{\Gamma/2}\int_0^{\Gamma/2} i(t)dt = V_{cc} I_{avg}\frac{t_{son}+t_{soff}}{2T} \tag{2.24}$$

That will lead to the average value of a half-sinusoid:

$$I_{avg} = \frac{2I_{max}}{\pi} = \frac{2I_{rms}}{\sqrt{2}\pi} \tag{2.25}$$

Results for cases A, B and C can then be calculated for a Silicon IGBT, SiC MOSFET and GaN HEMT inverter, where the Silicon IGBT and SiC MOSFET inverter use a topology as per Figure 2.3 and the GaN HEMT uses a topology as per 2.4, with the particular note that two GaN HEMT devices must be placed in parallel to be able to safely handle the required currents. Such results can be found in table 2.2.

It is important be noticed that those values consider a switching frequency of 8 kHz. The higher the

Table 2.2: Total losses per semiconductor in cases A, B and C

| Total | Silicon IGBT [W] | SiC MOSFET [W] | GaN HEMT [W] |
|---|---|---|---|
| Case A | 1684.3 | 1023.9 | 1265.5 |
| Case B | 504.7 | 66.5 | 74.1 |
| Case C | 772.9 | 199.3 | 235.6 |

frequency, the greater will be the difference between the losses of the IGBT and the SiC MOSFET, since the switching losses are considerably smaller on the SiC MOSFET. The same is valid for the GaN HEMT and the SiC MOSFET (where the GAN HEMT losses are lower).

This serves as a preliminary analysis to see that there are clear advantages in changing to new semiconductor technologies. Still further analysis must be done before actually making the decision of which technology to use, such analysis will be done experimentally in chapter 3.

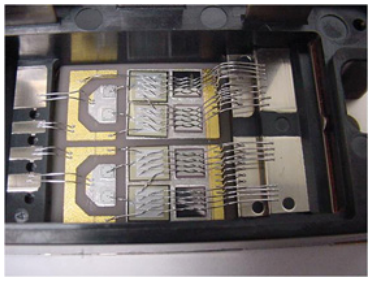
## 2.6 Thermal Model

When designing a 3-phase inverter it is important to understand the system's limitations. One of those limitations is a thermal one, particularly the temperature of the semiconductors.

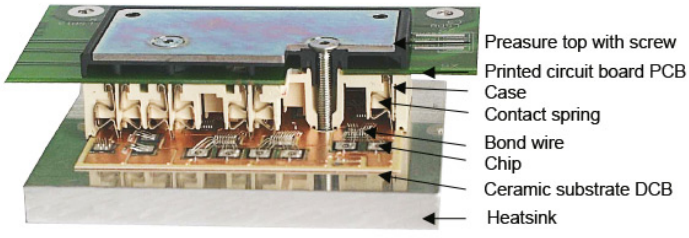
A major advantage in this field of SiC devices versus typical Si devices and GaN devices is that the SiC presents a much higher thermal conductivity (up to tree times higher)[22]. Even so, temperature is still a critical parameter, for example most Cree's SiC devices cannot withstand junction temperatures above 150 °C, and most of the devices parameters vary significantly with temperature.

Taking this into consideration, major benefits can be achieved by designing a thermal model of the devices. Such thermal model can then feedback the temperature so that the losses models can take the junction temperature into account.

Thermal behavior depends highly on the package used. Currently it is possible to find SiC devices that use standard TO-247 packages, thermally enhanced TO-247 packages, and even custom dedicated packagings specifically designed by the manufacturer, Figure 2.5.



(a) Thermally enhanced TO-247 Package for a SiC Device




(b) Custom packaging for a 2 Level 3-Phase Inverter SiC configuration

Figure 2.5: Examples of SiC Packagings

Junction temperature is typically the critical temperature point and even the best devices in the market can not handle temperatures above 200 °C. The temperature of the junction will be function of the power losses and the case temperature, that in turn will be function of the heatsink temperature. A model will

be designed such that junction temperature can be estimated. With this model it will then be possible to compare the thermal performance of different devices from different manufacturers.

Several authors tested SiC devices failure modes under high temperature conditions [23–26]. Any of those studies show the temperature dependence of the device properties, proving that it is extremely important to take temperature into account when designing the power module.

The models can be designed in one of two ways, with a steady state analysis where it is assumed that temperature differences are propagated instantly for each dissipated, or with a transient analysis where the thermal capacity of the materials is taken into account.

### 2.6.1 Steady State Analysis

A simple steady state model that allows to understand the temperature difference from junction, $T_j$, to case, $T_c$, can be achieved using only the thermal conductivity of the different materials present in the semiconductor. Thermal conductivity is measured in watts per meter-kelvin ($W \cdot K^{-1} \cdot m^{-1}$). Instead of supplying the different materials and thicknesses used in the fabrication of the semiconductor, manufacturers supply a thermal resistance from junction to case ($R_{\theta j-c}$) measured in kelvin per watt ($K/W$).

Using this thermal resistance one can calculate the junction temperature in function of the case temperature and the dissipated power in the following way:

$$T_j = T_c + P_d R_{\theta j-c} \tag{2.26}$$

This can be further extended into the ambient temperature if one knows the thermal resistances from case to the heatsink($R_{\theta c-s}$), and from the heatsink to the ambient($R_{\theta s-a}$). This way it is possible to use the following equation[11]:

$$T_j = T_a + P_d(R_{\theta j-c} + R_{\theta c-s} + R_{\theta s-a}) \tag{2.27}$$

Still it is important to emphasize that this is a steady state model, and therefore no transient effects are considered.

Increasing power density calls for the need of better models so that transient effects can be taken into account[27].

### 2.6.2 Transient Analysis

To include transient effects, the thermal mass of the materials must be considered. It is possible again to use an electrical analogue to represent this thermal mass, in this case modeled by a capacitor, $C_\theta$. This thermal capacitance is function of properties of the materials:

$$C_\theta = c_p \rho V \tag{2.28}$$

where $c_p$ is the specific heat of the material, $\rho$ is the volumetric mass density and $V$ is the volume.

The combination of this thermal resistance and capacitance gives a thermal time constant that similarly to the electrical analogue, from point a to point b, can be given by:

$$\tau_{\theta a-b} = R_{\theta a-b} C_{\Theta a-b} \tag{2.29}$$

This way as long as the manufacturer supplies a thermal resistance and capacitance from junction to case it is possible to calculate the temperature difference from junction to case over time for a step profile in the dissipated power, with amplitude $P_0$, in the following way:

$$\Delta T = R_{\theta j-c} P_0 (1 - e^{-t/\tau_\theta}) \quad , \quad \tau_\theta = R_{\theta j-c} C_{\theta j-c} \tag{2.30}$$

However this is a very simplified model, assuming only one equivalent thermal resistance and capacitance from junction to case disregards the several layers of different materials that compose the semiconductors and their packaging. On a better approach, RC networks are used to better model the different layers of the semiconductor. Two different models can be used with RC networks, Cauer and Foster networks are two different approaches for the RC network. Figure 2.6 and 2.7 shows this composition using the Cauer and Foster network, respectively. A Cauer network is a closer representation of the physical form of the thermal circuit because each node represents a real temperature [27]. Still this depends on packing details that are not often supplied by the manufacturers. Instead some researchers prefer to use the Foster network model, where the order of the RCs does not represent the number of layers, but the accuracy of mathematical approximation[28].

Furthermore, the transient thermal impedance is directly available in the datasheet, making it easy and fast to get the values of the RC network by curve fitting[28].

Taking a closer look at the Foster network (Figure 2.7), it is possible to calculate the thermal impedance as:

$$Z_{th} = \sum_{i=1}^{n} R_i \left[ 1 - exp\left( -\frac{t}{R_i C_i} \right) \right] \tag{2.31}$$

and the junction temperature is given by:

$$T_j = T_c + P_{Loss} Z_{th} \tag{2.32}$$

Some manufacturers actually provide the Cauer network parameters for simulation. Wolfspeed, for example, supplies Cauer networks models for their transistors with up to 16 RC elements. Even with

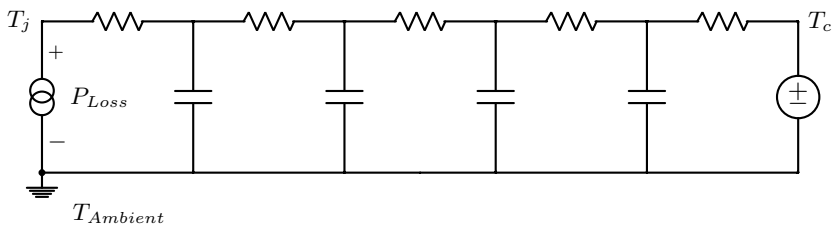



Figure 2.6: Thermal model of semiconductor layers using Cauer Model

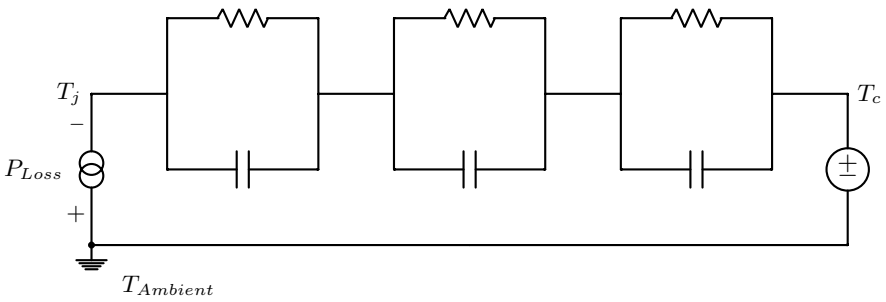



Figure 2.7: Thermal model of semiconductor layers using Foster Model

all the MOSFET Layers plus soldering and baseplate, there are less than 16 different layers involved in the thermal conduction path. Still to better capture the thermal behavior of a material where dissipated power is applied at a high frequency it is important to note that modeling an entire layer of a given material by a single RC thermal circuit assumes instant propagation of heat through that material. Such approximation is good enough for low frequencies but starts to present a considerable error when frequency increases[27]. Actually using a RC thermal element is a discretization of a continuous phenomenon. Some researchers propose the use of higher order RC networks to describe a single material [27]. For the reasons explained before, it is straightforward the use of high order Cauer networks to model thermal propagation across the layers of the semiconductors.

There is still one more considerable advantage in using a Cauer network instead of a Foster network. When the manufacturers supply a Cauer model it is trivial for a user to add more layers after the semiconductor, such as thermal greases and heatsink contacts by using more RC elements in series with the ones provided, while on the other hand Foster network would require new curve fitting. This, for example, is exactly the justification given by a well known power semiconductor devices manufacturer, GaN Systems, for having selected to supply Cauer network parameters instead of Foster network parameters [29].

# Chapter 3

# Experimental Determination of Semiconductor Losses

This chapter presents a methodology for power losses estimation in semiconductors functioning in an inverter power converter with sinusoidal output currents. The presented methodology is a experimental one, which is based on a calibration and a set of temperature measurements in thermal equilibrium. Such methodology is applied to both a GaN HEMT device and a SiC MOSFET device. The results estimate not only the total power losses but distinguish between conduction losses and switching losses. A comparison between the two is provided and in light of that data a semiconductor technology is selected to design a three phase inverter.

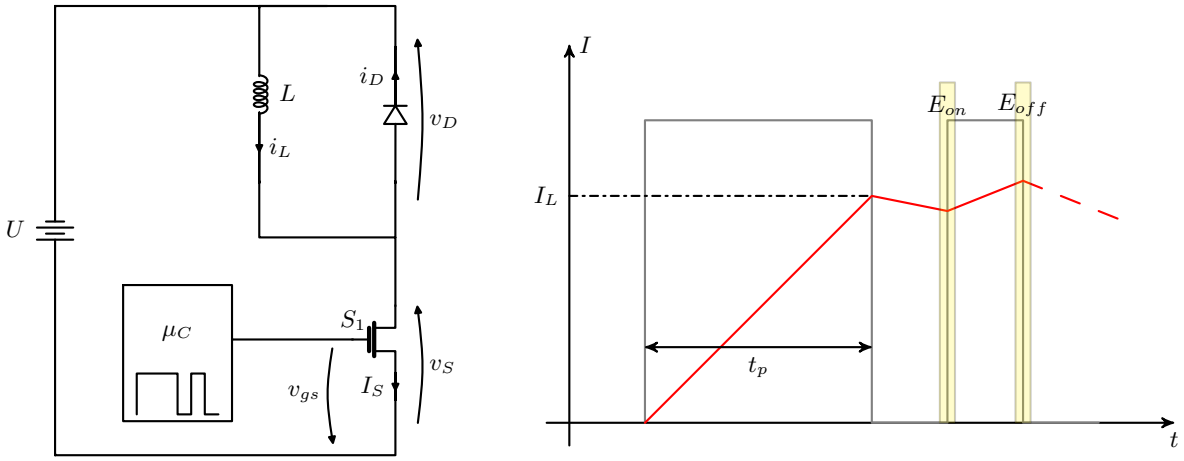
Finally, models are created that can calculate the losses dynamically for a given output current based on the acquired data. Such approach will facilitate the process of power losses estimations in dynamic environments that will improve the design of the cooling department of the team.

## 3.1 Methodology

Analytical analysis is somewhat limited for the analysis of a 3 Phase inverter in the suggested conditions (constantly changing output current and frequency). Temperature dependency of the parameters is not taken into account as well as other non linearities associated with the constantly varying output frequency and amplitude of the current. For that reason in this chapter, laboratory measurements were done in order to estimate conduction and switching losses in several conditions, allowing to obtain results that are specifically oriented for a leg inverter operation in a PWM Modulation schema.

First approach was to perform a double pulse test to measure the switching losses under different load currents. Using the circuit from Figure 3.2(a), it is possible to control the switching current by controlling the time of the pulse $t_p$, producing a waveform similar to Figure 3.2(b).

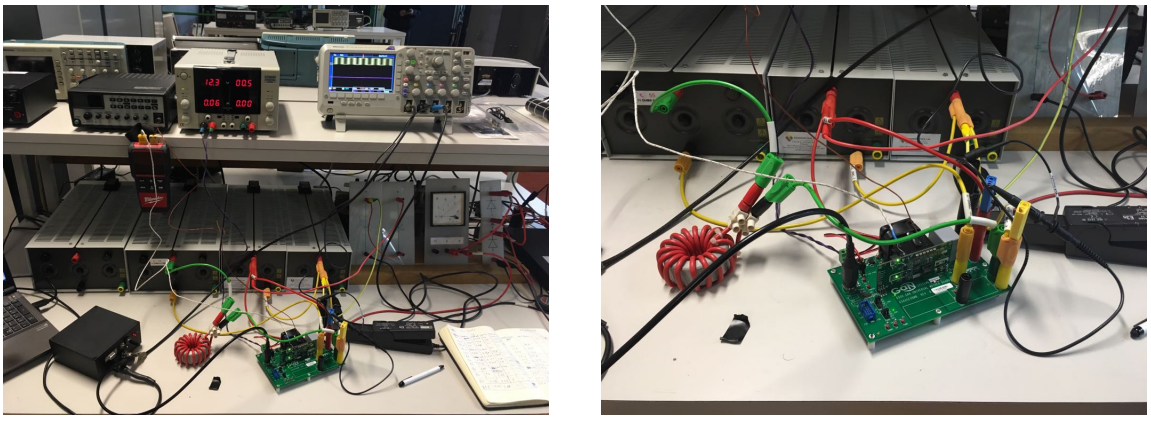
Assuming that for $t = 0$ no current flows through the inductor, the current at which the transistor




(a) Double Pulse Test Circuit

(b) Double Pulse Test Waveform

Figure 3.1: Double Pulse Test Setup



(a) Full View

(b) GaN HEMT and Inductor Focus

Figure 3.2: Double Pulse Test Setup

switches can be given by:

$$I_{sw} = \frac{1}{L}\int_0^{t_p} v(t)dt = \frac{V}{L}\int_0^{t_p} dt = \frac{V \cdot t_p}{L} \tag{3.1}$$

Using equation 3.1, it is possible to control in a easy manner the current at the transistor when switching occurs only by knowing the inductance of the used inductor and measure the switching energies by measuring the voltage and current during the switching process.

This test setup was mounted on the Laboratory of the Energy department of Instituto Superior Técnico and can be seen in Figure 3.2.

The current measurements were made using a current shunt and measuring the voltage across the terminals of the shunt. A small profile surface mount current shunt was used with a resistance of about 0.01 Ohm. The results were not as good as initially expected due to the high current transients, $\frac{di}{dt}$, during switching and the shunt resistor parasitic inductance. A higher bandwidth current shunt would be necessary but was not available at the laboratory where the tests were performed. The used shunt resistor can be seen in Figure 3.3.

Therefore a different approach to measure the switching losses was necessary. The FST Team,

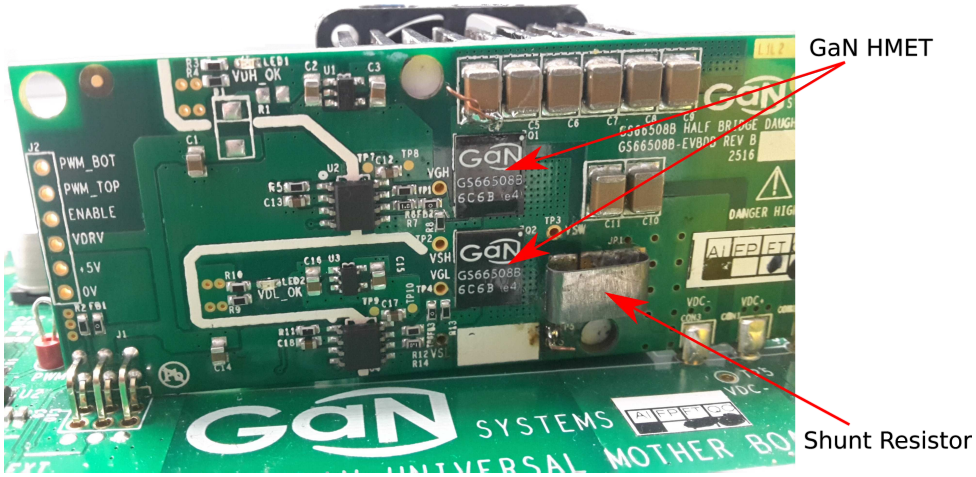



Figure 3.3: GaN Evaluation Board with detail on Shunt Resistor

has for some time, a thermal camera that allows to measure temperature where otherwise would be dangerous to place a temperature sensor such as a thermocouple.

The proposed and used method is based on the relation between dissipated power and the temperature increase of the semiconductors. To do so the setup was instrumented with temperature sensors and the following procedure is used:

1. Place the system under the operating condition for which to measure losses:
    - Switching Frequency;
    - Output Frequency;
    - DC Link Voltage;
    - Modulation Factor;
    - Output Current.
2. Ensure safe operating conditions (peak voltages and currents during switching).
3. Wait until the systems achieves thermal equilibrium.
4. Measure the temperature increase in the semiconductors and heatsink when thermal equilibrium is achieved.

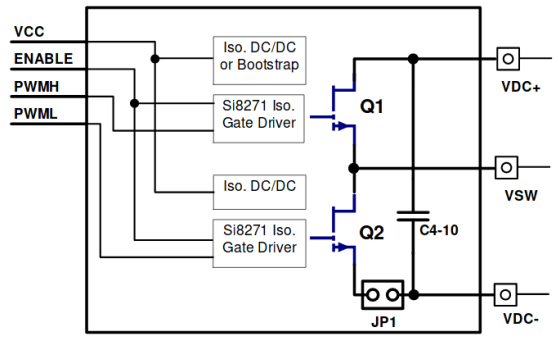
To then be able to convert the measured temperature into dissipated power, a calibration must be done to each test setup. Such calibration is done in the following way:

1. Connect a current limited capable power supply to the transistors leg;
2. Drive both transistors in order to achieve a conductive state for both;
3. Limit the current in order to achieve some pre defined dissipated power (at the cost of the on resistance of the transistor);

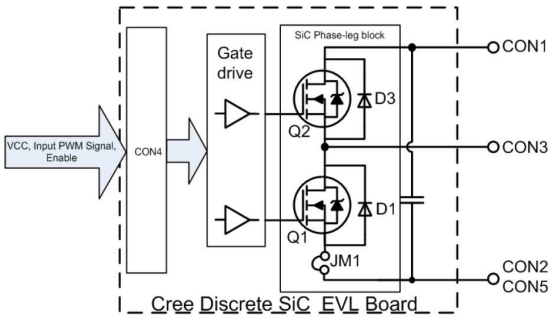
4. Measure the temperature increase in the semiconductors and heatsink when thermal equilibrium is achieved.

These tests are performed using the material available at the Laboratory of the Energy department, including two evaluation boards for the GaN (GS66508B-EVBDB [30]) and SiC (KIT8020-CRD-8FF1217P-1 [31]) transistors.

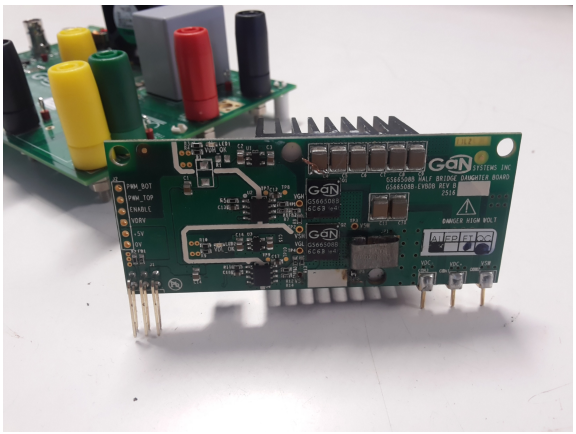
Each evaluation board provides two transistors in a leg configuration and their associated isolated gate drivers, as well as decoupling capacitors. In the case of the SiC evaluation board it also provides two SiC Schottky freewheeling diodes. A simple schematic of the GaN and SiC evaluation boards can be seen, respectively, in Figures 3.4(a) and 3.4(b).



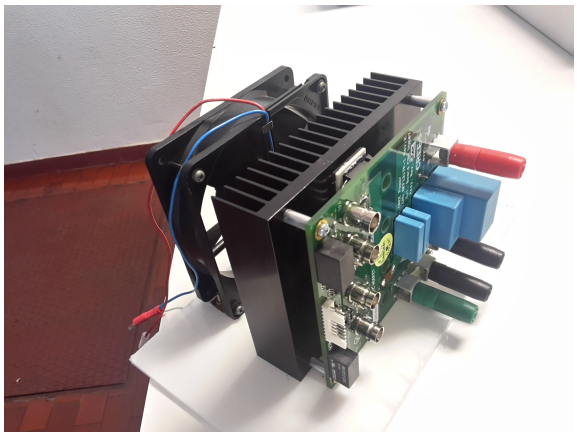

(a) GaN, courtesy of *GaN Systems*




(b) SiC, courtesy of *Wolfspeed/CREE*



(c) GaN, courtesy of *GaN Systems*



(d) GaN, courtesy of *GaN Systems*

Figure 3.4: Evaluation Boards Simplified Schematics

Table 3.1 sums up some of the most important parameters of the devices used in the evaluation boards. These devices are not the ones considered in the analytical loss analysis since they do not match the properties of the IGBT used in the FST 07e powertrain. However results taken from these devices can be extrapolated to lower $R_{DS_{on}}$ devices available from the manufacturer.

The experiments performed were always in a leg inverter operation, particularly in a half bridge configuration with a middle point balanced with capacitors as shown in Figure 3.5.

As mentioned above, a thermal camera along side with thermocouples were used to take the temperature measurements. Figure 3.6 shows the laboratory apparatus were measurements were done with the thermal camera. The used thermal camera is the M12 Thermal Imager[32] from Milwaukee,

Table 3.1: Parameters of the GaN and SiC transistors used in the evaluation boards

| | Gan Systems GS66508B | Wolfspeed C2M0080120D |
|---|---|---|
| On Resistance | $50m\Omega$ | $80m\Omega$ |
| Current Rating (Continuous) | 30 A | 36 A |
| Current Rating (Pulse) | 72 A | 80 A |
| Input Capacitance | 260 pF | 950 pF |
| Output Capacitance | 65 pF | 80 pF |
| Reverse Transfer Capacity | 2 pF | 7.6 pF |

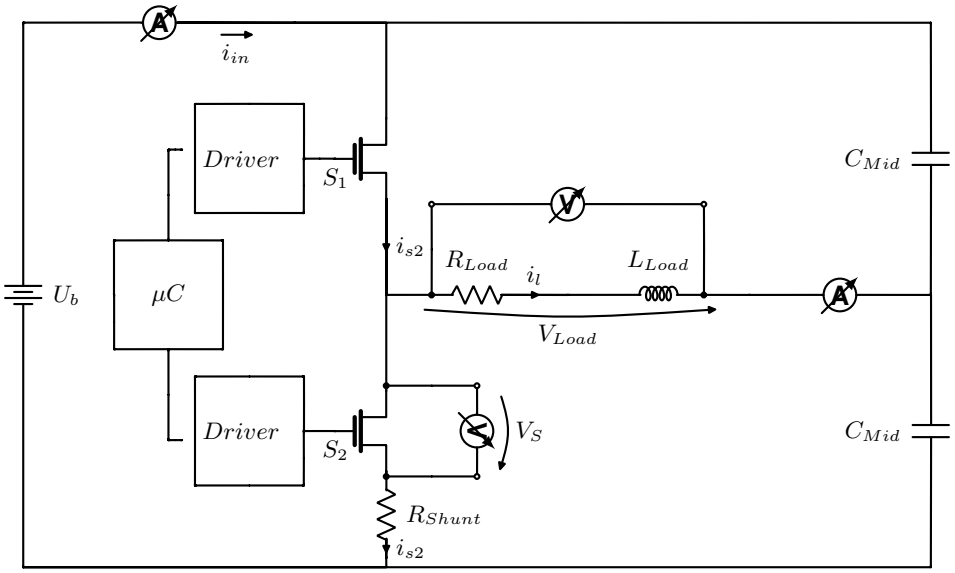
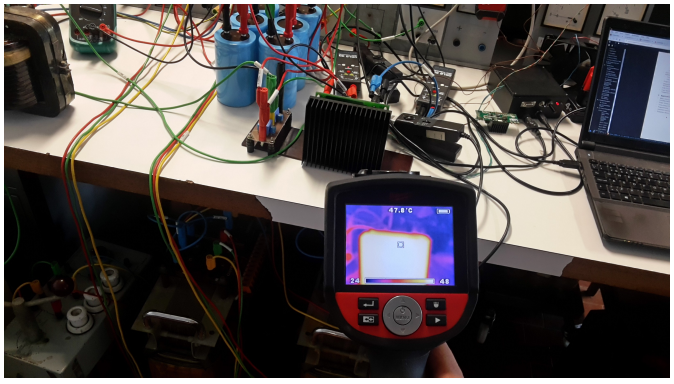



Figure 3.5: Half Bridge Inverter topology with capacitive middle point

that presents a resolution of 0.1 ° C and an accuracy of 1 ° C.



(a) Measurement on the Wolfspeed Evaluation Board


(b) Measurement on the GaN Systems Evaluation Board

Figure 3.6: Examples of temperature measurements with a thermal camera

Up to 4 K-Type thermocouple were used. The temperature was acquired using two devices, Milwaukee 2270-20 Contact Temp Meter[33] and the CENTER 306 Thermometer[34] both with a resolution of 0.1 ° C and an accuracy of 1 ° C. Figure 3.7 shows the use of these devices to measure different temperatures at different locations of the device under test.

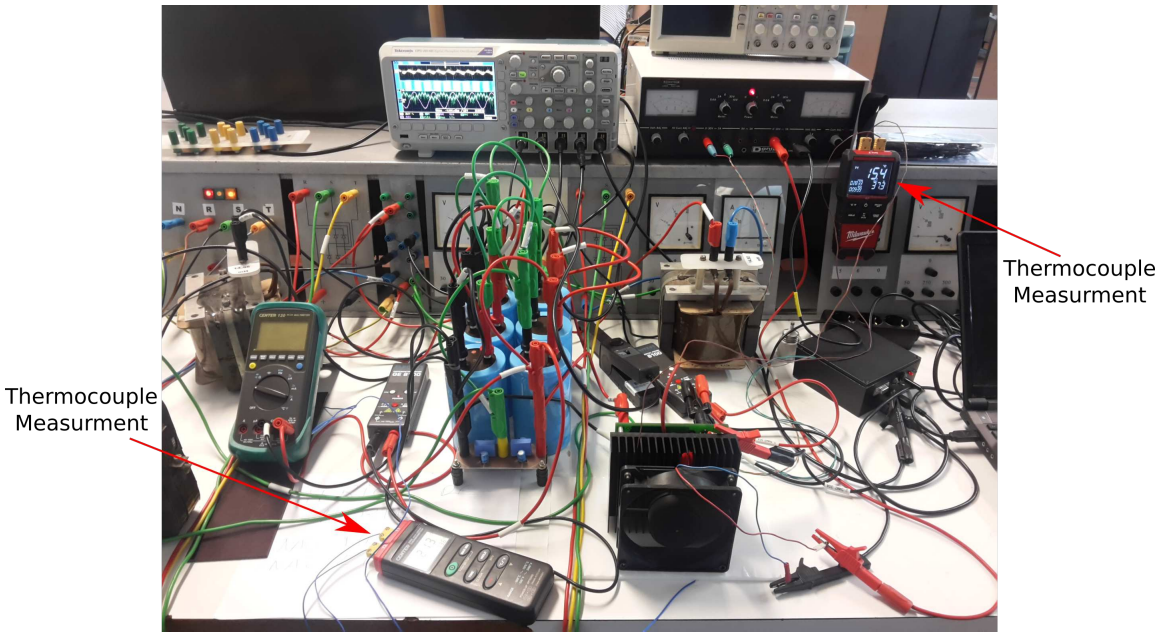



Figure 3.7: Example of temperature measurement with thermocouples

During experiments with both SiC MOSFET and GaN HEMT and during calibration special attention was taken to the places were such measurements where done, particularly ensuring that the measurements were done always in the same exact places. This is an important issue to take into account because, for example, the temperature at the heat sink will vary along its surface. The same is true for the measurements using the thermal camera. The focus points used in calibration were and must be the same focus points used during the experiments. Furthermore, with the thermal camera it was also important to maintain a constant distance from the measuring equipment to the point being measured across experiments.

## 3.2 Calibration

As stated before, in order to provide a correct relation between the temperature rise and the dissipated power, a calibration of the laboratory apparatus is necessary since the thermal resistance from each element of the system up to the junction is unknown resulting in a estimation that would lead to an error difficult to quantify.

Given the low on resistance of these devices, a quite considerable current is necessary to reach the desired dissipated powers.

Figure 3.8 shows one of the many calibrations done throughout the tests. A total of 3 power supplies were used in parallel to supply a current of up to 22 A.

On the calibration procedure not only a relation between power and temperature rise is obtained but also the variation of the channel resistance with temperature.

Several changes to the test setup had to be done throughout the course of the experiment in order to achive a test setup from which consistent results could be obtained. For each change in the test

(a) (b)

Figure 3.8: Calibration Test Setup for the SiC devices

setup a new calibration had to be done to ensure that calibration data best fitted the actual conditions at which the experiment was done. The presented calibration results are the ones used for higher voltages testing since those are the most important results. Still even though done in quite different conditions, the several calibration results showed to be consistent with each other. But since it makes little sense to average or fit different calibration data taken in different conditions, each test setup has its own calibration.

As a matter of fact, a total of 8 different calibrations were done for a variety of reasons, for example changing the workbench were the experiment was being performed.

Table 3.2: Example of calibration data acquired during a SiC MOSFET evaluation board calibration

| $V_{DS} \times 2$ [V] | $I_s$ [A] | $P$ [W] | $T_{HS}$ [℃] | $T_{S1}$ [℃] | $T_{S2}$ [℃] | $T_{HS_2}$ [℃] | $T_{A_1}$ [℃] | $T_{A_2}$ [℃] |
|---|---|---|---|---|---|---|---|---|
| 0.569 | 3.62 | 2.06 | 23.7 | 24.3 | 24.4 | 23.7 | 23.1 | 23.1 |
| 0.803 | 4.97 | 3.99 | 24.3 | 25.4 | 25.5 | 24.2 | 23.1 | 23.0 |
| 1.160 | 7.15 | 8.24 | 25.4 | 27.3 | 27.4 | 2.54 | 22.8 | 22.9 |
| 1.550 | 8.90 | 13.8 | 27.3 | 32.0 | 31.9 | 27.2 | 23.1 | 23.2 |
| 2.200 | 12.0 | 26.3 | 31.4 | 36.5 | 36.8 | 31.2 | 23.4 | 23.1 |
| 2.940 | 14.5 | 42.7 | 36.9 | 49.5 | 49.5 | 36.8 | 22.8 | 23.0 |
| 3.830 | 17.0 | 65.1 | 44.6 | 62.0 | 62.0 | 43.9 | 22.9 | 22.9 |

An example of the acquired calibration data can be seen in table 3.2, where $V_{DS} \times 2$ is the acquired voltage across both devices, $I_s$ is the current across the semiconductors, $T_{HS}$ is the temperature of the heatsink measured with the thermal camera, $T_{S1}$ is the temperature of the upper transistor measured with the thermal camera, $T_{S2}$ is the temperature of the bottom transistor measured with the thermal camera, $T_{HS_2}$ is the heatsink temperature measured with the thermocouple, and $T_{A_1}$ and $T_{A_2}$ are the ambient temperatures measured with the thermal camera and the thermocouple, respectively.

### 3.2.1 GaN HEMT Calibration Results

One of the main results obtained from calibration was the variation of the GaN channel resistance with temperature, that can be seen in Figure 3.9. The high quality surfaces used in the manufacturing of

GaN devices provides a positive temperature coefficient for all operating temperature range (since there is little to none impurity ionization). Even though this is a good characteristic in order to parallel connect devices, the temperature dependence is quite high, meaning that losses will increase substantially with temperature rise.

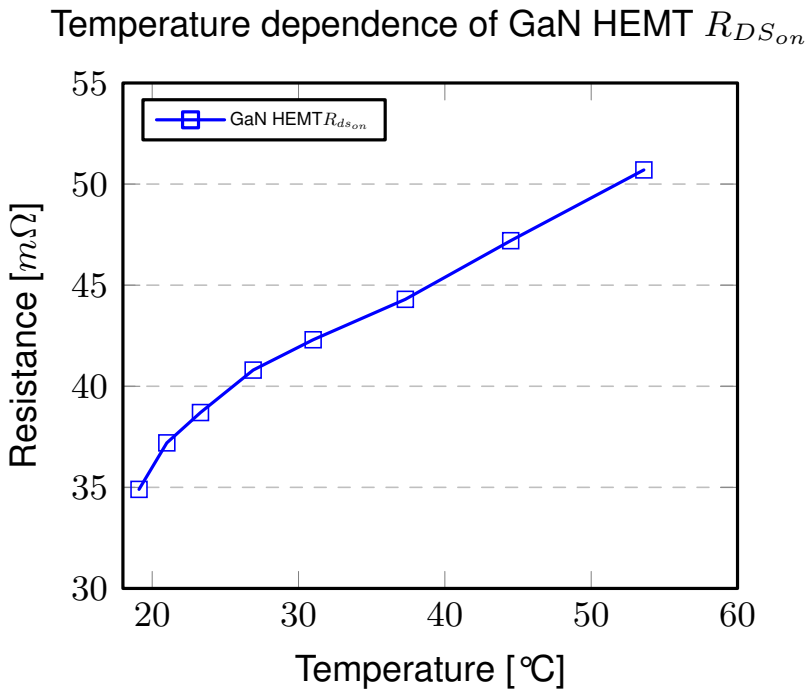



Figure 3.9: GaN HEMT Channel Resistance variation with temperature

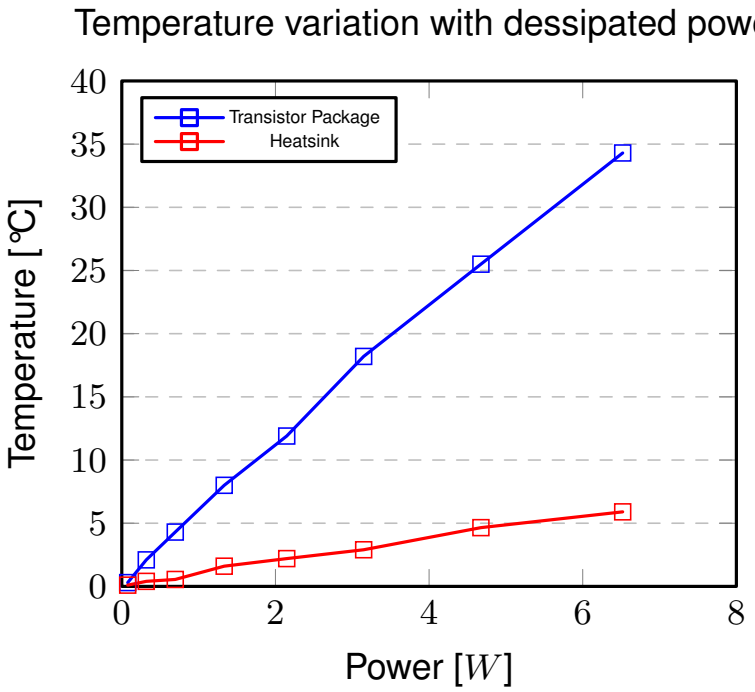



Figure 3.10: GaN HEMT Evaluation Board temperature to dissipated power

Looking at Figure 3.10, it is possible to see that the obtained temperatures for the heat sink and the transistor case increase almost linearly with the dissipated power, given the power range and temperatures considered. It is also important to note that there is a considerable difference between the temperature rise at the transistor case and at the heatsink. This indicates that the thermal resistance between the two is quite relevant. It indeed makes sense, since the transistor is bottom cooled using the land pads on the PCB, meaning that the PCB itself is part of the thermal path and as such increasing thermal resistance. GaN Systems also presents devices that are top cooled but such devices were not available to be used during the development of this thesis, and for that reason they were not tested.

### 3.2.2 SiC Calibration Results

In a similar manner to the GaN HEMT calibration, the channel resistance of the SiC MOSFET was also measured for different temperatures.

On Figure 3.11, it is possible to see that there is some negative temperature coefficient behavior, followed by a dominance of the positive temperature coefficient behavior. At higher temperatures the increase in channel resistance is also quite relevant more so than the GaN HEMT. Still these devices were tested under a considerably higher current, since the thermal conductivity allows to dissipate a considerably higher amount of power than the GaN HEMT, and the mounted heatsink of the SiC evaluation board is also considerably bigger. This means that other resistances beyond the channel resistance are more relevant here (PCB trace resistance and component legs).

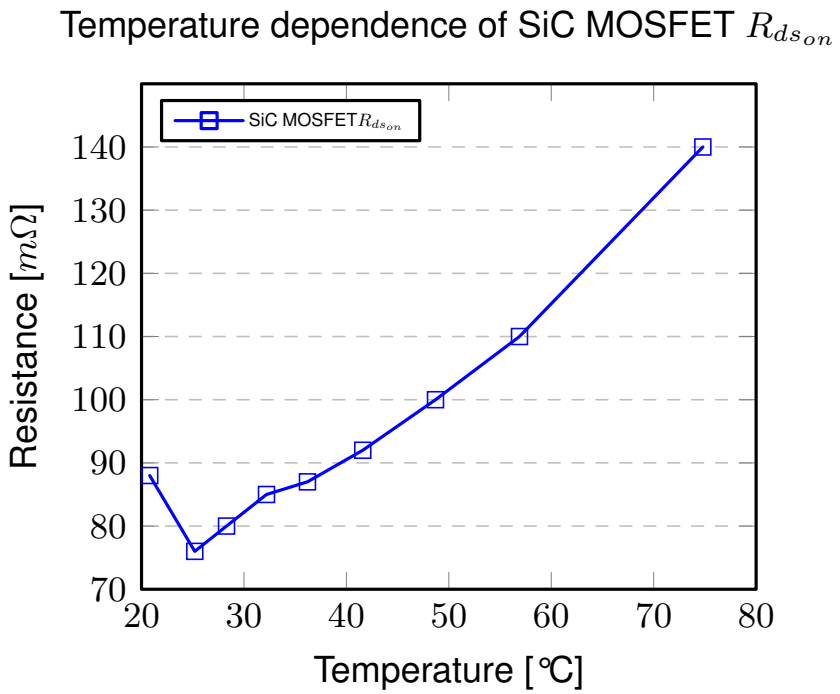



Figure 3.11: SiC MOSFET Channel Resistance variation with temperature

The obtained results for the temperature variation with the dissipated power can be seen in Figure 3.12, also reveling a near linear increase of temperature with dissipated power. It is important to note that

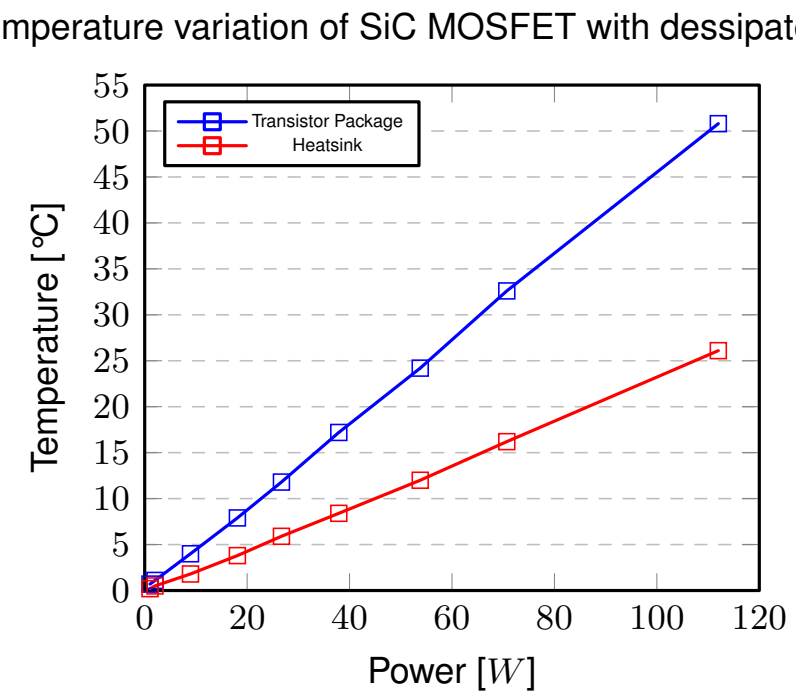



Figure 3.12: SiC MOSFET Channel Resistance variation with temperature

the difference between the heatsink temperature and the transistor case is lower than the one in GaN HEMT evaluation board, reveling a better thermal conductivity from the transistor case to the heatsink. Since, as shown in section 1.2.4, the thermal conductivity of SiC is considerably higher than the one of GaN, the temperature difference from junction to case is lower for the SiC device, which gives more confidence to work at higher heatsink temperatures, making the process of heat extraction from the devices much easier.

## 3.3 Test Results

In this section the test results are shown and discussed. The experiments performed on these devices were probably the most time consuming process throughout the development of this thesis. It has to be pointed out that the obtained data is the result of countless adjustments made to the experiment setup that together with more than 150 hours of actual experiment runtime, resulted in good and consistent data.

An important added value of the results obtained when comparing to those supplied by the manufactures is that the presented results provide all the losses as a function of the RMS value of the output sinusoidal current. This means that average values of the losses for each conditions in inverter operation are obtained.

### 3.3.1 GaN Test Results

The GaN evaluation board was tested with voltages ranging from 80 V to 300 V. The results here presented are for both 80 V and 300 V DC link voltage.

The load represented by $R_{load}$ in Figure 3.5 was varied in order to obtain different sinusoidal output currents, a modulator implemented in a dsPIC33EP256MU806[35] microcontroller was set to create an output current wave with 50 Hz frequency and a modulation index of 0.85. Since one of the main goals is to estimate switching losses at sinusoidal currents output, a total of 4 test setups were done to provide the final results:

- 80 V DC link with a switching frequency of 20 kHz;
- 80 V DC link with a switching frequency of 80 kHz;
- 300 V DC link with a switching frequency of 20 kHz;
- 300 V DC link with a switching frequency of 80 kHz.

For each of these test setups the load resistance is changed in order to create different RMS values of output currents under which measurements are made. The conduction losses are estimated using the RMS current and temperature measurements and making use of $R_{DS_{on}}$ calibration with temperature.

The switching losses are then estimated by subtracting the total dissipated power of the system, which is estimated from the temperature to power calibration, to the estimated dissipated power associated with the conduction losses.

The estimated losses in function of current can be seen in Figure 3.13, where the losses are depicted in function of the RMS current on the load. As expected, the relevance of the switching power losses increases with the switching frequency and with current. Not so obvious is the fact that the switching losses from the 80 V to the 300 V experiments did not increase proporcionaly to the voltage. This is due to the fact that the parasitic capacitances that dominate the switching losses vary in a non linear way with the voltage, being higher at lower voltages. This means that in one hand the losses increase due to the increased voltage, and therefore the increased charged energy of the parasitic capacitances but on the other hand there is a loss decreasing contribution resulting from the decrease of the parasitic capacitances values. Such phenomenon can be observed in Figure 3.14, where the behavior of the input, output and reverse capacitances ($C_{iss}$,$C_{oss}$,$C_{rss}$) are plotted against the voltage across the device.

A note should be made to the 300 V 80 kHz experiment, Figure 3.13d, where for a considerable current range the switching losses are actually more relevant than the conduction losses.

From this point the switching energies were estimated. Unfortunately, using this method it is not possible to separate the turn-on from the turn-off energies. The switching energies were calculated from the previous switching power estimation and were done for both 20 kHz and 80 kHz experiments. These results also serve as a control test, given that results from both should be quite similar since the switching energy should not depend on the frequency, it does however depend on the temperature which is different for a given current between the experiments at the two frequencies since higher frequencies result in higher losses, and therefore higher temperatures. Still this effect should be very little and

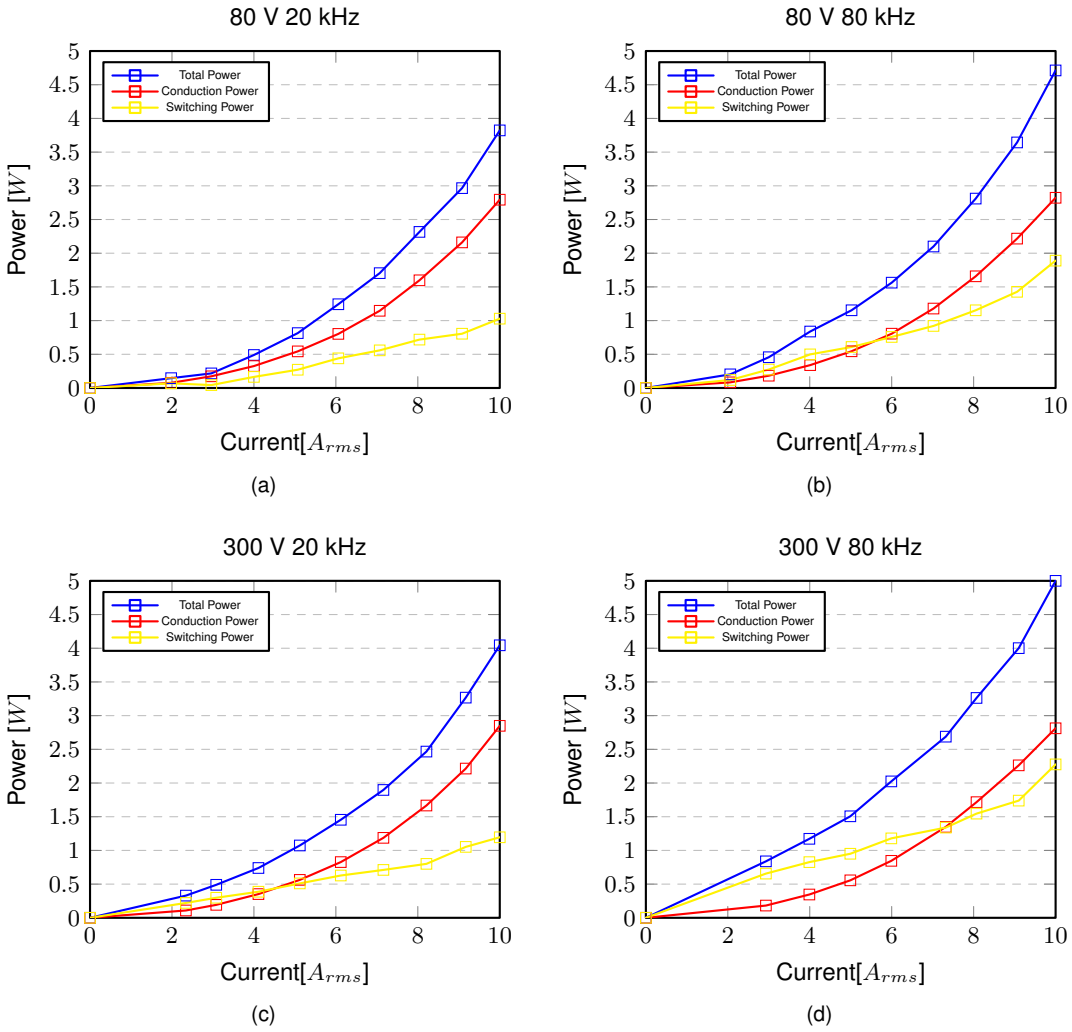



Figure 3.13: Total, conduction and switching dissipated powers

unlikely to be distinguishable from noise given the measurement equipment used. Nevertheless more investigation should be done, but to do so an external mean of controlling the temperature should be used. The calculated energies can be seen in Figure 3.15.

The obtained results for the switching energies not only are concordant to each other, but they also fall within the specified range of $E_{on} + E_{off}$ provided in the manufacturer's datasheet [36]. Just as a side note, values from manufacturer datasheet, namely switching energies, should be taken with a grain of salt since they are acquired in close to ideal unrealistic conditions, for example using extremely complex current controlled gate drivers, that favor such device in the market.

The resulting experiments outputted a total conduction and switching losses that vary with the output load power. These results are extremely important in order to design a heatsink that best fits the needs of the team, as far as integration with the rest of the car goes. Since the car varies from year to year a methodology like this would allow to better understand the losses involved and design a better overall car. This topic will be further discussed in section 3.7.

An example of the acquired data during one of the experiments can be seen in table 3.3, where $V_{DC}$ is the input DC link voltage, $I_{DC}$ is the DC link current, $I_{load_{rms}}$ is the RMS current at the load, $f_{sw}$

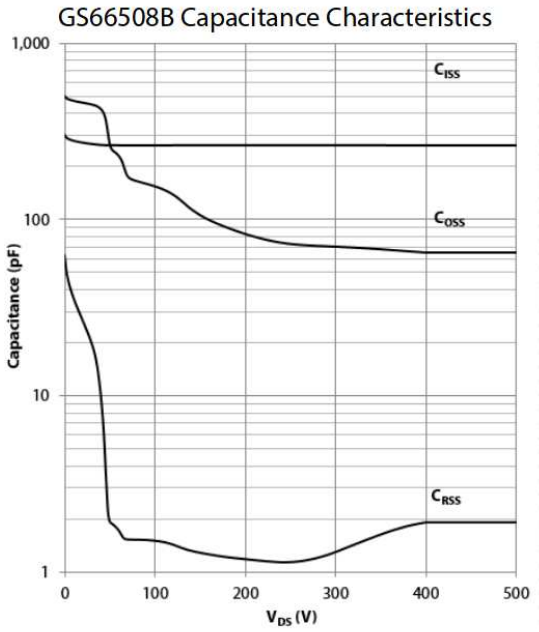



Figure 3.14: Typical $Ciss$, $Coss$ and $C_{rss}$ vs $V_{ds}$, courtesy of GaN Systems

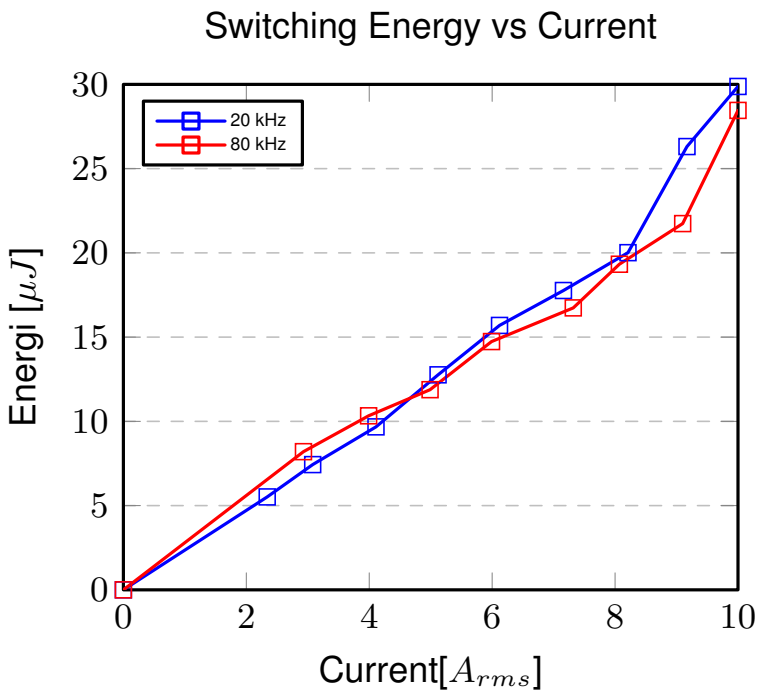



Figure 3.15: Switching Energy vs Current

and $f_{out}$ are the switching and output current wave frequencies, respectively, $T_{S_1}$ is the temperature of the bottom semiconductor measured with the thermal camera, $T_{HS_1}$ and $T_{HS_2}$ are temperatures of the heatsink measured with the thermal camera and the thermocouple, respectively, and finally $T_{A_1}$ and $T_{A_2}$ are the ambient temperatures measured with the thermal camera and the thermocouple, respectively.

Table 3.3: Example of acquired data for GaN HEMT evaluation board experiment

| $V_{DC}$ [V] | $I_{DC}$ [A] | $I_{load_{rms}}$ [$A_{rms}$] | $f_{sw}$ [kHz] | $f_{Out}$ [Hz] | $T_{S_1}$ [℃] | $T_{HS_1}$ [℃] | $T_{HS_2}$ [℃] | $T_{A_1}$ [℃] | $T_{A_2}$ [℃] |
|---|---|---|---|---|---|---|---|---|---|
| 300.2 | 2.35 | 2.34 | 20 | 50 | 22.1 | 19.1 | 19.2 | 18.6 | 18.6 |
| 300.5 | 2.63 | 3.08 | 20 | 50 | 23.9 | 19.2 | 19.5 | 18.7 | 18.7 |
| 300.2 | 2.98 | 4.11 | 20 | 50 | 26.7 | 20.2 | 20.5 | 18.8 | 18.9 |
| 300.9 | 3.31 | 5.12 | 20 | 50 | 30.0 | 21.1 | 21.2 | 18.6 | 18.6 |
| 300.5 | 3.72 | 6.12 | 20 | 50 | 34.2 | 22.0 | 22.0 | 18.7 | 18.8 |
| 300.0 | 4.05 | 7.16 | 20 | 50 | 38.6 | 22.8 | 22.7 | 18.5 | 18.4 |
| 300.5 | 4.44 | 8.21 | 20 | 50 | 45.1 | 24.0 | 24.0 | 18.9 | 18.9 |
| 300.7 | 4.70 | 9.17 | 20 | 50 | 53.6 | 25.1 | 25.1 | 18.9 | 18.9 |
| 300.8 | 4.99 | 10.2 | 20 | 50 | 62.0 | 26.6 | 26.5 | 19.1 | 19.0 |

### 3.3.2 SiC Test Results

The SiC evaluation board was tested with voltages ranging from 80 V to 600 V.

During the testing of SiC MOSFET devices, using DC link voltages of around 80 V revealed to be too little to actually estimate switching losses due to highly non linear behavior of the parasitic capacitance at that lower voltages. Therefore the most prominent results were obtained for the following setups:

- 300 V DC link with a switching frequency of 20 kHz;
- 300 V DC link with a switching frequency of 80 kHz;
- 600 V DC link with a switching frequency of 20 kHz;
- 600 V DC link with a switching frequency of 80 kHz.

The 300 V testing allows for a direct comparison to the experiments made with GaN HEMT devices and the 600 V experiment is done in similar voltage conditions to those required in a formula student inverter.

Since there was no available power supply that provided both the necessary DC voltage with the required output current, a different approach had to be undertaken. Using components available at the Laboratory a variable voltage power supply that could reach voltages up to 720 V and an output current of up to 10 Ampere was built. A simplified schematic of the experiment setup can be found in Figure 3.16 and the resulting laboratory apparattus can be seen in Figure 3.17.

This way it was possible to test the inverter leg in a voltage equivalent to the maximum voltage allowed by formula student regulations [37] of 600 V.

Figure 3.19 shows the total losses power and the respective contribution of the conduction and the switching losses for the four setups described above, 300 V at 20 kHz, 300 V 80 kHz, 600 V 20 kHz and 600 V 80 kHz in Figures 3.19a, 3.19b, 3.19c and 3.19d respectively. This data reveals that as it was expected the switching losses are much more relevant for the SiC Device than for the GaN Device. Still the superior thermal conductivity of SiC allows to reach much higher currents.

Even though results are within the expected range, it is important to note that this experiment was much more susceptible to electromagnetic interference due to the self design power supply that would

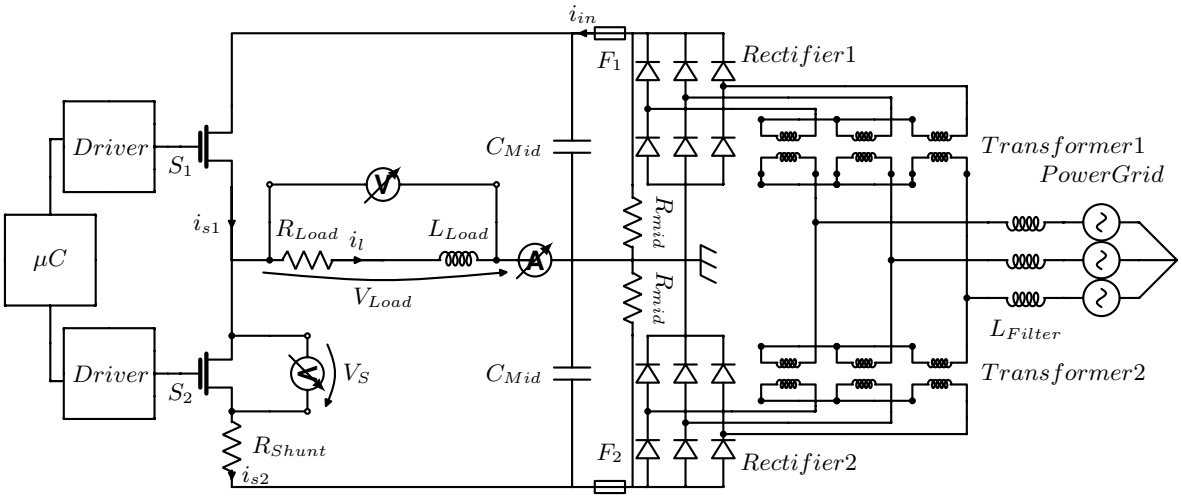



Figure 3.16: Half Bridge Inverter topology with on laboratory built power supply

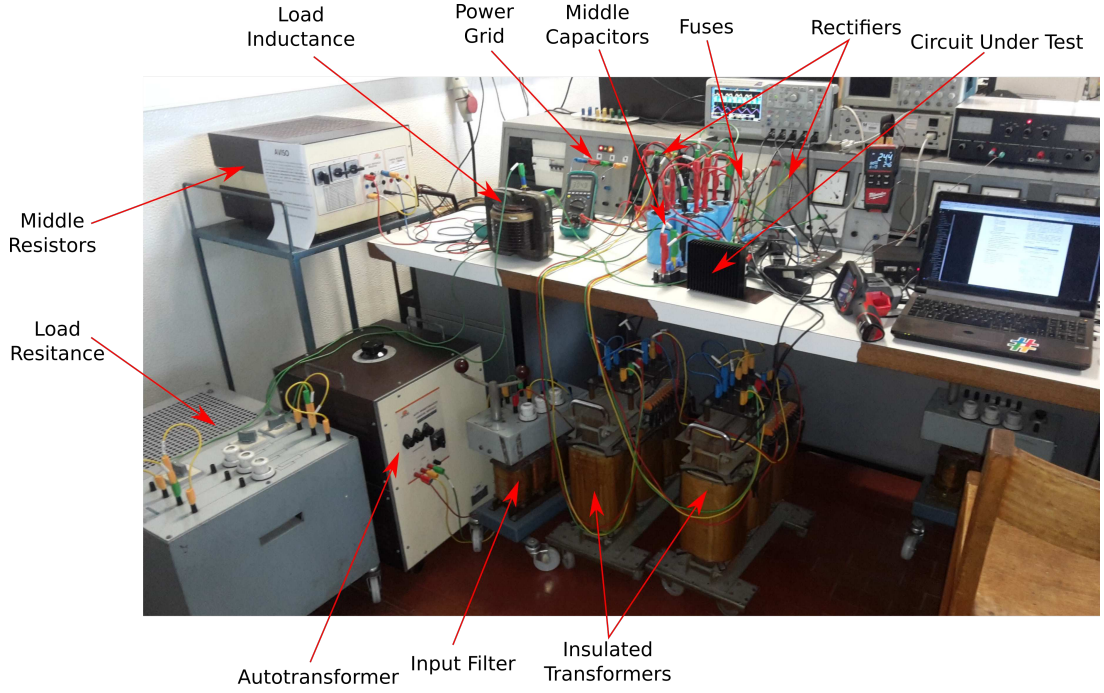



Figure 3.17: Experimental setup with on laboratory built power supply

cause some measurements error. Those undesirable effects were minimized while still bounded with the available equipment.

In Figures 3.20a and 3.20b one can see the switching energies, $E_{on} + E_{off}$, for 300 V and 600 V, respectively. Here it is possible to verify that the losses approximately doubled when doubling the voltage, which makes sense since input, output and reverse transfer capacities are stable from 200 V and above.

Secure operating conditions were always ensured with respect to over voltages and over currents. An example of the turn on and the turn off behavior can be seen in Figure 3.18, where the blue line is the DC link voltage in a 200 V per division scale, the yellow line is the DC link voltage ripple in a 4 V per division scale, the green line is the DC link current at 2 Ampere per division scale and the pink line is the

current at the load at a 10 Ampere per division scale.

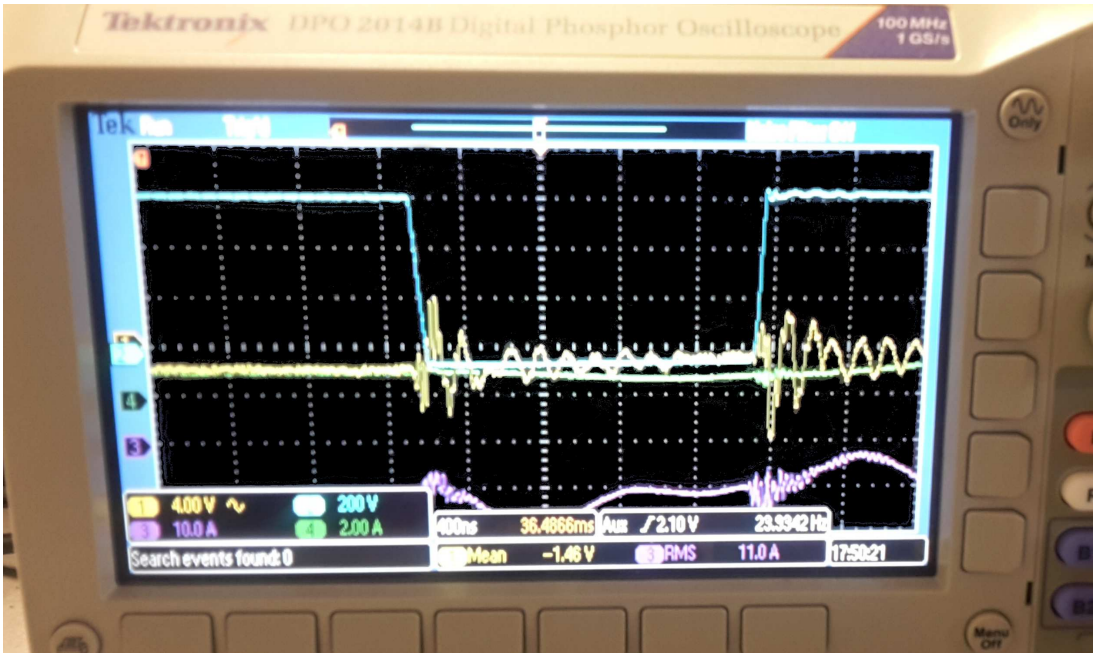



Figure 3.18: Turn on and turn off under 600 V DC link Voltage

Given that the dissipated power is obtained using temperature measurements, the higher thermal conductivity of the SiC evaluation module comes with one disadvantage, a loss in power measurement resolution since temperature measurement is limited by the resolution of the measurement device (0.1 ° C).

An example of the acquired data during the SiC MOSFET evaluation board experiments can be seen in table 3.4.

Table 3.4: Example of data acquired during SiC MOSFET evaluation board experiments

| $V_{DC}$ [V] | $I_{DC}$ [A] | $I_{load_{rms}}$ [$A_{rms}$] | $f_{sw}$ [kHz] | $f_{Out}$ [Hz] | $T_{HS_1}$ [℃] | $T_{S1}$ [℃] | $T_{S2}$ [℃] | $T_{HS_2}$ [℃] | $T_{A_1}$ [℃] | $T_{A_2}$ [℃] |
|---|---|---|---|---|---|---|---|---|---|---|
| 300 | 1.04 | 1.81 | 80 | 50 | 25.8 | 27.2 | 27.4 | 25.5 | 23.0 | 22.8 |
| 302 | 1.64 | 3.37 | 80 | 50 | 26.8 | 28.7 | 29.5 | 26.2 | 23.2 | 23.6 |
| 301 | 2.32 | 5.35 | 80 | 50 | 27.7 | 31.6 | 31.6 | 27.5 | 23.4 | 23.5 |
| 302 | 3.03 | 7.60 | 80 | 50 | 29.0 | 32.6 | 32.6 | 28.7 | 23.6 | 23.5 |
| 302 | 3.59 | 9.52 | 80 | 50 | 30.9 | 35.6 | 36.4 | 29.4 | 23.4 | 23.7 |
| 301 | 3.93 | 10.7 | 80 | 50 | 31.4 | 38.3 | 38.1 | 30.1 | 23.5 | 23.2 |

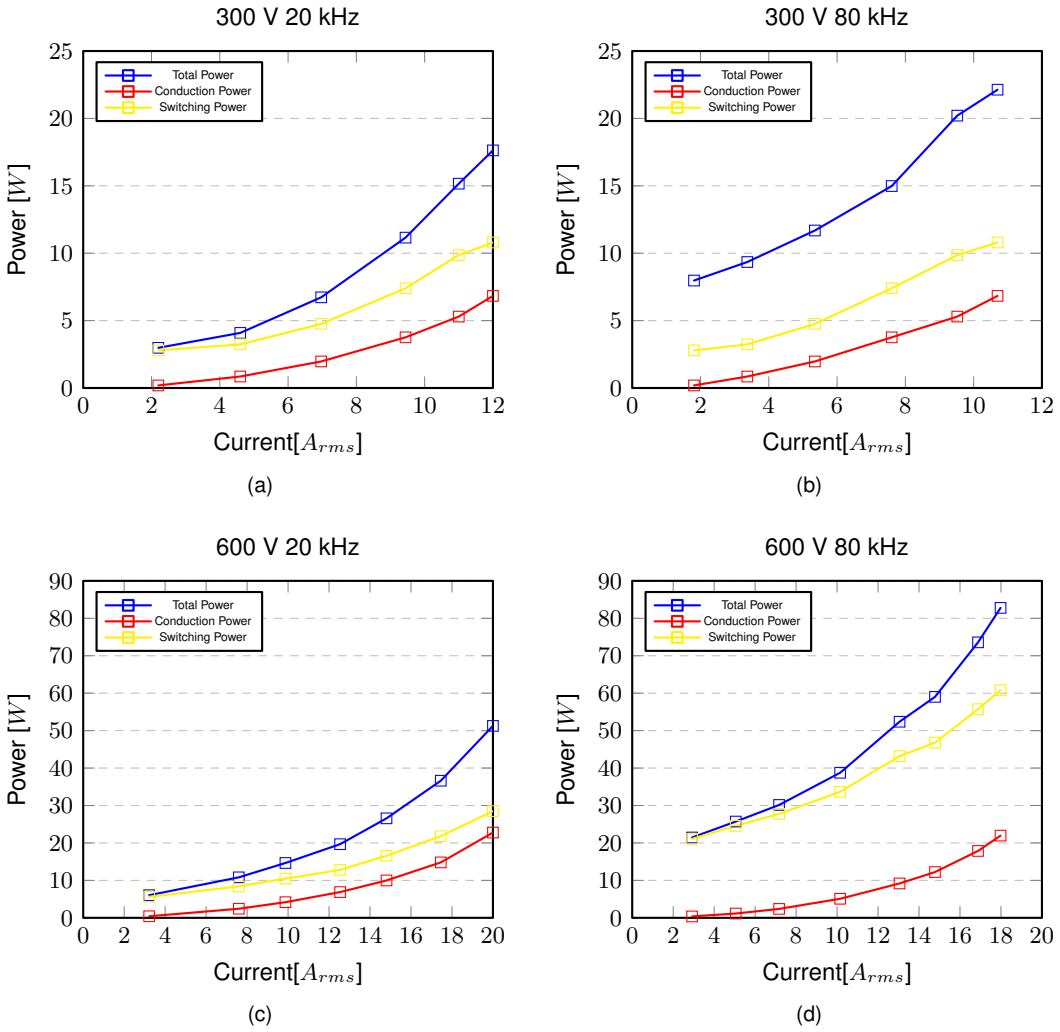



Figure 3.19: Total, conduction and switching dissipated powers

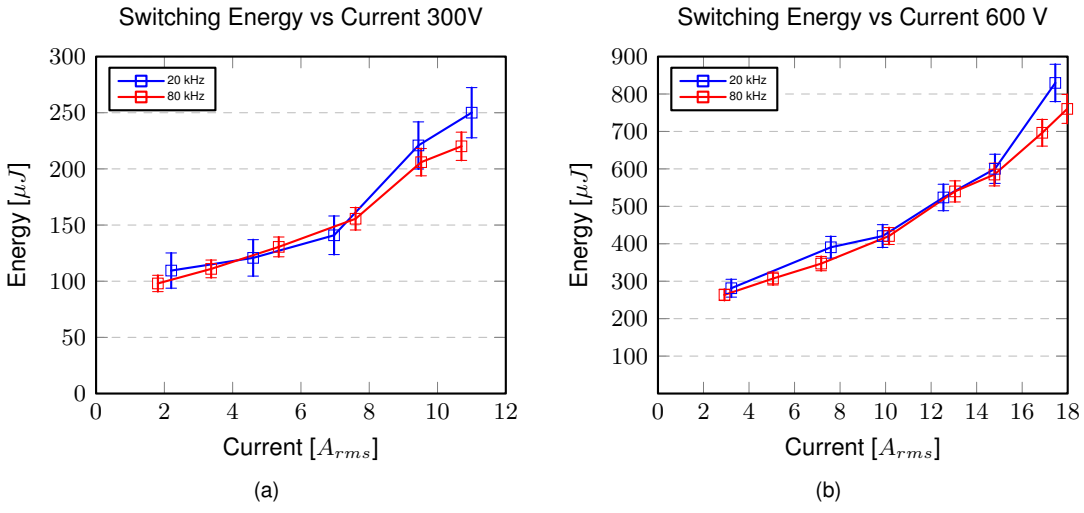



Figure 3.20: Switching Energies against output current for SiC MOSFET

## 3.4 Error analysis

Since the acquired results are obtained by the process of measurements in an experimental setup it is important to evaluate the uncertainty associated with the obtained results. During the experiments one important parameter to obtain was the dissipated power. Such power was obtained by the measurement of the system temperature in thermal equilibrium. This temperature to power relation on the other hand was obtained by means of calibration, as explained in detail in section 3.1.

On the calibration process, power measurement was done by using a current probe and voltmeter, which specifications have been presented in section 3.1.

The power is obviously obtained by the multiplication of the measured voltages and currents:

$$P = V \cdot I \tag{3.2}$$

and if the uncertainty of voltage and current measurements are $\delta V$ and $\delta I$ then the fractional uncertainty of the power measurement is given by:

$$\frac{\delta P}{|P|} = \sqrt{\left(\frac{\delta V}{|V|}\right)^2 + \left(\frac{\delta I}{|I|}\right)^2} \tag{3.3}$$

The uncertainty for both current and voltage meter devices are specified as a percentage of the reading value plus a number of digits. For the voltmeter this yields:

$$\delta V = 0.3\,\%rdg + 2\,dgt \tag{3.4}$$

and for the ampmeter:

$$\delta I = 2\,\%rdg + 10\,dgt \tag{3.5}$$

This errors are calculated for both the SiC MOSFET experiments as well as the GaN HEMT experiments, since for each case several measurements for one calibration are made the mean error of the power measurements are considered. This yields a fractional uncertainty of 2.60% and 2.25% for the GaN HEMT and SiC MOSFET calibrations, respectively.

Both calibration and experiments temperature measurements were made in the exact same spots and with the same equipment. Therefore the accuracy of the temperature meter is not considered since by simplicity it is assumed that the error due to accuracy of the device stays constant over measurements of the same quantities. Still the resolution of the temperature measurement must be considered.

Using only the resolution of the temperature measurement devices the uncertainty of the experiment temperature measurement, $\delta T$, is 0.1 °C.

Since the power is obtained by dividing the temperature by the temperature to power relation, then the combined fractional uncertainty for the power measurement of the experiments is:

$$\frac{\delta P'}{|P'|} = \sqrt{\left(\frac{\delta T}{|T|}\right)^2 + \left(\frac{\delta C_{T-P}}{|C_{T-P}|}\right)^2} \tag{3.6}$$

Where $C_{T-P}$ is the calibration value obtained in calibration, $T$ is the measured temperature in the experiment setup and $P'$ is the estimated power dissipated in thermal equilibrium.

This yields a maximum fractional uncertainty of the power estimation of 2.65% and 2.3% for the GaN HEMT and SIC MOSFET, respectively.

## 3.5 Verification and Validation

Both manufacturers, GaN Systems and Wolfspeed, provide LTSice[38] models for their semiconductors.

Using the LTSpice[38] models from the manufacturers, a LTSpice[38] model was made to recreate the test conditions, as well as the parasitic elements present. It is actually quite important to modulate the parasitic elements since it is crucial to minimize discontinuities that would otherwise cause numerical instabilities under really small time steps, remembering that the selected time steps must be able to capture the switching behavior of the transistors. Such a schematic for the GaN device can be seen in Figure 3.21. A similar model for the SiC devices was also made.

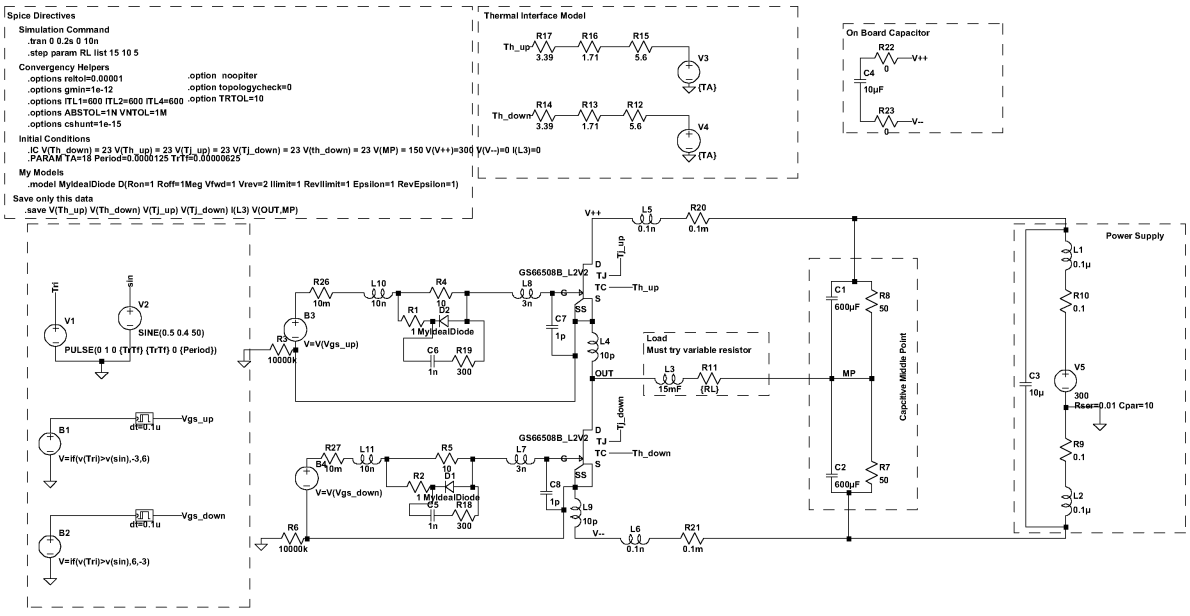
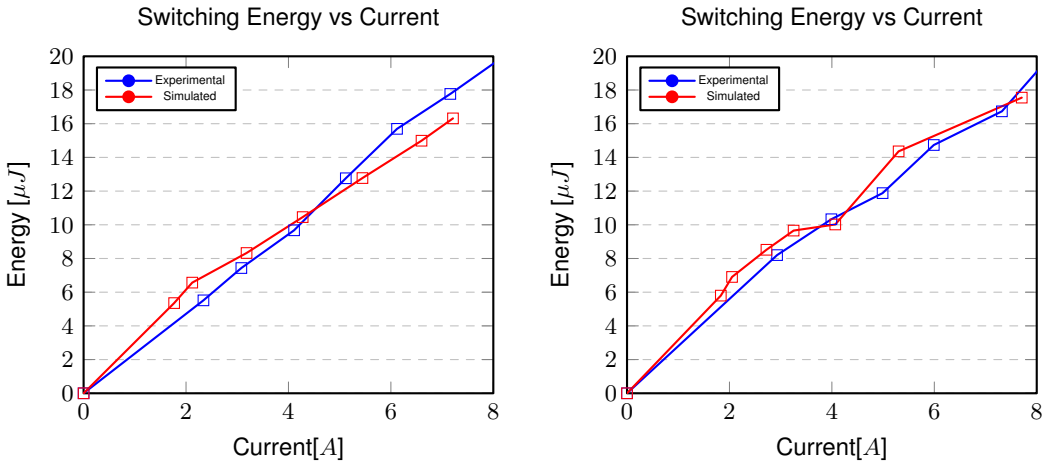



Figure 3.21: Spice schematic representing the GaN Evaluation Board

These models are computationally heavy since the losses are calculated under actual operating conditions, and therefore thermal equilibrium is required to obtain the results. To speed up simulations, the thermal capacitance of all elements after the case was removed. The most important results of the simulation lie with the switching losses that are by far the hardest to estimate.

Figure 3.22 compares the experimental and simulated data for Swithing Energy versus Current for the GaN HEMT evaluation board from GaN Systems. The obtained results from the simulation correlate rather well with the experimental results providing extra confidence to use the LTSpice models supplied by GaN Systems.



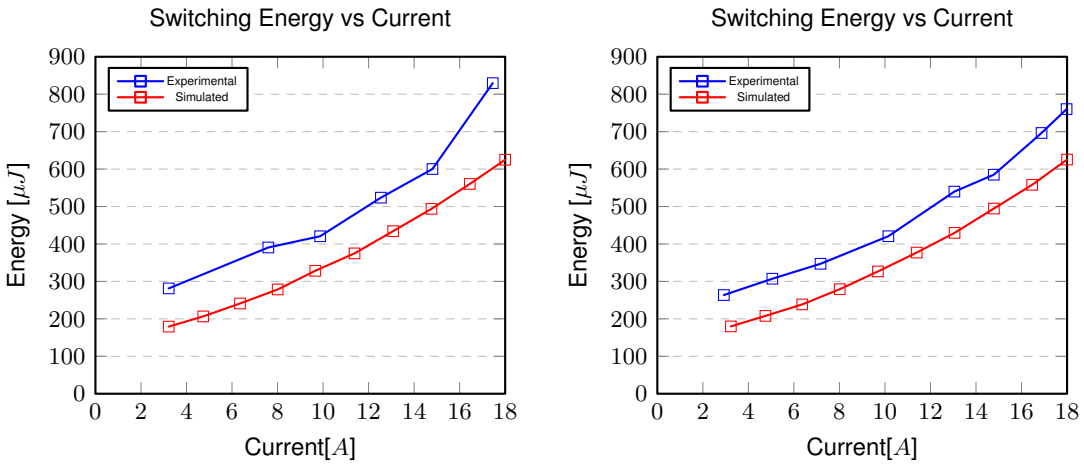

(a) Switching Energies at 20 kHz

(b) Switching Energies at 80 kHz

Figure 3.22: Simulated vs Experimental GaN HEMT Switching Losses Measurement

Figure 3.23 compares the experimental and simulated data for Switching Enery versus current for the SiC MOSFET evaluation board from Wolfspeed. Unlike the results obtained for the GaN HEMT simulations, these appear to be more optimistic as far as switching losses is concerned.

To further investigate those differences, a LTSpice model implementing the double pulse test as represented in Figure 3.2 was made. After some tests it was observed that the switching losses of the device model were practically insensitive to temperature variations, and that might explain the observed difference. Still bounded by time and not to compromise the rest of the objectives of this thesis, this issue was not further investigated given the high amount simulation time needed for the model to run.




(a) Switching Energies at 20 kHz

(b) Switching Energies at 80 kHz

Figure 3.23: Simulated vs Experimental SiC MOSFET Switching Losses Measurement

## 3.6 Experimental Conclusions

With the experiments performed it was possible to compare the losses behavior of two of the most prominent semiconductor technologies for future generation power converters. Special remarks in different aspects must be given to each of the technologies. The GaN HEMT devices provide incredible low switching losses with the down side of poor thermal conductivity that generates a new set of challenges. The SiC MOSFET provides an extremely attractive thermal conductivity that eases the process of heat management while also providing considerable less switching losses when compared to the Silicon IGBT devices.

The experimental results yield an interesting set of information that allows better estimate losses in actual dynamic conditions close to those found in a inverter operating in a formula student car. This is further developed in the next section.

As stated before, the SiC MOSFET devices also offer attractive gate driver requirements using a wide voltage band (around 25 V) and the ability to use a negative voltage that combined provides good noise immunity that reduces the likelihood of a non intentional turn on of the device. This combined with the higher breakdown voltage and better thermal conductivity when compared to the GaN HEMT devices makes them the most suitable device to use in the first generation of a self made inverter.

Still the GAN HEMT devices should not be looked out since the development technology of those devices is increasing rapidly, and the advantages of different topologies for motor control should be further investigated to be able to quantify the performance increase by the use of an open winding motor for example.

## 3.7 Dynamic Model for Loss Analysis

As mentioned before the FST team would greatly benefit from a better way to estimate the inverter losses in real racing conditions. As of this day the team is using parameters supplied by the manufacturers that are far from good approximations of real operating conditions, such as for example maximum losses (this is typically the only value supplied by a considerable number of manufactures). This impacts the development of the cooling devices of the car from the cooling plate to the radiator design, meaning that a better losses estimation will lead to a better design of the overall cooling system design.

During the development of this thesis a more in depth understanding of the losses involved in the inverter operation was investigated. By using the data of either the performed experiments or the simulations it is possible to create a model that predicts the instantaneous losses of the inverter for each point in time.

The vehicle dynamics department of the FST team already modulates the vehicle behavior across a race track using Simulink[39], which is a tool from Mathworks that allows to analyze multi-domain dynamical system. Therefore, on this thesis, a simulink model for the semiconductor losses is developed. The general idea behind such model is that with a well defined test method, such as the one presented, one can for any given device retrieve the necessary data to feed the model.

Basically the model is divided into two blocks, one regarding loss calculation ($E_{on}$,$E_{off}$ and conduction losses) and a second one regarding the thermal model of the device. The loss calculation is achieved with look up tables, where the switching energies and channel resistances are available for the different operating conditions. The thermal model is basically the implementation of the manufacturers Cauer model refered in section 2.6.

The model makes use of Simscape for the electrical quantities and Simulink for power loss calculations. The top level of that model can be seen in Figure 3.24. The model on the figure is for GaN HEMT and the difference for SiC MOSFET is only the activation of the reverse diode block by changing the data tables used.

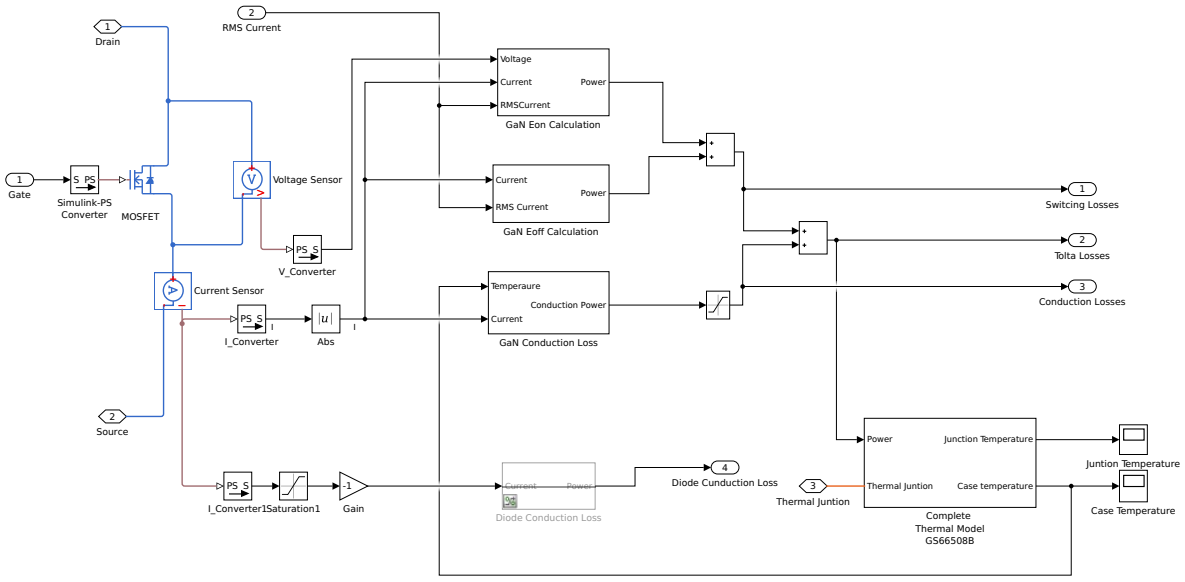



Figure 3.24: Simulink model for the GaN HEMT

### 3.7.1 Temperature Dependent Models

After having a model that estimates the junction temperature of the devices, obtained by making use of the Cauer networks provided by the manufactures, it is possible to feedback that information into the electrical model. This way it is possible to design a Simulink model where the semiconductors parameters vary with temperature.

The variation of these parameters was first modeled according to the plots provided by the manufacturers. A software[40] was used to automatically extract data points from the plot images from the

datasheet. On a second approach the experimental data obtained was used to feed the model. Using Matlab, the points were organized in a matrix format that are passed to Simulink. Whith this approach future teams can use the testing procedures detailed in previous chapters to obtain the necessary information to feed the model, or simply use the manufacturers data if such infomation is available (that is not always case).

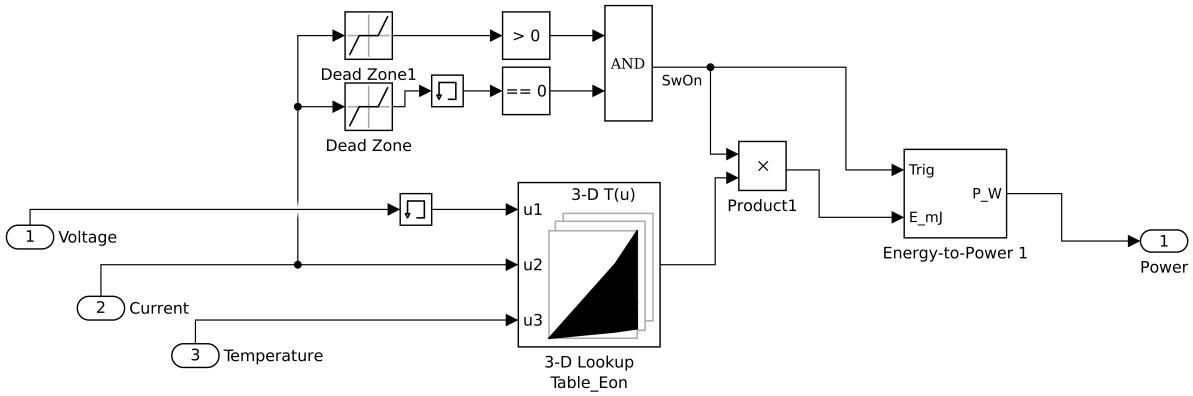



Figure 3.25: Simulink subsystem for $E_{on}$ calculation

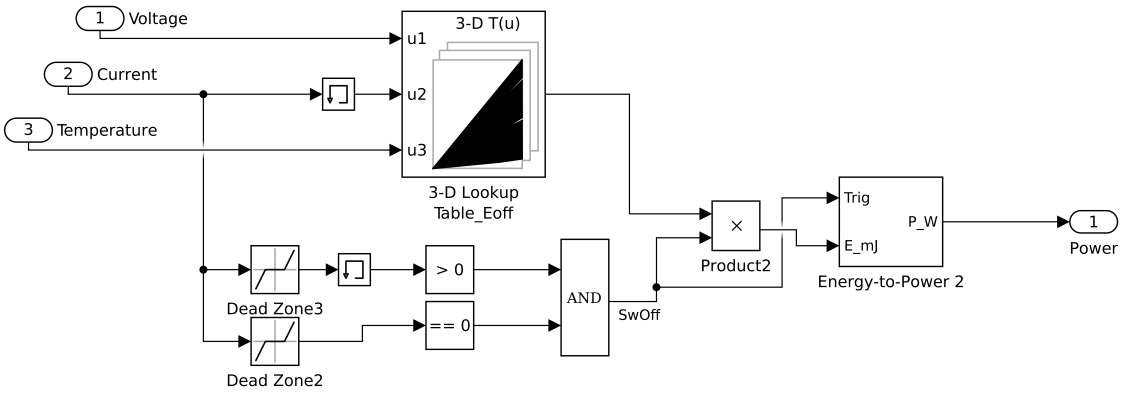



Figure 3.26: Simulink subsystem for $E_{off}$ calculation

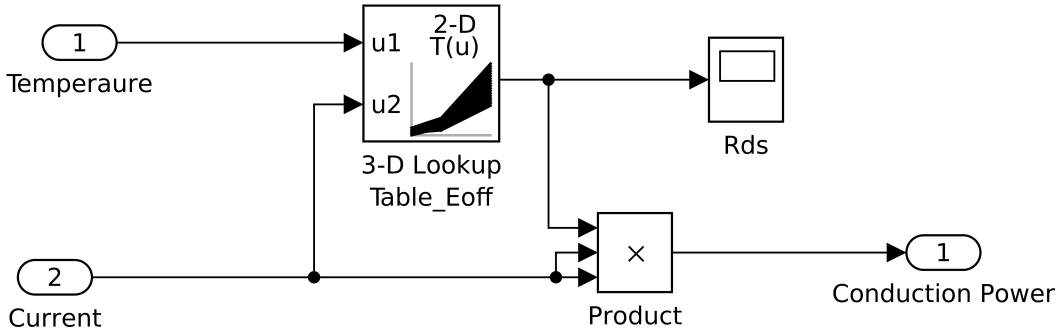



Figure 3.27: Simulink subsystem for $R_{DS_{on}}$ calculation

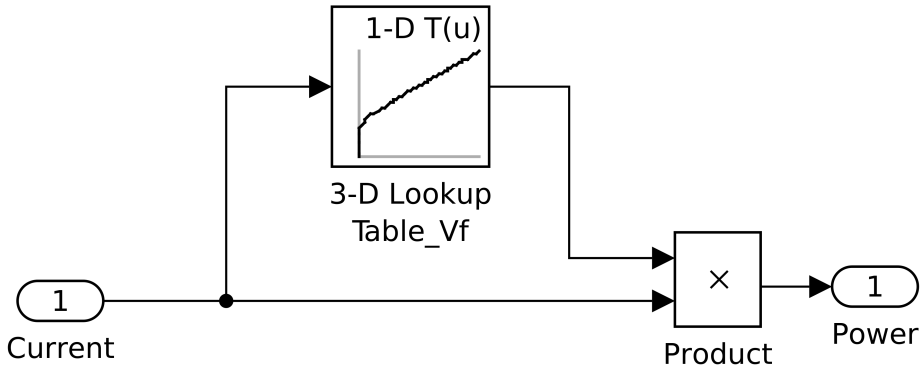



Figure 3.28: Simulink subsystem for diode forward voltage, $V_f$, calculation

Such data will then be used in simulink subsystems represented in Figures 3.25, 3.26, 3.27 and 3.28, allowing to dynamically calculate the losses of the inverter and aid the design of the cooling department of the team.

The parameters that vary with temperature are $R_{DS_{on}}$, $E_{on}$ and $E_{off}$. Since the experimental data does not distinguish the $E_{on}$ from the $E_{off}$ energies, an estimated division of the contribution of each one to the total switching energies must be assumed, for example typical ratios for the device type.

For the Schottky Diode only the forward voltage is modeled with temperature dependence.

The designed Simulink subsystems are in Figures 3.25, 3.26 and 3.27, for the turn on energy, turn of energy and on state resistance, respectively.

The diode forward voltage variation Simulink subsystem is in Figure 3.28.

# Chapter 4

# 3 Phase Inverter Design and Manufacturing

In this chapter the design of the prototype for 3-Phase inverter is discussed. Given the results and knowledge gained with the experiments executed to both GaN HEMT and SiC MOSFET, it was decided to use SiC MOSFET for several reasons: The ability to have more dissipated power in SiC MOSFET; The lower cost of the overall semiconductors (GaN HEMTs are more expensive and to fulfill the required specifications at least the double of transistors would be necessary); Easier gate driving requirements and better EMI immunity given the ability to drive the transistor with a negative voltage; Easier packaging when compared to GaN HEMT that are surface mount components implying an heatsink design that would be dependent of the circuit board layers and layout, adding an extra degree of complexity.

Having select SiC MOSFET as the switching element a market analysis was made to find the transistors available in the market and compare their properties (note that since the beginning of this analysis more solutions) have reached market given the enormous expansion of the SiC MOSFET market[41, 42]).

An overview of the design for the main elements of the inverter is also discussed. The schematics and drawings of all the inverter parts can be found in appendix A and appendix C.

## 4.1 Semiconductor Selection

To find a collection of SiC Devices that would perform in the desired situation, the major commercially available distributors catalogs were consulted.

Three companies presented discrete solutions that could fit the application:

- CREE - Wolfspeed
- ROHM Semiconductor
- STMicroelectronics

Still non-discrete solutions should also be taken into account, in particular power modules that already pack 6 SiC MOSFET devices as well as 6 SiC Schottky Diodes and their internal connections for a 3-phase inverter. For this type of other manufacturers appear with solutions:

- Microsemi
- CREE - Wolfspeed
- Semikron

Complete packed power modules provide two main advantages when compared to discrete solutions: a typically lower on state resistance; and a lower thermal impedance from the junctions to the case. This is obviously related to the package itself since the discrete transistors are packed in a TO-247 (a standard semiconductor packaging), while dedicated power modules use different approaches that allow to place the bare dies directly on top of a heatsink with more area and better properties of those supplied by the TO-247 packages. As a drawback the price increases significantly.

Since the maximum DC link voltage used is around 600 V, only semiconductors with 1200 V breakdown voltage are considered in order to safely handle high voltage transients. 1700 V breakdown SiC MOSFET transistors are also sold, however the price increases as well as the on resistance and therefore they are not considered.

Table 4.1 lists the found discrete SiC MOSFETs with the most important parameters.

| Manufacturer | Model | $V_{DSS}$ [V] | $I_d$ [A] | Rds [mΩ] | Coss [pF] | $T_{MAX}$ [℃] | $T_{s_{ON}}$ [ns] | $T_{s_{OFF}}$ [ns] | Price [Eur] |
|---|---|---|---|---|---|---|---|---|---|
| ROHM | SCT3040KLGC11 | 1200 | 55 | 40 | 122 | 175 | 21 | 49 | 20.58 |
| ROHM | SCT3030KLGC11 | 1200 | 72 | 30 | 180 | 175 | 24 | 61 | 35.06 |
| Cree | C2M0040120D | 1200 | 60 | 40 | 150 | 150 | 14.8 | 26.4 | 29.00 |
| Cree | C2M0025120D | 1200 | 90 | 25 | 220 | 150 | 14.4 | 28.8 | 59.33 |
| ST | SCT50N120 | 1200 | 65 | 52 | 170 | 200 | | | 29.86 |
| ST | SCTWA50N120 | 1200 | 65 | 52 | 170 | 200 | | | 30.02 |

Table 4.1: Parameters of the most relevant SiC MOSFET discrete devices

Table 4.2 lists the found discrete SiC Schottky Diodes with the most important parameters.

| Manufacturer | Model | $V_{RRM}$ [V] | $V_f$ [V] | $I_f$ [A] | $I_{fsm}$ [A] | $T_{MAX}$ [℃] | Price [Eur] |
|---|---|---|---|---|---|---|---|
| Cree | C4D10120E | 1200 | 1.5 | 33 | 75 | 175 | 9.80 |
| Cree | C4D30120D | 1200 | 1.8 | 30 | 130 | 175 | 28.7 |
| Cree | C4D40120D | 1200 | 1.8 | 40 | 130 | 175 | 38.25 |
| ON Semiconductor | FFSH40120ADN_F155 | 1200 | 1.45 | 40 | 135 | 175 | 25.14 |
| ON Semiconductor | FFSH30120ADN_F155 | 1200 | 1.45 | 30 | 125 | 175 | 15.67 |
| Infineon | IDW40G120C5BFKSA1 | 1200 | 1.4 | 40 | 290 | 175 | 26.61 |
| Infineon | IDW30G120C5BFKSA1 | 1200 | 1.4 | 30 | 240 | 175 | 18.52 |
| Littelfuse | LFUSCD30120B | 1200 | 1.5 | 30 | 240 | 175 | 32.23 |
| USCi | UJ2D1230K | 1200 | 1.5 | 30 | 240 | 175 | 16.51 |
| Microsemi | MSC030SDA120B | 1200 | 1.5 | 69 | 280 | 175 | 11.61 |
| Microsemi | MSC020SDA120B | 1200 | 1.5 | 43 | 150 | 175 | 10.12 |

Table 4.2: Parameters of the most relevant SiC Schottky Diodes discrete devices

Table 4.3 lists the found complete power modules( that pack 6 SiC Schottky Diodes as well as 6 SiC MOSFETs) in a 3-Phase inverter configuration and their most important parameters.

| Manufacturer | Model | V [V] | Rds [mΩ] | Id [A] | Coss [pF] | T [℃] | Tson [ns] | Tsoff [ns] | Vf [V] | If [A] | Afsm [A] | Price [Eur] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Semikron | SKiiP 26ACM12V17 | 1200 | 23 | 79 | 274 | 175 | 52 | 88 | 1.4 | 71 | 196 | 399.75 |
| Cree | CCS050M12CM2 | 1200 | 25 | 89 | 393 | 150 | 21 | 50 | 1.5 | 50 | 90 | 386.75 |
| Microsemi | APTSM120TAM33CTPAG | 1200 | 33 | 89 | 360 | 175 | 10 | 45 | 1.5 | 30 | 60 | 517.04 |

Table 4.3: Parameters of the most relevant SiC 3 Phase Legs power modules

Selecting a discrete transistor was the first compromise, since given the context under which this inverter was designed (trying to be the first generation of inverters to be used in the formula student team) selecting a discrete transistor makes more sense by two reasons. The first one is price since the power modules are considerably more expensive and the second one is versatility given that is the first prototype mistakes can happen and if one transistor is burned the cost of recovery is significantly lower. Additionally, power modules differ for each manufacturers while discrete transistors such as TO-247-3 follow a standard that allows to test different transistors with the same design.

From this point the transistors with the lowest on resistances and therefore higher current ratings are the ones considered. This leads to the selection of the Wolfspeed C2M0025120D[20] SiC MOSFET with the increased benefit of being very similar as far as gate driving requirements and behavior to those used in the experimental measurements.

Unfortunately later in the design process due to a stockout of that device the C2M0040120D[43] also from Wolfspeed had to be selected instead, that represents a small increase in the on state resistance.

The current requirements of the diode are considerably lower since MOSFET devices can handle reverse current unlike IGBTs and for the particular case of SiC MOSFET body diode behaves with positive temperature coefficient in the forward voltage as well as the SiC Diode. The selected diode was then the Wolfspeed C4D10120E due to the lower price combined with a considerably smaller surface mount package (TO-252-2).

## 4.2 Gate Driver Design

The gate driver design is based on a reference design from Infineon Technologies using 1ED020I12-F2[44] component that was developed for single IGBT driving. This IC is used to provide a galvanic isolation between the low voltage system gate driver signal and the subsequent high voltage gate driver signal.

This signal is then used to attack a totem-pole driver that is connected to the series gate resistances. A desaturation circuit provided by the IC is also used to detect short circuits and turn off the transistors in such event.

The supply for each gate driver is individually provided by insulated DC/DC converters that generate -5 V and 20 V, which are the ideal values for gate driving the SiC transistors according to the manufacturer.

The gate driver design ensures a propagation delay lower than 140ns. This value can be further

improved using faster galvanic insulation communications methods.

The gate driver was designed in order to be possible to place up to 4 gate driver resistors allowing for different values of gate resistances to be tested with fine increments. Nevertheless calculations were done that help to provide a starting point for the gate resistor values. To do so an RLC circuit was considered, being R the gate resistance, L the parasitic inductance of the path to the gate of the device (that includes the legs of the transistor case) and C the input capacitance of the device. Finally, the gate resistance was selected in such a way that the damping ratio will equal $1/\sqrt{2}$ giving us the faster response with respect to the 5 % response criterion:

$$Rg = 2\epsilon Z_0 = 2\epsilon\sqrt{\frac{L_s}{C_s}} \tag{4.1}$$

The input capacitance is extracted by the manufacturer capacitance parameters and the relation between the drain to source and gate to source voltage [45]:

$$C_s \approx C_{iss} + C_{rss}\frac{V_{DS}}{V_{GS}} \approx 2.2\,nF \tag{4.2}$$

The inductance is estimated to be around 30nH including the inductance of the component legs. Therefore:

$$Rg = 2\epsilon Z_0 = 2\epsilon\sqrt{\frac{L_s}{C_s}} = 2\frac{1}{\sqrt{2}}\sqrt{\frac{40}{2.2}} \approx 10\,\Omega \tag{4.3}$$

The PCB also provides space for turn off resistors that are in parallel with the turn-on resistors during the turn-off of the semiconductor. This is achieved with a diode in series with these resistors.

The short circuit protection is achieved with minor teaks to the desaturation circuit provided by the 1ED020I12-F2[44] IC for IGBTs. A figure of this circuit can be seen in Figure 4.1.

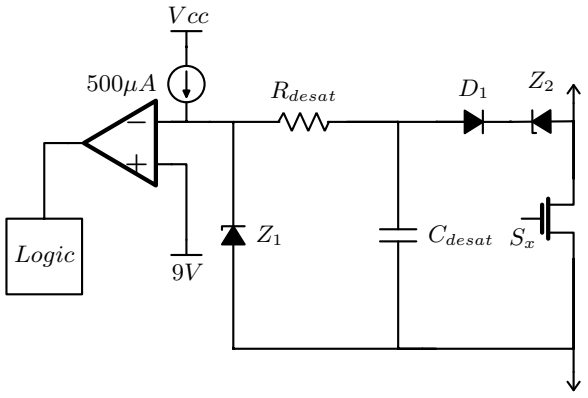



Figure 4.1: Short Circuit protection circuit

The IC provides the $500\mu A$ precision current source, when the voltage at the capacitor $C_{desat}$ exceeds the reference voltage of 9 V, also provided by the IC, the transistor command is driven low. Therefore the value of the capacitor can be sized in the following way:

$$C_{desat} = \frac{I_{desat}t_{desat}}{V_{ref}} \tag{4.4}$$

where $I_{desat}$ is the current of the current source, $V_{ref}$ is the reference voltage of 9 V and $t_{desat}$ is related to the maximum short circuit time in the following away:

$$t_{sc} < t_{desat} \tag{4.5}$$

where $t_{sc}$ is the short circuit withstand time of the transistor. A typical value of 3$\mu$s is used for short circuit withstand time, that yields:

$$C_{desat} = \frac{500 \times 10^{-6} \times 3 \times 10^{-6}}{9} \approx 167pF \tag{4.6}$$

Since 160 pF is the closest standard capacitor with a value lower than 167 pF this is the value used.

The zener diode $Z_1$ is used just to protect the input pin.The zener diode $Z_2$ provides a more important function given that the desaturation circuit uses a 9 V reference since collector emitter voltages in short circuit conditions for the IGBTs are considerably higher than in SiC MOSFETs, the zener diode $Z_2$ complements the drain to source voltage to reach a value higher than 9 V for a short circuit condition. From the datasheet[43] of the device it can be deduced that for the gate driving voltages used, a drain to source voltage higher than 5.5 V represents a short circuit condition, and therefore a zener diode with 4.3 V zener voltage is used to complement. The $R_{desat}$ resistor must be present to limit the current out of the Desat pin of the IC.

## 4.3 DC Link capacitance

The DC Link capacitance bus plays an important role in the 3-Phase inverter, performing a number of crucial functions, such as maintaining a controlled voltage ripple and ensuring a low inductance current path for the high frequency currents that arise due to the PWM control of the transistors.

The selection of DC bus capacitors is mostly influenced by the maximum ripple current that will be observed through the capacitors since capacitors have limits for the maximum current ripple that they can handle. They also must handle high current transients generated by rapidly changes from motoring to breaking. Taking $\Delta$I as the current variation and $\Delta$U the allowed capacitor voltage variation then, the DC bus capacitance can be sized in the following way[46]:

$$C = \frac{\Delta iT}{4\Delta V_{DC}} = \frac{0.2I_{peak}}{4 \times 0.01 V_{DC} f_{sw}} = \frac{0.2 \times 120}{4 \times 0.01 \times 600 \times 20000} = 50\mu F \tag{4.7}$$

Analytically calculating DC link capacitors ripple current depends on a considerable number of parameters (PWM squema, output current and output current variation, DC link capacitors characteristics and their variation with temperature, load inductance and resistance as well as fundamental output frequency)[47, 48]. As a reference the DC link capacitance of the FST 07e inverters that switches at a frequency of 8 kHz is around 100 $\mu$F but as a downside the team experienced considerable problems with the stability of DC link voltage that leads to a number of faults that turn down power to the motors during track time.

Additionally, new generation ceramic capacitors are used close to the semiconductors. This ceramic capacitor not only presents extremely low equivalent series resistances and inductances but they can also handle high ripple currents and have a positive DC bias effect on the capacitance value, meaning an increase in capacitance with increasing voltage. Such effect will act as a snubber for high voltage transients.

The bulk capacitance is provided by two 20$\mu$F capacitors, then capacitors with smaller capacitance and consequently smaller ESL and ESR are places in series this are two capacitors of around 2$\mu$F, finally 3 capacitors of 100nF are also placed in parallel following the same principal, this ensures that high order harmonics can be handled better given that the total inductance is lower.

## 4.4 Voltage, Current and Temperature Sensing

Since the purpose of the designed inverter is to control an electric motor in a highly dynamic environment the inverter must be instrumented in a way that, by itself, allows the measurement of at least the input voltage and the output currents.

Current measurement is achieved using a current transducer from LEM, CKSR 50-NP[49], this transducer is a closed-loop sensor, also called ”zero-flux sensor”. The current to be measured is passed through a primary coil and an hall-effect sensor feeds back an opposing current to the secondary, and the current on the secondary is used to estimate the current on the primary. This particular model allows to measure currents up to 150 A in both directions. One of the advantages achieved with this type of transducers is the high galvanic isolation provided, which is necessary for this type of applications. Furthermore, they also provide excellent linearity and low temperature drift while achieving a high enough measurement bandwidth.

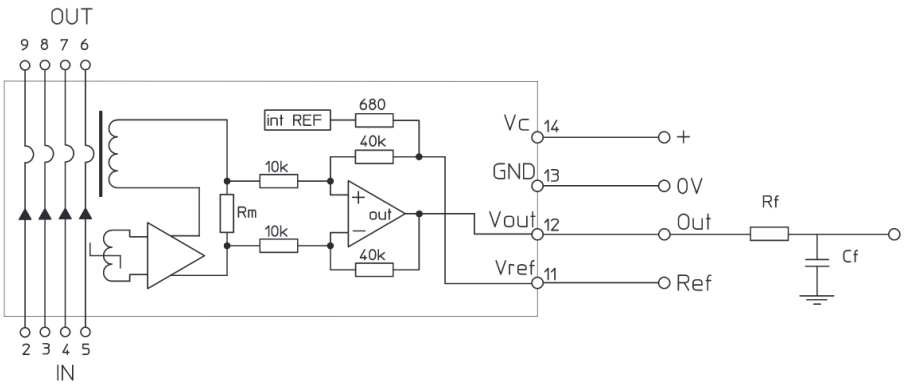



Figure 4.2: Current Sensor schematic, Courtesy of LEM[49]

Figure 4.2 shows the schematic of the current measurement circuit. The output filter was designed to achieve a cut off frequency of around 1.6 kHz since it is the maximum output frequency that can be sent to the motors, which is still far, by at least a factor of 10, of the minimum switching frequency. The

cut off frequency is given by:

$$f_c = \frac{1}{2\pi R_f C_f} = \frac{1}{2\pi 1 \times 10^3 \times 10 \times 10^{-9}} \approx 1600Hz \tag{4.8}$$

where the selected values for $R_f$ and $C_f$ are 1 k$\Omega$ and 10 nF respectively.

Voltage measurement is achieved using a voltage divider that ranges the input voltage from 0 to 600 V to a voltage between 0 and 2 V, that is then feeded to a reinforced isolated amplifier, that modulates the signal through a capacitive isolation and is then demodulated in the low voltage side. The amplifier used is the AMC1311[50] amplifier from Texas Instruments.

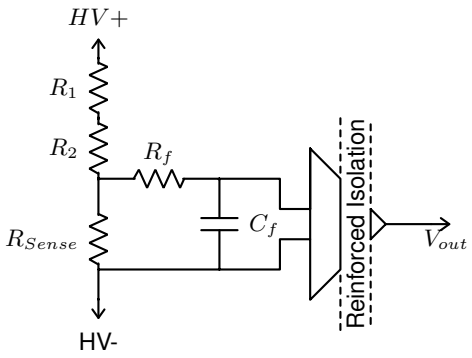



Figure 4.3: Voltage Sensing Schematic

The simplified schematic of the voltage sensing circuit can be seen in Figure 4.3. The filter was designed to provide a cut-off frequency of 80 kHz, which close to the maximum switching frequency. This way the input voltage ripple can be measured. The voltage at $R_{sense}$ is the result of a voltage divider composed by $R_1$,$R_2$ and $R_{sense}$ with the values of 3.01 M$\Omega$, 3.01 M$\Omega$ and 20 k$\Omega$, respectively.

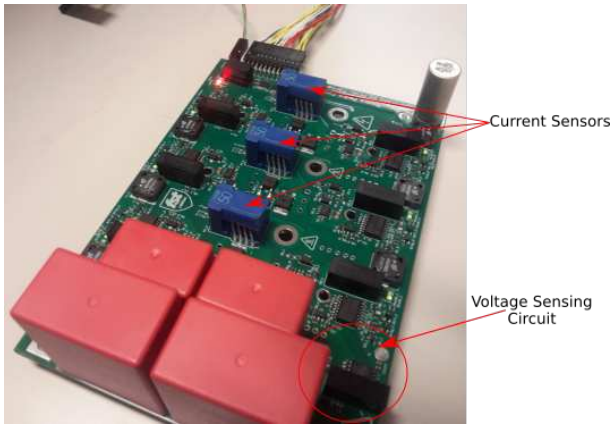



Figure 4.4: Voltage and current sensing in the PCB

Temperature measurement is achieved using a couple of negative temperature coefficient (NTC) resistors that are placed directly into the water cooled cooling plate, allowing to derate the power output in the event of overheating in order to prevent damage of the semiconductors. The placement of the temperature sensor on the cooling plate can be seen in Figure 4.5.

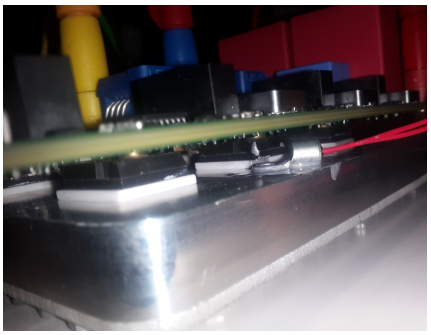


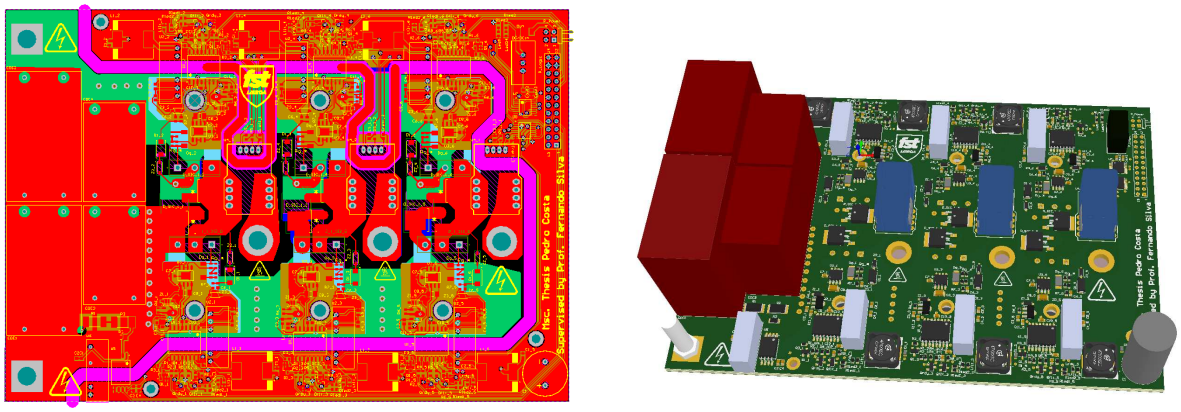
Figure 4.5: Temperature sensing placement on the cooling plate

## 4.5 PCB Design

The PCB was designed using the commercial software Altium Designer [51]. During the layout phase of the design circuitry it is important to take a number of parameters into account. The most important factor to take into consideration when designing a PCB that will handle voltages as high as 1200 V is the creepage distances and insulation across the different PCB layers. As a reference for creepage distances, the Generic Standard on Printed Board Design, IPC2221A, [52] was used.

Special attention was given to the layout of the gate driver circuitry in order to ensure a low inductance path to and from the transistor, since having a low inductance path will reduce gate ringing and provide a smaller delay on the driving signal.

In order to handle the high currents necessary for driving a Formula Student motor, the PCB is composed of 6 layers of 140 $\mu$m thick copper (4 times the regular thickness). Using this conductor thickness and the Standard for Determining Current Carrying Capacity in Printed Board Design, IPC2152[53], the conductors widths were designed in accordance to the expected average RMS currents.



(a) 2D visualization

(b) 3D visualization

Figure 4.6: Altium Designer renders of PCB design files

In Figure 4.6, renders of the PCB design files can be observed. Some effort was placed into providing a compact solution, still since this is the first generation of inverters higher margins were given specially in conductor spacing, and therefore there is still room for improvement as far as compactness on the PCB layout goes. Also as stated before, the use of power modules (already packed transistors in a 2-Level inverter configuration) instead of discrete transistors, might bring even more compactness to the

inverter design.

## 4.6 Cooling Plate

With the aid of former FST team members, a cooling plate design for water cooling was developed. Its intent was more of a proof of concept then a high cooling performance part, therefore it was designed having ease of fabrication in mind. The idea is to maintain a close concept to that used by the current team as to eventually use the same testbenches currently being designed for the FST 08e powertrain.

Table 4.4: Parameters for cooling plate thermal conductive calculation

| Symbol | Parameter | Unit | Value |
|---|---|---|---|
| $\eta$ | Dynamic Viscosity @40° C | $Ps$ | $0.653 \times 10^{-3}$ |
| $\upsilon$ | Kinematic Viscosity @40° C | $m^2/2$ | $0.658 \times 10^{-6}$ |
| $\alpha$ | Thermal Difusivity @40° C | $m^2 s$ | $0.14 \times 10^{-}6$ |
| $k$ | Water Thermal Conduction Coefficient | $W/(mK)$ | 0.61 |
| $\rho_0$ | Water density | $kg/m^3$ | 1000 |
| $Q$ | Pump flow, | $L/min$ | 10.4 |

Based on the parameters of the cooling plate the convective heat transfer coefficient,$h$, will be calculated so that it is possible to see that the cooling plate is capable to comply with the heat transfer requirements. As a side note, in reality the dynamic and kinematic viscosity change with temperature thus changing the convection coefficient making this an iterative process. For simplicity sake it was assumed that these values remain constant and they are assumed for a temperature of 40 degrees, which corresponds to the maximum ambient temperature under which the vehicle performs.

First the equivalent reference cross-section is calculated based on the actual cross section of the cooling plate, $A = 72mm^2$, and the perimeter $P = 36mm$:

$$D = \frac{4A}{P} = 8mm \tag{4.9}$$

The flow speed,$U$, inside the cooling plate can be given by the relation of the pump flow and cross section:

$$U = Q/A \approx 2.5m/s \tag{4.10}$$

Using the flow speed, the reference cross section, the dynamic viscosity and the water density it is possible to calculate the Reynolds Number,$Pr$, that represents a balance between the inertial forces and viscous forces[54]:

$$Re = \frac{\rho_0 U D}{\eta} = 30628 \tag{4.11}$$

It is also possible to calculate the Prandtl Number,$Pr$, that represents the fluid's balance between its kinematic viscosity and thermal diffusion rate[54].

$$Pr = \upsilon/\alpha = 4.7 \tag{4.12}$$

With the Prandtl Number and the Reynolds Number calculated, it is possible to calculate the Nusselts Number. This value represents the ratio between the convective and conductive heat transfer across a boundary. A relation between the Nusselts Number and the Reynolds and Prandtl Number can be obtained using the Dittus-Boelter equation[54]:

$$Nu = 0.023 Re^{4/5} Pr^{0.4} \approx 165.8 \tag{4.13}$$

Finally having the Nusselts Number it is possible to determine the coefficient of convection[54]:

$$h = Nu \frac{k}{D} = 12.6 \times 10^3 \, W/(m^2 K) \tag{4.14}$$

An equivalent thermal circuit can now be used to calculate the temperature rise for a given temperature rise. Knowing that the used aluminium in the cooling plate has a thermal conductivity of 121 $W/(mK)$, and the contact surface of the top of the water channel is about 0.008 $m^2$ then the total thermal resistance can be given by:

$$R_{th} = \frac{1}{0.008h} + \frac{1}{121 \times 0.01} = 0.043 \, k/W \tag{4.15}$$

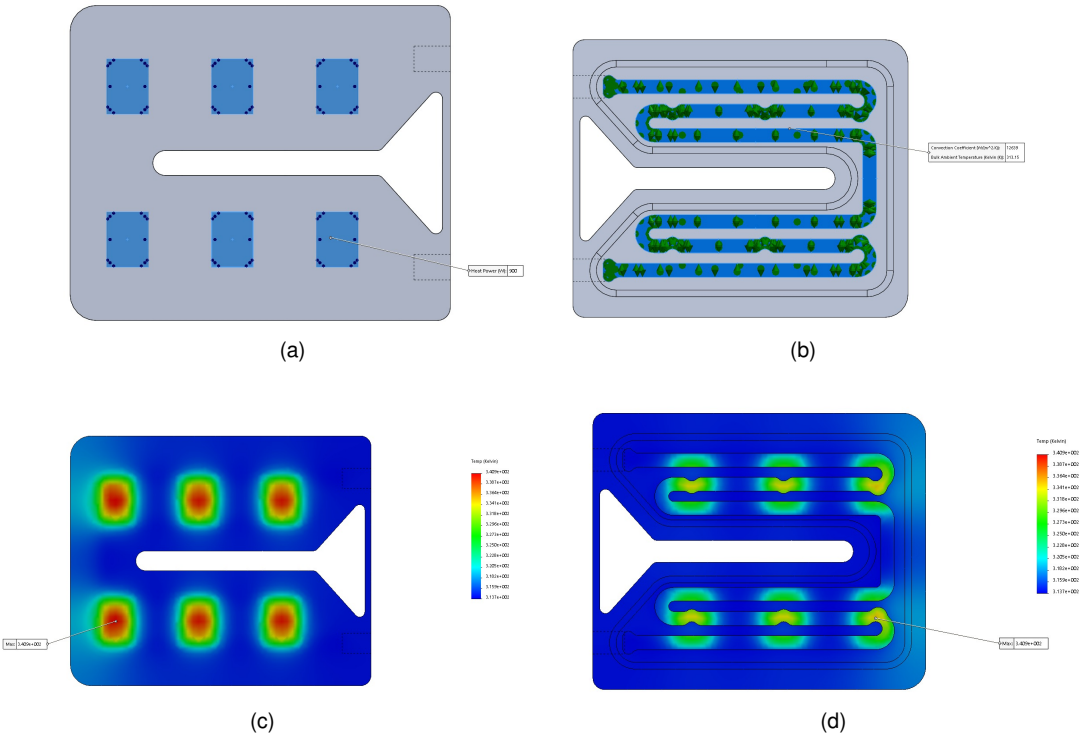
This determination of the convection coefficient assumes that its value remains constant for the range of temperatures calculated and also through the entire cooling plate. Thus ignoring local changes related to the non-uniform flow of water through the circuit.

This means that for example at a total dissipated power of 900 W, equivalent to a 97% efficiency at peak power the temperature increase top of the cooling plate (where the transistor case is placed):

$$\Delta T = 900 R_{th} = 38.7 \, ^\circ C \tag{4.16}$$

Still this thermal resistance does not take into account the convection at the side walls of the cooling plate, therefore a finite element simulation was made using the commercial software Solidworks[55], a dissipated power is defined in the area equivalent to the contact of the transistor as can be seen in Figure 4.7a. The temperature of the fluid is defined as constant and equal to 40 °C with the coefficient of convection calculated, this can be seen in Figure 4.7b. The resulting temperature increase can be seen in Figures 4.7c and 4.7d that yield a temperature rise of 27.75 that as it was expected is lower than the one calculated by the equivalent thermal resistance.

Renders of the cooling plate can be found in Figure 4.8a and 4.8b while the actual manufactured cooling plate can be seen in Figure 4.12a and 4.12b. The cooling plate is equipped with two fittings, for the inlet and outlet of water, that bolt directly into it.

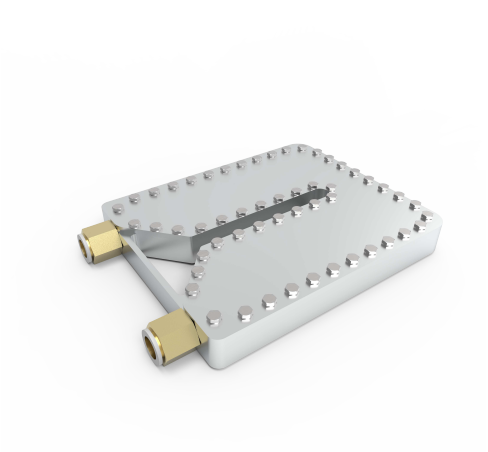


(a) (b)

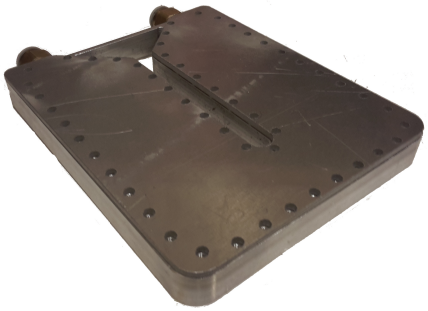
(c) (d)

Figure 4.7: Cooling plate finite element analysis simulations

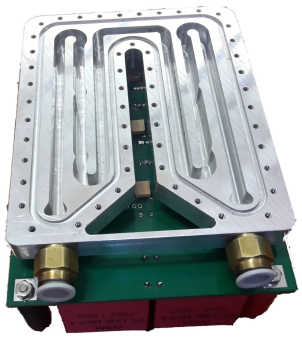
(a) Cooling Plate Render detail without cover



(b) Cooling Plate Render detail with cover



(c) Cooling Plate detail

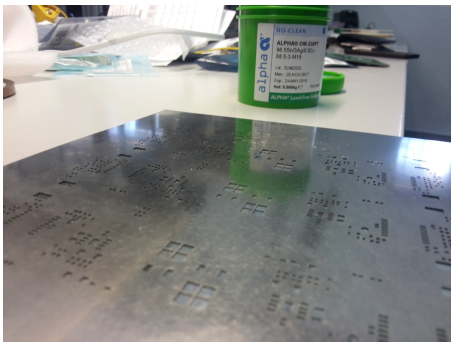


(d) Cooling Plate mounted on the inverter

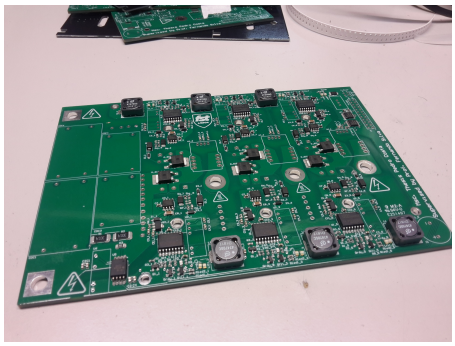
Figure 4.8: Computer drawing renders and actual manufactured cooling plate

## 4.7 PCB Manufacturing

The high copper density of the PCB makes it harder than normal to solder. Fortunately Primetec, a OEM company that sponsors the FST team, provided access to a reflow soldering oven, therefore all surface mount component were hand placed in the PCB, after previously filling the PCB pads with solder paste, and then soldered in the oven. Finally, all through hole components were hand soldered using a soldering iron. Some details of this process can be seen in Figure 4.9

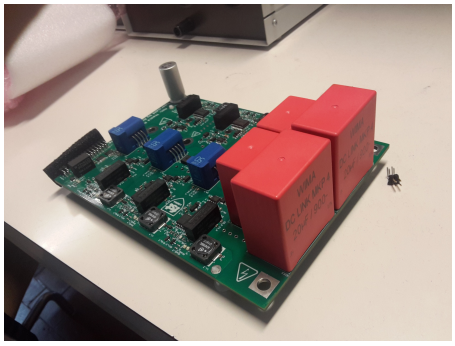



(a) Solder Paste Placement



(b) SMD Component Placement

(c) Reflow Soldering Oven



(d) Final result after trough hole component soldering

Figure 4.9: PCB manufacturing process

The transistors and the low ESL and low ESR ceramic capacitors are placed on the bottom side of the PCB and can be seen in Figure 4.10.

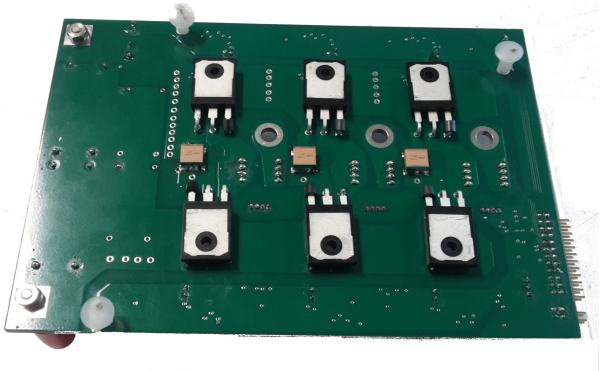
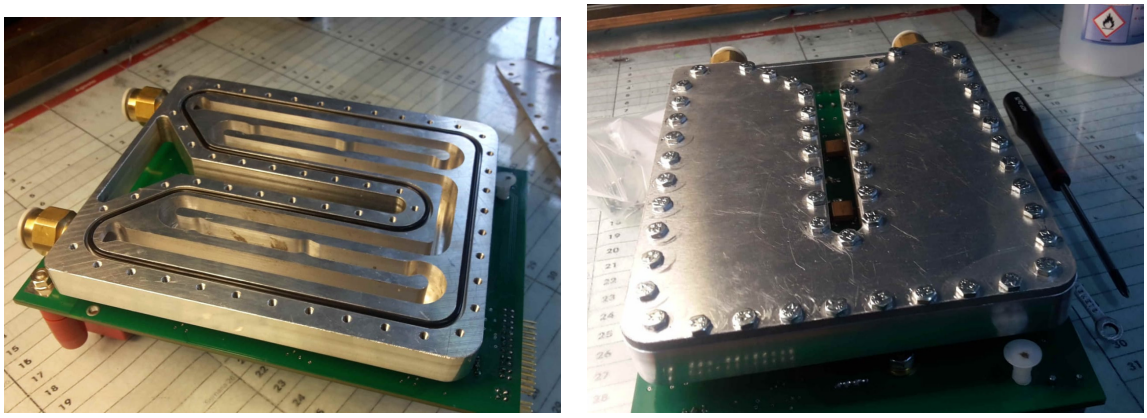


Figure 4.10: Transistors and capacitors on the bottom side of the PCB

Even though a lot of attention during the PCB design was given to minimize potential errors, a couple

of errors were made in the footprint design of components, specifically in the freewheeling diode and the current sensor. Such errors were corrected manually in the prototype and the design files were updated for future versions.



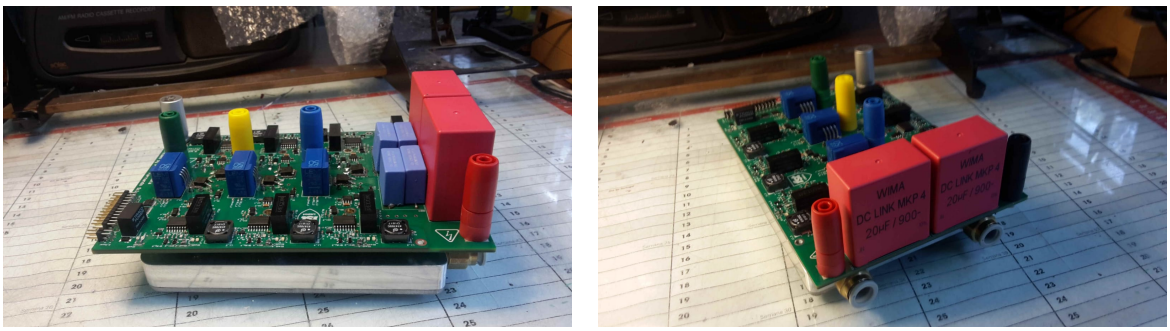
(a) Cooling Plate O-Ring placement

(b) Cooling Plate cover bolted

Figure 4.11: Assembly process of the cooling plate

## 4.8 Final Assembly

The last part of the Inverter prototype assembly is the cooling plate. The cooling plate is mounted directly on the transistor pads using a ceramic material as thermal interface between the transistor pads and the cooling plate that provides a good thermal conductivity (around 25 W/mK) with a high dielectric strength for electric isolation. Six M3 size bolts are used to fasten the cooling plate onto the transistors.



(a) Side View

(b) Top View

Figure 4.12: Complete Inverter Assembly

The complete inverter assembly can be seen in Figure 4.12. The Inverter weights approximately 1.05 Kg without water inside the cooling plate. As a comparison, the inverter supplied by AMK[5] provides a weight of 11 Kg for a quadruple inverter also without water inside the cooling plate, this adds up to a weight per inverter of 2.75 Kg. This leads to a weight reduction of 1.7 Kg per inverter that is equivalent to a reduction of about 62% in weight.

Table 4.5 provides an insight about the weight, power and power densities of the two past inverter

Table 4.5: Comparison of power density's of different inverter solutions

| | AMK Inverter[5] | Siemens Inverter[4] | Self Made Inverter |
|---|---|---|---|
| Power [kW] | 30 | 45 | 30 |
| Weight [kg] | 2.75 | 14.60 | 1.05 |
| Power Density [kW/kg] | 10.91 | 3.1 | 28.57 |

solutions adopted by the team as well as the prototype build in this master thesis. The provided solution represents an increase of around 3 times in power density when compared to the previous solution (AMK Inverter[5]) and an increase of around 9 times the power density when compared to the FST 06e solution (Siemens Inverter[4]).

It is also worth to mention that the prototyped inverter has about half the occupied volume of the AMK inverter, that will result in a more compact packaging that by consequence will reduce the weight of the inverter container, that will result in about doubling the volumetric power density, ($kW/m^3$).

# Chapter 5

# 3 Phase Inverter Testing

In this chapter the testing of the developed prototype is described.

As a starting point the low voltage circuitry was checked for proper behavior as well as the gate driver circuitry. After a successful check of both the low voltage and gate driver circuitry, small corrections had to be made to the current sensor and freewheeling diodes due to errors on their footprint design.

The low voltage circuitry includes logic that disables all gate drivers if one gate driver detects a short circuit. This was tested by removing temporally one of the Zener diodes from the desaturation circuit of the gate driver and thereby triggering the desaturation circuit. It was confirmed that all gate drivers were disabled, only to be enabled by a reset signal from the microcontroller or from a power cycle to all the circuitry.

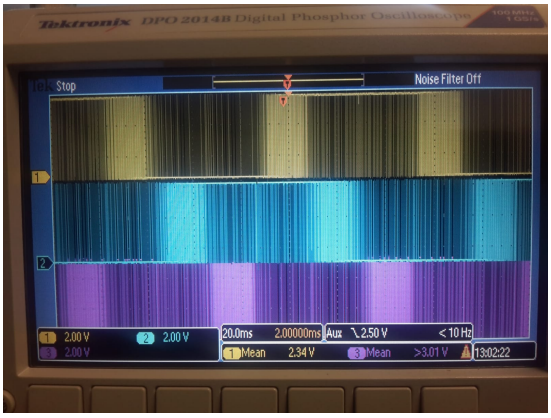
In order to properly test the inverter, a variable frequency modulator had to be designed, by using a microcontroller a space vector modulator was implemented. The microcontroller used was a dsPIC33EV256GM106 [56] placed on an evaluation board from microchip [57].

Space vector modulation is an algorithm for the control of pulse width modulation[11], using 8 different vectors, where 2 of those are zero voltage vectors, that allows to select the duty cycle of the semiconductors for a given reference by a combination of vectors.

The resulting waveforms of the implemented modulator can be seen in Figure 5.1.

To validate the modulator behaviour the first tests under power were performed using a start connected RL load, as can be seen in Figure 5.2, where the inverter was supplied by a 80 V power supply, and feeded the RL load with AC currents with variable frequency. The load current could be varied by resorting to the variable resistors.

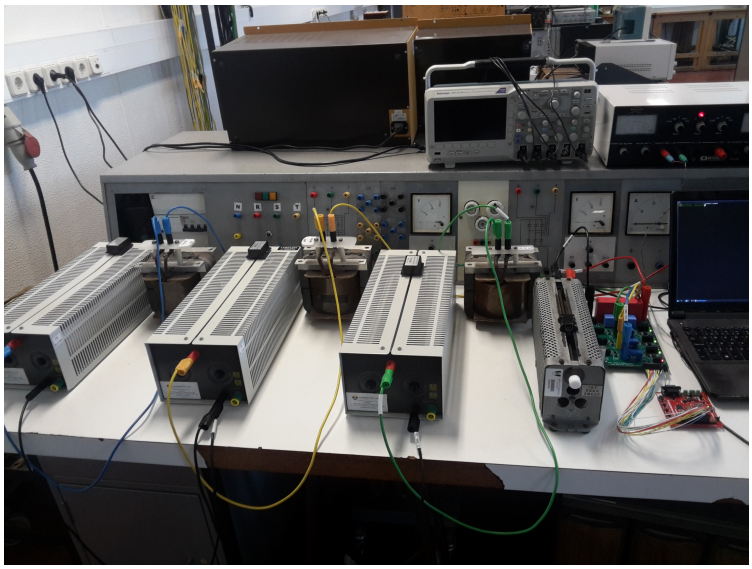
Since this experiment was dedicated to test the modulator, no external measurements were made. Still it was ensured that the current and voltage sensing embedded in the inverter were correctly working. Different switching frequencies and output frequencies were tested to ensure the consistency of the modulator implementation.



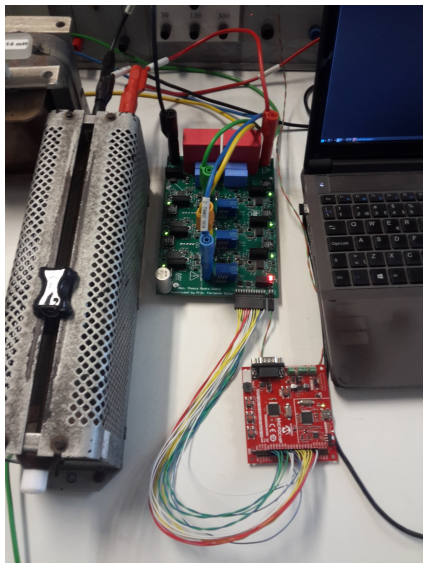

(a) Raw modulator output signals


(b) Low pass filtered modulator output signals

Figure 5.1: Modulator output waveforms



(a) Experiment Setup



(b) Inverter and controller detail

Figure 5.2: Inverter testing against a RL Load

After successful control of the frequency and amplitude of the output current waveform in the RL load, a delta connected induction motor was then connected to the inverter as it can be seen in Figure 5.3.

Even though a small test, it shows the validity of the concept for designing highly compact inverters for a formula student vehicle. The power supplied was used to supply a voltage of 150 V (the maximum voltage it could output). To generate a load a flywheel was coupled to the induction motor.

The setup was then rearranged to add a wattmeter to measure the power delivered to the machine, as it can be seen in Figure 5.4a, and an ampmeter was placed at output of the power supply to measure the current delivered to the inverter that together with a measurement of the input voltage provided the input power to the inverter. With this setup, it was possible to spin the motor close to its nominal speed of 2800 rotations per minute (RPM), Figure 5.4b shows a tachometer measurement of motor speed. Still given the low nominal power of the motor no actual data could be withdrawn besides the proof of

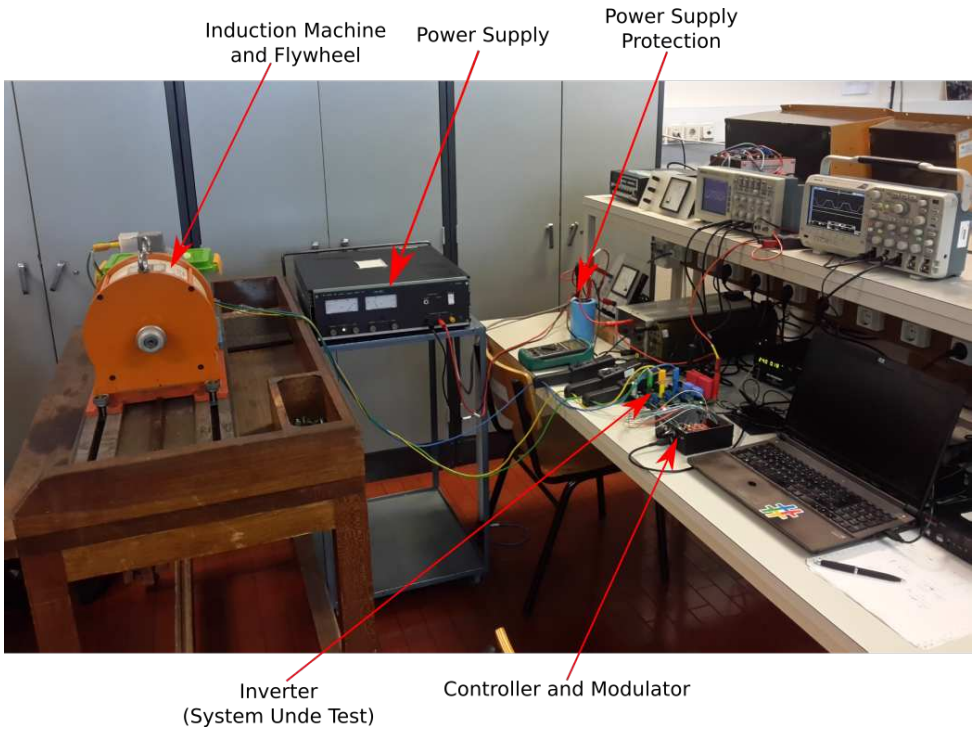



Figure 5.3: First Test Setup with the inverter controlling an induction motor

concept.

(a) Experiment Setup

(b) Machine RPM measurement

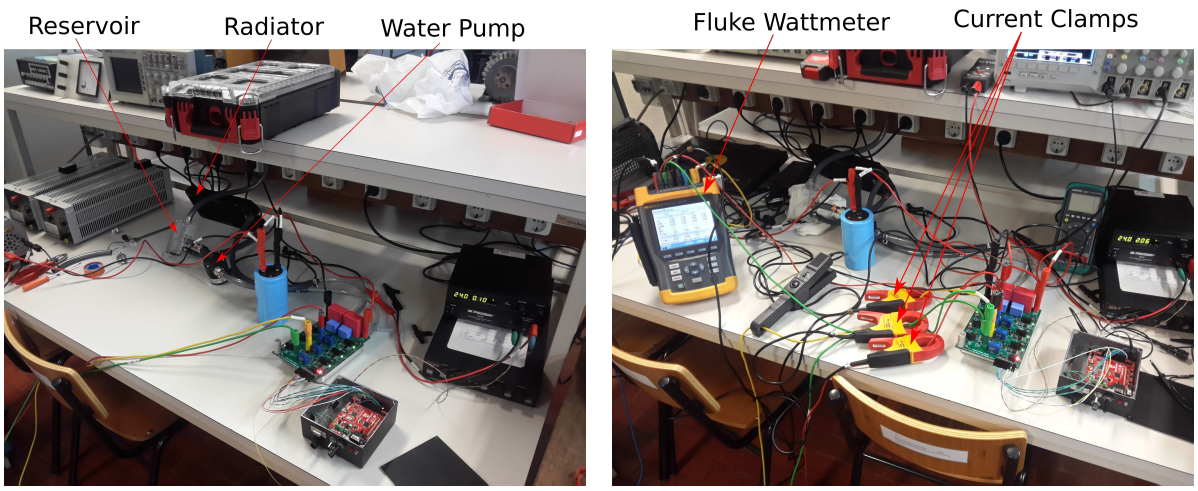
Figure 5.4: Second Test Setup

In an attempt to measure the efficiency of the prototype the inverter was connected again to an RL load.

This time de cooling circuit composed of a reservoir, a water pump, a radiator and all the tubing to connect the cooling circuit was also assemble, as can be seen in Figure 5.5a.

The output was measured resorting to a power measurement device from Fluke as can be seen in Figure 5.5b. Using the measurements provided by this device complemented with a power measurement at the input side performed with a center 120 voltmeter and a center 223 ammeter the efficiencies are measured for a variety of output powers. Still the maximum output power is limited by the equipment

available at the laboratory. In this case the limit is the power supply for which the maximum output power is 3 kW.




(a) Cooling Circuit Assembly

(b) Output power measurement with Fluxe wattmeter

Figure 5.5: Cooling circuit and power measurement setup

Efficiency was measured for 3 different DC link voltages at different output powers. The output power was varied resorting to a variable resistor on the load. The complete setup can be seen in Figure 5.8. To fully use the measurement range of the current probes 4 turns of the cable carrying the current were given to the clamp probe.

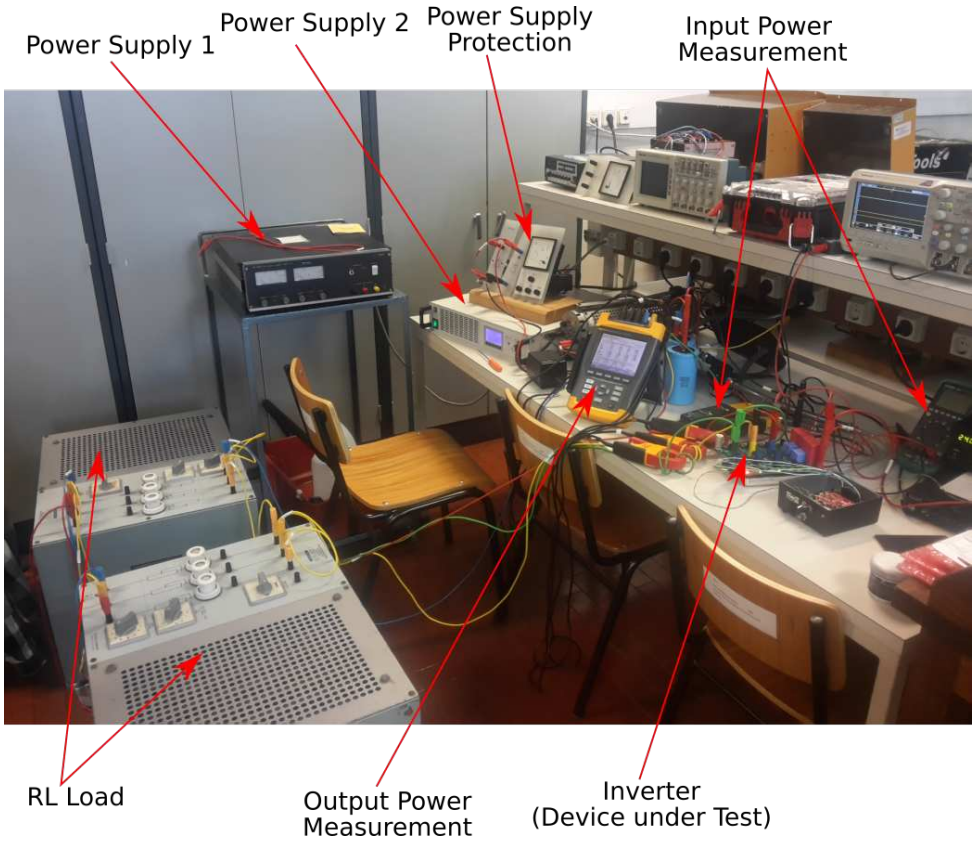



Figure 5.6: Test setup for efficiency measurement

Table 5.1: Example of acquired data for a set of efficiency measurements

| $V_{in}$ [V] | $I_{in1}$ [A] | $I_{in2}$ [A] | $V_{a_{rms}}$ [V] | $V_{b_{rms}}$ [V] | $V_{c_{rms}}$ [V] | $I_{a_{rms}}$ [A] | $I_{b_{rms}}$ [A] | $I_{c_{rms}}$ [A] | Power [kW] |
|---|---|---|---|---|---|---|---|---|---|
| 298.7 | 2.252 | 2.250 | 120.5 | 121.4 | 121.2 | 1.8 | 1.8 | 1.8 | 0.66 |
| 298.6 | 3.211 | 3.220 | 121.8 | 120.4 | 120.2 | 2.6 | 2.6 | 2.6 | 0.94 |
| 298.3 | 4.136 | 4.154 | 121.8 | 119.9 | 120.0 | 3.4 | 3.4 | 3.4 | 1.22 |
| 298.3 | 5.016 | 5.042 | 121.6 | 119.6 | 120.1 | 4.1 | 4.1 | 4.2 | 1.48 |
| 298.1 | 5.912 | 5.946 | 121.7 | 119.2 | 120.1 | 4.9 | 4.9 | 4.9 | 1.75 |
| 298.0 | 6.795 | 6.835 | 121.5 | 119.0 | 120.2 | 5.6 | 5.6 | 5.7 | 2.01 |
| 298.7 | 7.647 | 7.700 | 121.5 | 118.6 | 120.2 | 6.4 | 6.4 | 6.4 | 2.27 |

An example of the acquired data during one efficiency setup measurement can be seen in table 5.1. Both input voltages and currents are measured as well as the power factor and the output power.

In Figure 5.7, it is possible to observe the efficiencies ploted against time. A special remark is given to peak efficiencies for 300 and 600 V of 98.8% and 97.5%, respectively. It is clear that switching losses are dominating the efficiency given that the output current at 600 V is around half of that at 300 V, therefore the increase in switching losses due to the increase in voltage surpasses the decrease of the conduction losses.

Unfortunately no efficiencies could be measured beyond 3 kW due to the power supply and the load limitations. Still it is expected for efficiency to rise before it starts decreasing.

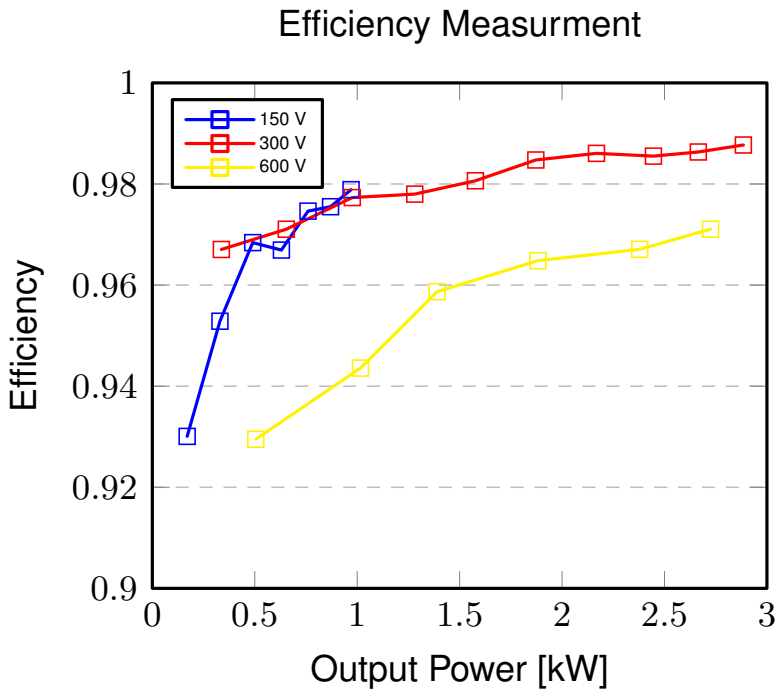



Figure 5.7: Measured efficiency at 150,300 and 600 V

Two of the resulting phase to phase voltages, as well as one of the phase currents can be seen in Figure 5.8, where the resulting waveforms behave as expected providing the 3 line to line voltage levels.

One of the major advantages provided by using a SiC Inverter against a Silicon IGBT is the ability to

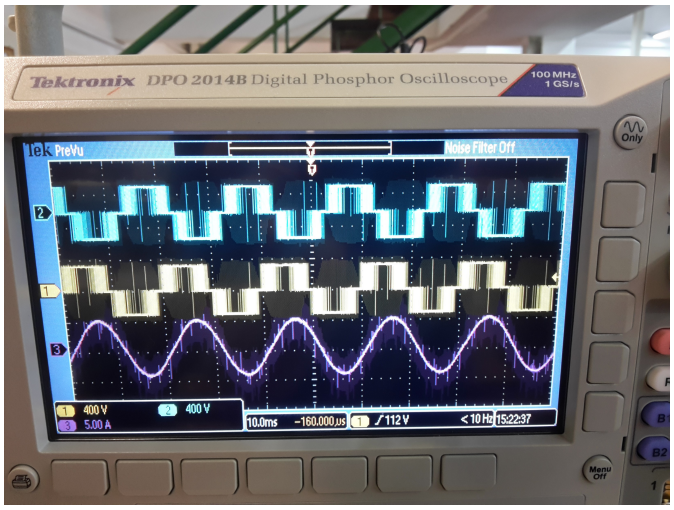
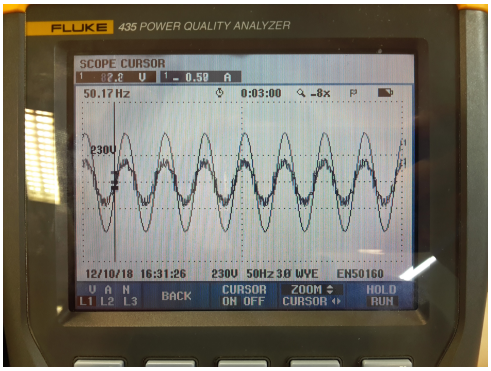
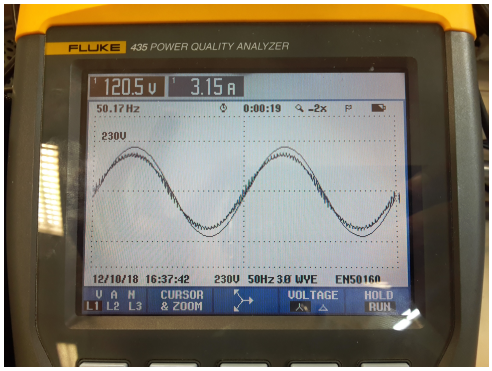



Figure 5.8: Waveform of phase to phase voltages and output current on one of the phases

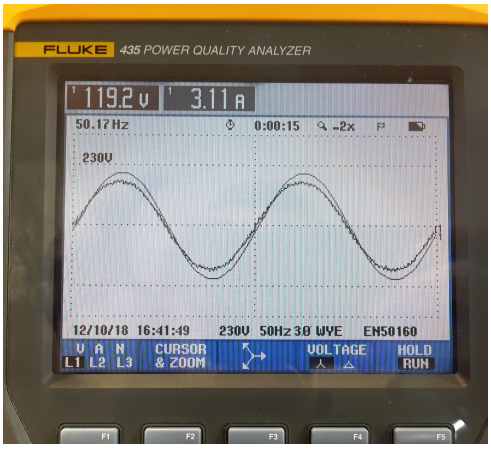
have higher switching frequencies given the reduction of switching losses. This provides better current sinusoidal waves to the motor, that not only increases the motor life but also provides a better efficiency profile of the motor and a reduced torque ripple that eases the strucutral requirements of the mechanical parts of the motor and transmission.



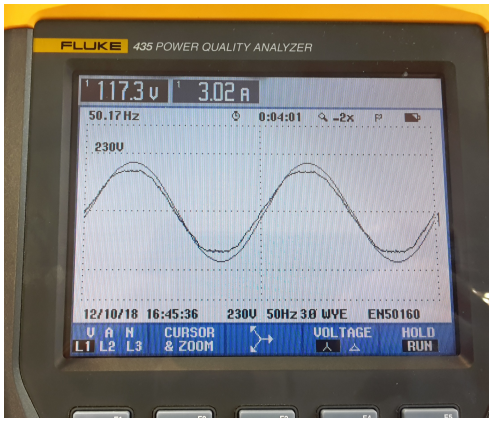

(a) Output at 10 kHz $f_{sw}$




(b) Output at 20 kHz $f_{sw}$




(c) Output at 40 kHz $f_{sw}$




(d) Output at 80 kHz $f_{sw}$

Figure 5.9: Waveforms of output currents at 300 V DC link voltage

Table 5.3: Weighted Total harmonic distortion for the first 50 harmonics

| | Current Harmonic Distortion [%] | Voltage Harmonic Distortion [%] |
|---|---|---|
| $f_s = 10kHz$ | 1.4 | 3.4 |
| $f_s = 20kHz$ | 1.0 | 2.5 |
| $f_s = 40kHz$ | 0.9 | 2.1 |
| $f_s = 80kHz$ | 0.8 | 1.8 |

Figures 5.9a, 5.9b, 5.9c and 5.9d show one of the phases current and voltage for a switching frequency of 10 kHz, 20 kHz, 40 kHz and 80 kHz, respectevely. It is clear that with the increased switching frequency the quality of the output waves increases susbtancialy.

Table 5.2 shows measures of total harmonic distortion on the first 50 harmonics, complementing the waveforms showing the reduction of distortion with the increase of the switching frequency.

These preleminary experiments show the potencial benefits provided by the the developed inverter against past solutions particular for the efficiency and the quality of the output waves.

The author would have liked to perform more experiments to the developed prototype in order to bring more insight of the system limitations. More tests weren't performed since they would requeire different test setups in particular for higher power experiments, for which equipment was not directly available, and the time bounds limited the amount of experiments data aquired.

# Chapter 6

# Conclusions

During the development of this master thesis the possibility of designing an inverter for a Formula Student prototype was evaluated and a first generation prototype was developed. To do so the inverter operation was studied with a particular focus on the influence of the semiconductors on the efficiency of these devices.

For this purpose new wide bandgap semiconductor technologies were considered and their benefits were evaluated using only datasheet parameters of both state of the art SiC MOSFET's and GaN HEMT's. The obtained results were promising as far as efficiency goes and with the advantage of potentially pushing the switching frequency higher with all the benefits that brings to the electric machine controlled by the inverter.

Still given that such technologies are not yet mature on the market, experimental measurements had to be made to devices of each technologies manufactured by leading companies in the development of these devices. The experiments were limited to the equipment available at Laboratório de Máquinas of the Alameda Campus of Instituto Superior Técnico.

With the gathered knowledge and data obtained during the experiments, models were created to better estimate losses for future inverters of the team, allowing a better design of the cooling systems, which has great relevance for a Formula Student Prototype governed by performance.

A gate driver was also designed together with the sizing of the rest of the inverter components (DC Link capacitance, connectors, current voltage and temperature measurement, cooling plate and PCB parameters) in order to be able to develop a complete prototype.

The developed prototype serves not only as a proof of concept (since it was designed thinking in the integration in a Formula Student prototype) but also as a platform that will stay for the team to perform extra testing and research.

Some initial tests were made to the designed prototype. Starting from the gate driving circuitry and low voltage logic, to the implementation of a space vector modulator that allowed to supply a 3 Phase RL load as well as a small motor. Testing at higher powers was not possible given the lack of load that could handle the peak power of the inverter in the Laboratory combined with the lack of time to design and assemble one.

## 6.1 Achievements

The major achievement obtained with this master thesis was the development of a SiC MOSFET inverter in a time where very few Formula Student teams across the world develop their own inverters and much less using new wide bandgap technologies. Furthermore providing power densities considerably higher than the ones presented by commercial solutions that the team currently uses. Such prototype will stay at the hands of the new Formula Student team of Instituto Superior Técnico.

As far as the objectives under which this thesis was developed:

- The current systems efficiencies were theoretically estimated;
- SiC MOSFET's and GaN HEMTS were evaluated both analytically and experimentally;
- Those solutions were compared and the SiC MOSFET was selected;
- The subsystems supply and drive of the semiconductors were designed;
- A dedicated PCB for the inverter was designed and manufactured with integrated cooling devices;
- Some testing was done to the inverter even though not in the rated power;
- Specific documents of a number of topics in the development of the inverter, together with schematics, simulations and code are left to the team for further improvement.

## 6.2 Future Work

During the development of this master thesis a considerable amount of decisions had to be made were other paths possible were left unexplored. In what is concerned with experimental measurements it would be beneficial to decouple the temperature of the experiments and therefore obtain an extra degree of freedom. To do so, the experiments would require to be executed in a temperature controlled environment where the ambient temperature could be externally controlled. For the same test procedure the accuracy of the results could be increased resorting to a calorimeter so that dissipated power could be measured with further accuracy and less calibration efforts.

The downside of not being able to decouple turn on from turn off losses could be solved resorting to a high bandwidth current measurement device that would allow to measure the current waveforms during switching.

Given that the technologies are maturing and new devices are being placed into the market every year, continuous testing is required to keep selecting the best devices for the application.

The gate driver design, even though equipped with protections is a simple toten-pole driver, further investigation and testing would lead to better drivers that would ultimately also benefit efficiency such as resonant gate drivers [58, 59].

Even though in this thesis it was opted the use discrete devices, integrated power modules can bring advantages specially in easiness of cooling given the lower thermal resistances offered by a full packed

power modules. Another advantage might be the compactness of the system that would result form a more compact power modules that will ultimately have a positive impact in reducing weight.

The analysis of the ripple currents in the DC Link capacitors is also of an extreme importance for the proper selection and design of the DC Link capacitors. This had to be overlooked in this thesis in detriment of other objectives and further investigation both analytical and experimental should be made.

Finally, new topologies such as the double inverter for the open-winding should be further investigated though they would require further changes in the overall powertrain concept other than the inverter itself, with the benefit of potentially bringing further efficiency and better dynamics of the powertrain solution presented by the team.

# Bibliography


[1] European Automobile Manufacturers' Associatio (Quarter 1 to 4 of 2017). New passenger car registrations by alternative fuel type in the european union, 2017.

[2] CNBC Tom DiChristopher. Headline on electric vehicle growth, 2018.

[3] João Gonçalo Viseu Vieira Sarrico. Design and implementation of a 20kw, 12000rpm permanent magnet synchronous motor (pmsm) for the ist formula student powertrain. Master's thesis, University of Lisbon - Técnico Lisboa, Rua Rovisco Pais n1, 2017.

[4] Siemens AG. *1TE28-5AA3 - SINGLE MOTOR MODULE Inverter*, 1 2014.

[5] AMK-Group. *KW26-S5-FSE-4Q - Formula Student Racing Kit*, 1 2015. Version. 26.

[6] O. Stalter, B. Burger, and S. Lehrmann. Silicon carbide (sic) d-mos for grid-feeding solar-inverters. In *2007 European Conference on Power Electronics and Applications*, pages 1–10, Sept 2007.

[7] N. Kaminski and O. Hilt. Sic and gan devices - wide bandgap is not all the same. *IET Circuits, Devices Systems*, 8(3):227–236, May 2014.

[8] Microsemi. Gallium nitride (gan) versus silicon carbide (sic) in the high frequency (rf) and power switching applications. Technical report, 2017.

[9] H. Amano, Y. Baines, E. Beam, Matteo Borga, T. Bouchet, Paul R. Chalker, M. Charles, Kevin J. Chen, Nadim Chowdhury, Rongming Chu, Carlo De Santi, Maria Merlyne De Souza, Stefaan Decoutere, L. Di Cioccio, Bernd Eckardt, Takashi Egawa, P. Fay, Joseph J. Freedsman, L. Guido, Oliver Häberlen, Geoff Haynes, Thomas Heckel, Dilini Hemakumara, Peter Houston, Jie Hu, Mengyuan Hua, Qingyun Huang, Alex Huang, Sheng Jiang, H. Kawai, Dan Kinzer, Martin Kuball, Ashwani Kumar, Kean Boon Lee, Xu Li, Denis Marcon, Martin März, R. McCarthy, Gaudenzio Meneghesso, Matteo Meneghini, E. Morvan, A. Nakajima, E. M.S. Narayanan, Stephen Oliver, Tomás Palacios, Daniel Piedra, M. Plissonnier, R. Reddy, Min Sun, Iain Thayne, A. Torres, Nicola Trivellin, V. Unni, Michael J. Uren, Marleen Van Hove, David J. Wallis, J. Wang, J. Xie, S. Yagi, Shu Yang, C. Youtsey, Ruiyang Yu, Enrico Zanoni, Stefan Zeltner, and Yuhao Zhang. The 2018 GaN power electronics roadmap, 2018.

[10] Nando Kaminski and Oliver Hilt. SiC and GaN devices – wide bandgap is not all the same. *IET Circuits, Devices & Systems*, 8(3):227–236, 2014.

[11] José Fernado Alves da Silva. *Electrónica industrial: Semicondutores e Conversores de Potência*. Fundação Calouste Gulbenkian, Av. de Berna — Lisboa, 2013.

[12] J . Huselstein, C Gauthia, C Glaize, C Gauthier, and C Glaize. Use of the MOSFET channel reverse conduction in an inverter for suppression of the integral diode recovery current. In *1993 Fifth European Conference on Power Electronics and Applications*, pages 431–436 vol.2, 1993.

[13] Alessandro Acquaviva and Torbjörn Thiringer. Energy efficiency of a SiC MOSFET propulsion inverter accounting for the MOSFET's reverse conduction and the blanking time. In *2017 19th European Conference on Power Electronics and Applications, EPE 2017 ECCE Europe*, volume 2017-January, 2017.

[14] T. Palacios, A. Chakraborty, S. Heikman, S. Keller, S. P. DenBaars, and U. K. Mishra. AlGaN/GaN high electron mobility transistors with InGaN back-barriers. *IEEE Electron Device Letters*, 27(1):13–15, 2006.

[15] E G Shivakumar, K Gopakumar, S K Sinha, Andre Pittet, and V T Ranganathan. Space Vector PWM Control of Dual Inverter Fed Open-End Winding Induction Motor Drive. *EPE Journal*, 12(1):9–18, 2002.

[16] Reaz Ul Haque, Alex Kowal, Jeffrey Ewanchuk, Andy Knight, and John Salmon. PWM control of a dual inverter drive using an open-ended winding induction motor. In *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, pages 150–156, 2013.

[17] A.E. Fitzgerald. *Electric machinery*, volume 319. 2003.

[18] Ned Mohan, Tore M., and William Robbins. *Power Electronics*. Number 2. 1989.

[19] Infineon Technologies AG. *FS200R12PT4 - 200V sixpack IGBT module*, 12 2013. Rev. 2.2.

[20] Wolfspeed, A Cree Company. *C2M0025120D - 2nd-Generation Z-FET 1200-V, SiC MOSFET*, 6 2018. Rev. B.

[21] GaN Systems. *6GS66516T - 650V Enhancement Mode GaN Transistor*, 4 2018. Rev. 180422.

[22] R. Kibushi, T. Hatakeyama, K. Yuki, N. Unno, and M. Ishizuka. Comparison of thermal properties between si and sic power mosfet using electro-thermal analysis. In *2017 International Conference on Electronics Packaging (ICEP)*, pages 188–192, April 2017.

[23] Andreas Maerz, Teresa Bertelshofer, and Mark-M Bakran. A structural based thermal model description for vertical sic power mosfets under fault conditions. 2016, 01 2016.

[24] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, Z. Liang, D. Costinett, and B. J. Blalock. Temperature-dependent short-circuit capability of silicon carbide power mosfets. *IEEE Transactions on Power Electronics*, 31(2):1555–1566, Feb 2016.

[25] Maxime Berthou, Dominique Planson, and Dominique Tournier. Short-circuit capability exploration of silicon carbide devices. 821-823:810–813, 06 2015.

[26] G. Romano, L. Maresca, M. Riccio, V. d'Alessandro, G. Breglio, A. Irace, A. Fayyaz, and A. Castellazzi. Short-circuit failure mechanism of sic power mosfets. In *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, pages 345–348, May 2015.

[27] J. N. Davidson, D. A. Stone, and M. P. Foster. Required cauer network order for modelling of thermal transfer impedance. *Electronics Letters*, 50(4):260–262, February 2014.

[28] Shan Yin, Tao Wang, K. J. Tseng, Jiyun Zhao, and Xiaolei Hu. Electro-thermal modeling of sic power devices for circuit simulation. In *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, pages 718–723, Nov 2013.

[29] GaN Systems. *Modeling Thermal Behavior of GaN PX E-HEMTs Using RC Thermal SPICE Models*, 1 2017. Rev. 1.

[30] GaN Systems. Evaluation board: Gs66508b-evbdb, 2017.

[31] Wolfspeed/CREE. Kit8020-crd-8ff1217p-1: 1200v mosfet evaluation kit, 2017.

[32] Milwaukee Tools. *2260-21NST - M12 160 X 120 Thermal Imager (NIST) Kit*, 4 2013. Serial Number. C87A.

[33] Milwaukee Tools. *2270-20 - Contact Temp Meter*, 5 2012. Serial Number. D13A.

[34] CENTER TECHNOLOGY CORP. *306 - Data Logger Thermometer*.

[35] Mircochip. *dsPIC33EP256MU806 -DSC with Dual Motor Control, Dual CAN and USB*, 4 2018. Rev. G.

[36] GaN Systems. *GS66508 - B650V Enhancement Mode GaN Transistor*, 7 2018. Rev. 180709.

[37] FSAE. Formula Student competition rules. http://www.fsaeonline.com, 2016.

[38] Inc. Analog Devices. Ltspice xvii. `http://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html`, 2018.

[39] MATLAB SIMULINK. *version 9.1.0 (R2016b)*. The MathWorks Inc., Natick, Massachusetts, 2016.

[40] Ankit Rohatgi. Webplotdigitizer. https://automeris.io/WebPlotDigitizer/, 2018.

[41] Ashok Bindra. Wide-bandgap-based power devices reshaping the power electronics landscape, 2015.

[42] A. Bindra. Wide-bandgap power devices: Adoption gathers momentum. *IEEE Power Electronics Magazine*, 5(1):22–27, March 2018.

[43] Wolfspeed, A Cree Company. *C2M0040120D - 2nd-Generation Z-FET 1200-V, SiC MOSFET*, 6 2018. Rev. B.

[44] Infineon Technologies AG. *1ED020I12-F2 - Single IGBT Driver IC*, 9 2017. Rev. 2.1.

[45] José Fernado Alves da Silva. Metal oxide semiconductor field effect transistors. Lecture in Electronic Power Conversion and Storage, 2017.

[46] João José Esteves Santana and Francis Labrique. *Electrónica de Potência*. Fundação Calouste Gulbenkian, Av. de Berna — Lisboa, 1991.

[47] Brendan Peter McGrath and Donald Grahame Holmes. A general analytical method for calculating inverter DC-link current harmonics. *IEEE Transactions on Industry Applications*, 45(5):1851–1859, 2009.

[48] M. Bierhoff and F.W. Fuchs. DC link harmonics of three phase voltage source converters influenced by the pulse width modulation strategy-an analysis. *31st Annual Conference of IEEE Industrial Electronics Society, 2005. IECON 2005.*, pages 491–496, 2005.

[49] LEM International SA. *CKSR 50-NP - Current Transducer CKSR series*, 12 2015. Version. 13.

[50] Texas Instruments. *AM1311 - 2V Input, Reinforced Isolated Amplifier With High CMTI for Voltage Sensing*, 6 2018. Version. SBAS786A.

[51] Altium Altium Designer. *Altium Designer 2018*. Altium Limited, La Jolla, California, 2018.

[52] Generic Standard on Printed Board Design . Standard, IPC – Association Connecting Electronics Industries, Bannockburn, Illinois, 20 2012.

[53] Standard for Determining Current-carrying Capacity in Printed Board Design. Standard, IPC – Association Connecting Electronics Industries, Bannockburn, Illinois, 8 2009.

[54] Frank P Incropera, Eds.)Water (Vol. 6th). John Wiley & Sons. http://doi.org/10.1016/j.applthermaleng.2011.03.022P DeWitt, David Incropera, F. P., DeWitt, D. P., Bergman, T. L., & Lavine, A. S. (2007). Fundamentals of Heat and Mass Transfer. (F. P. Incropera & F. P. F. O. H. A. M. T. Incropera, Theodore L Bergman, and Adrienne S Lavine. *Fundamentals of Heat and Mass Transfer*, volume 6th. 2007.

[55] Dassault Systems. *Solidworks 2018*. Dassault Systems, Vélizy-Villacoublay, France, 2018.

[56] Mircochip. *dsPIC33EV256GM106 - 5V Robust DSC with CAN, Safety, Motor Control*, 5 2018. Rev. G.

[57] Mircochip. *dsPIC33EV 5V CAN-LIN STARTER KIT*, 11 2014. Rev. A.

[58] Philip Anthony, Neville McNeill, and Derrick Holliday. High-speed resonant gate driver with controlled peak gate voltage for silicon carbide MOSFETs. *IEEE Transactions on Industry Applications*, 50(1):573–583, 2014.

[59] Juzheng Yu, Qinsong Qian, Peng Liu, Weifeng Sun, Shengli Lu, and Yangbo Yi. A high frequency isolated resonant gate driver for SiC power MOSFET with asymmetrical ON/OFF voltage. In *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, pages 3247–3251, 2017.

# Appendix A

# Altium Schematics

## A.1 Top Schematic

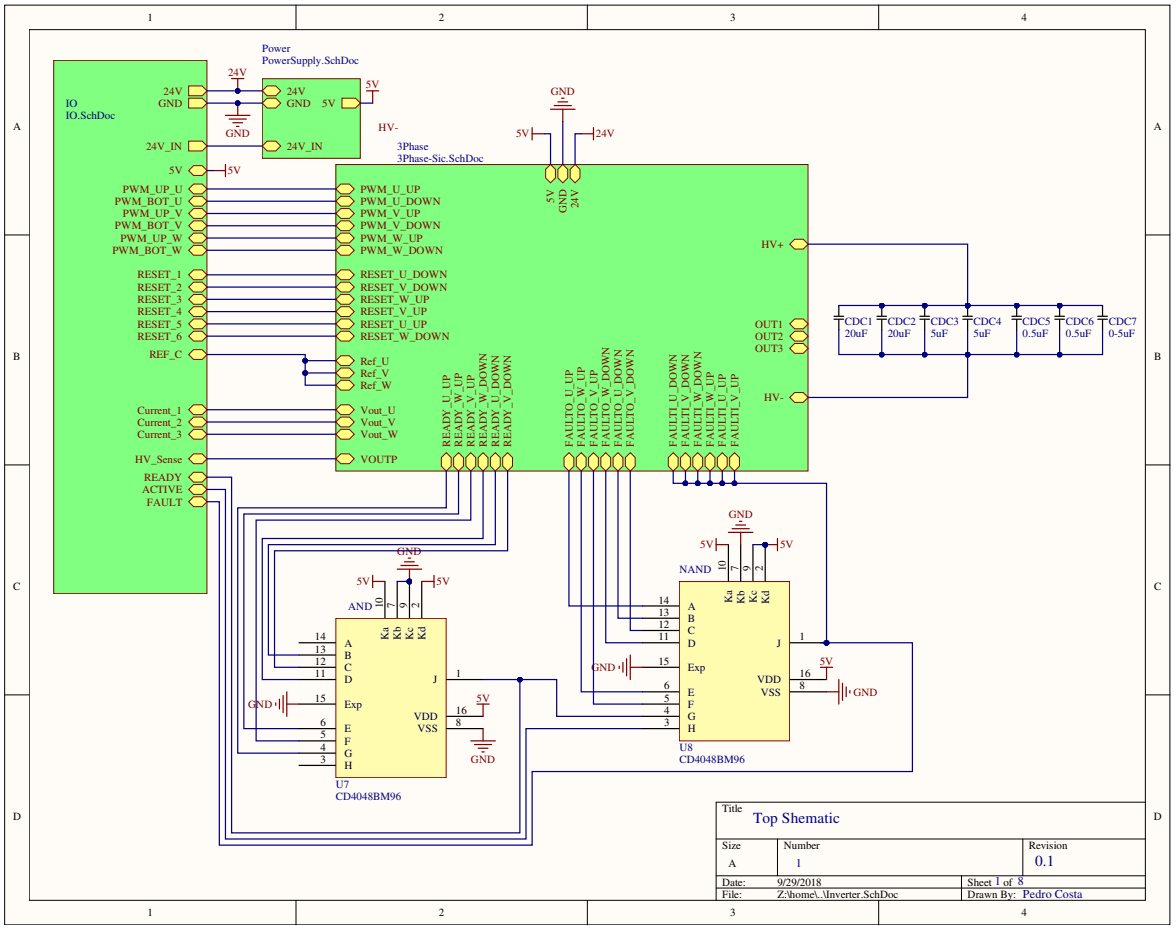



Figure A.1: Top Schematic

## A.2 Inverter Schematic

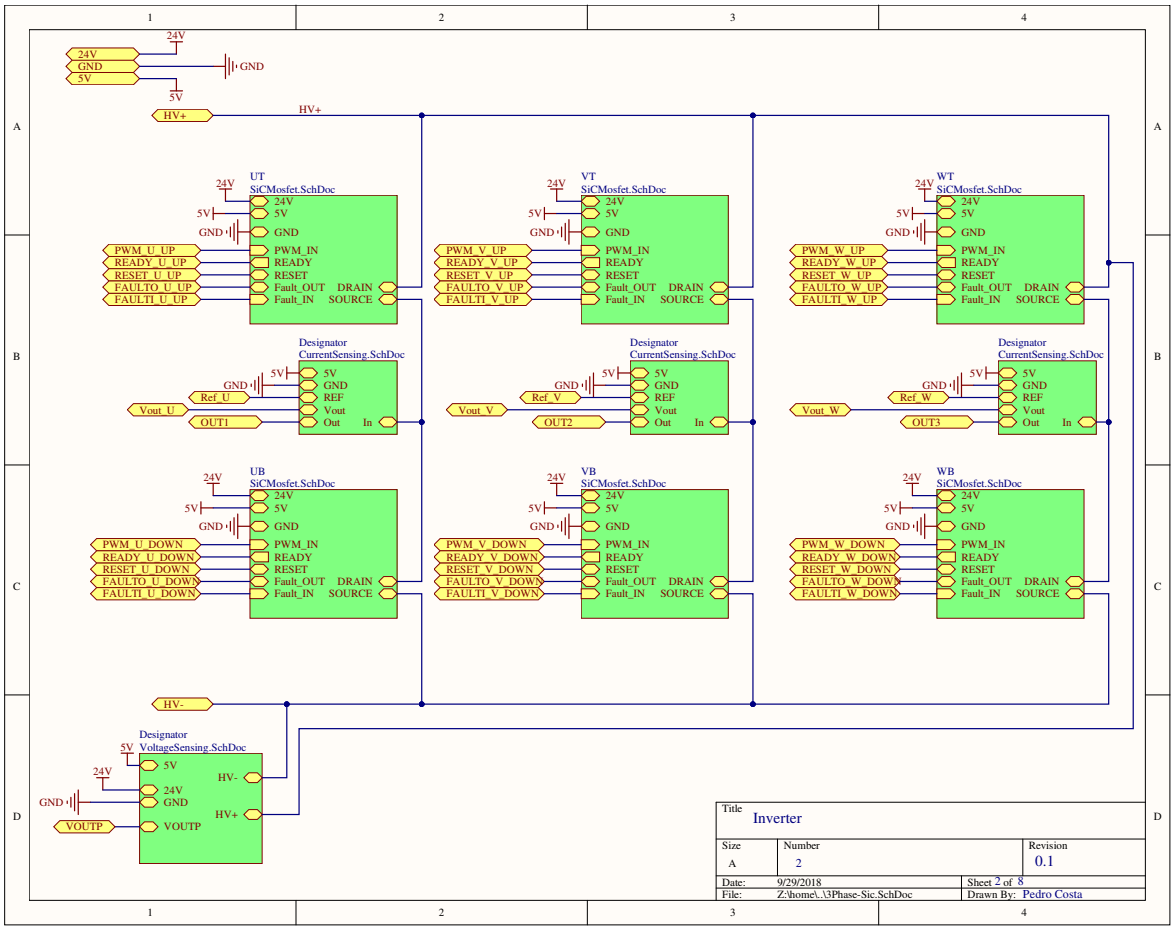



Figure A.2: Inverter Shematic

## A.3 Semiconductor Schematic

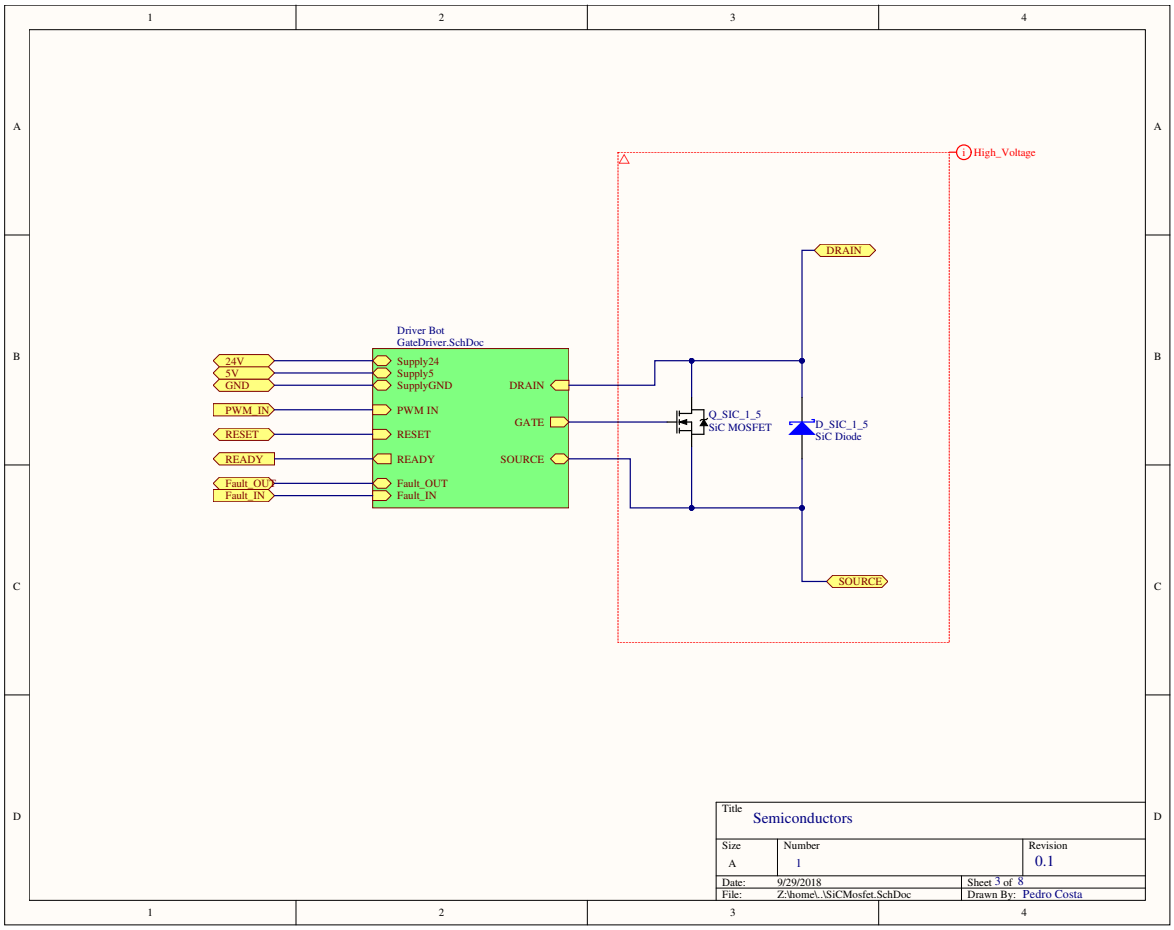



Figure A.3: Semiconductors Shematic

## A.4 Gate Driver Schematic

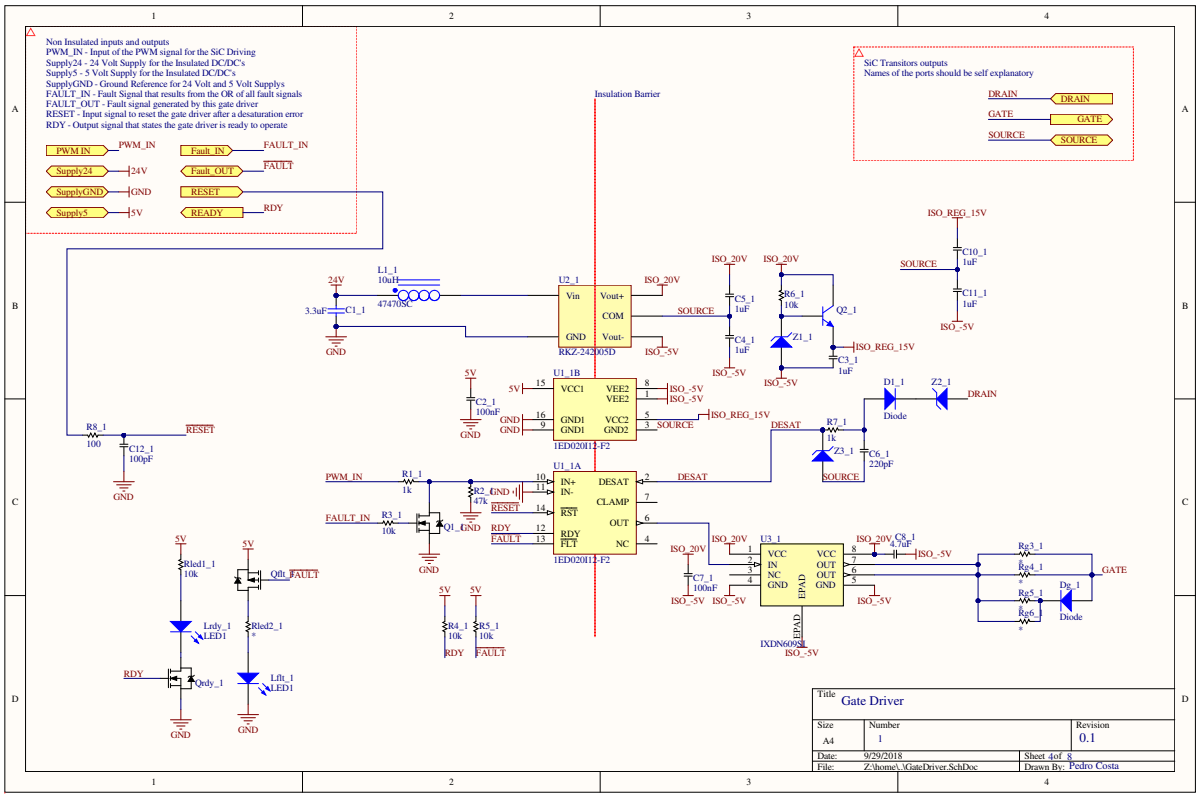



Figure A.4: Gate Driver Shematic

## A.5 Current Sensing Schematic

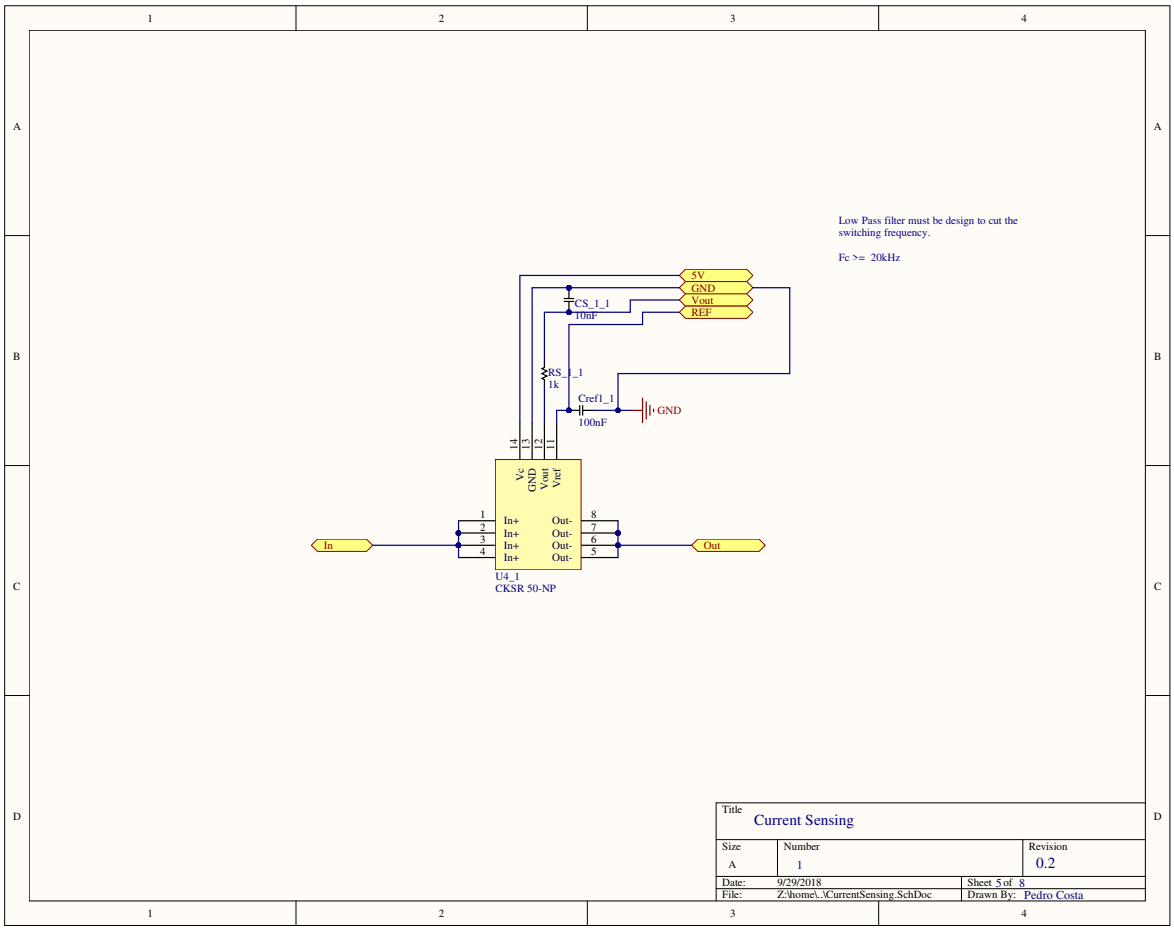



Figure A.5: Current Sensing Shematic

## A.6 Voltage Sensing Schematic

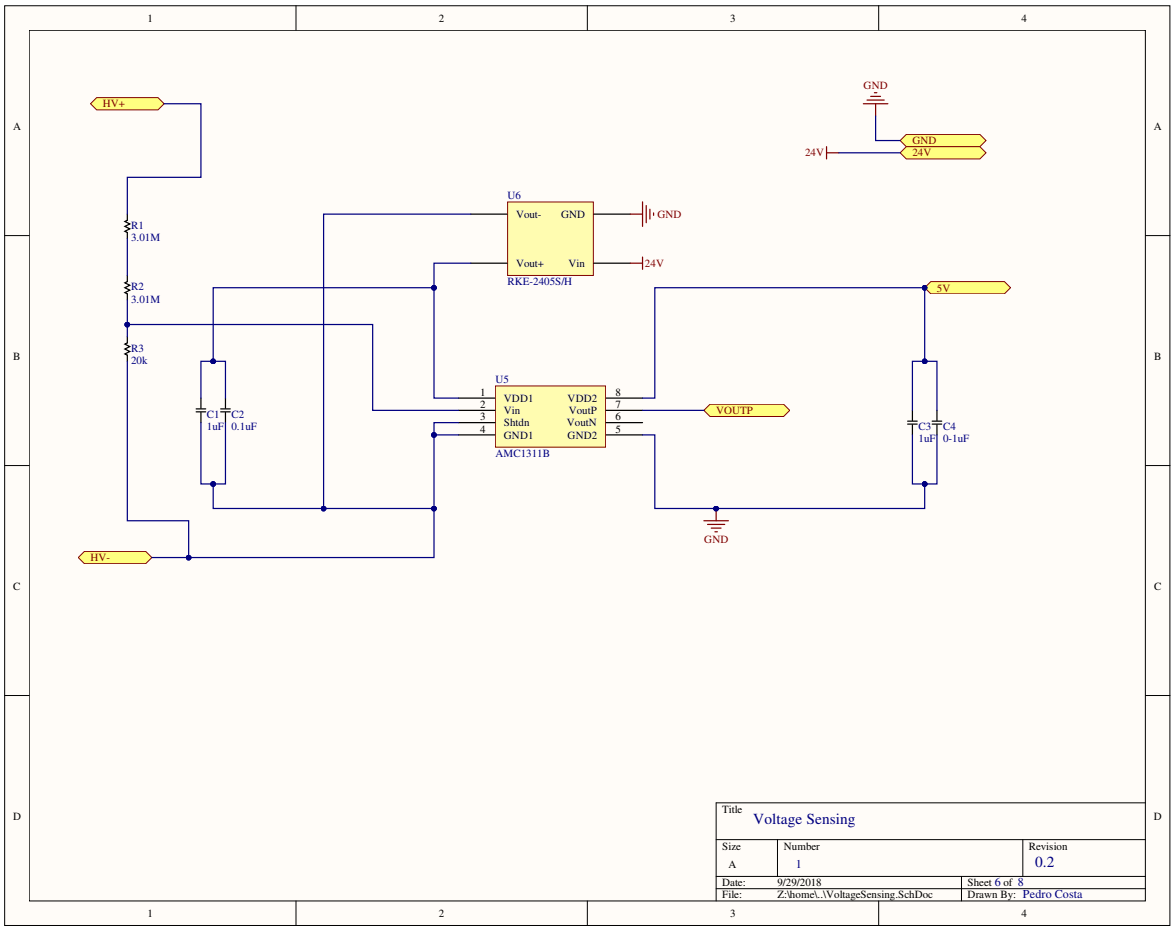



Figure A.6: Voltage Sensing Shematic

## A.7 Low Voltage Power Supply Schematic

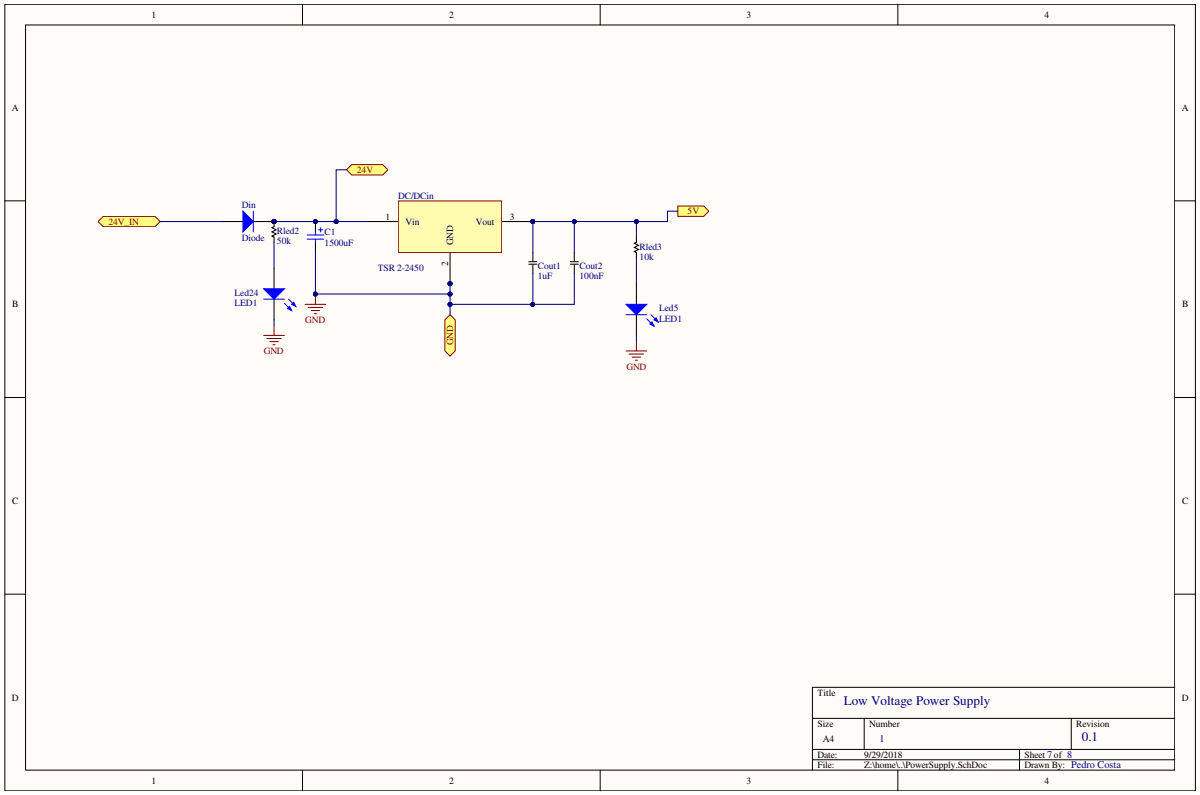



Figure A.7: Low Voltage Power Supply Shematic

## A.8 Input/Output Schematic

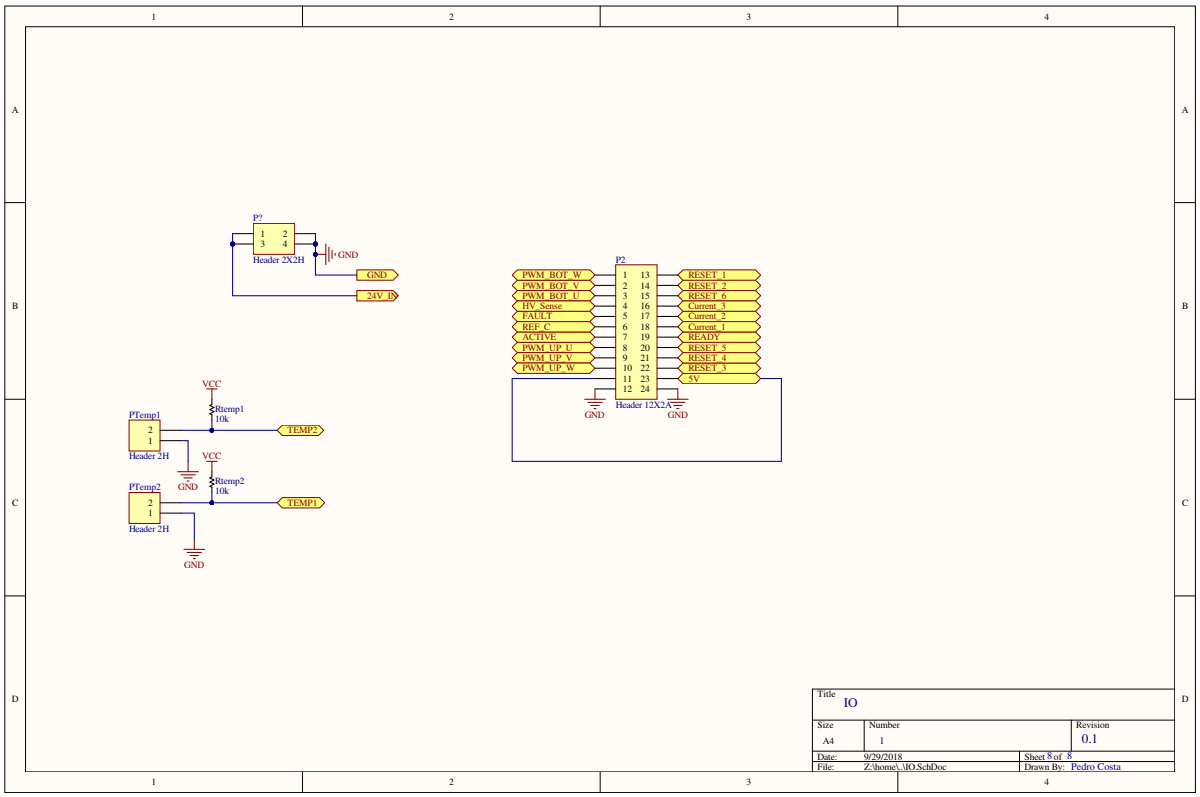



Figure A.8: Input/Output Shematic

# Appendix B

# Printed Circuits Boards Drawings

## B.1 Altium PCB Layers

## B.2 Top Layer

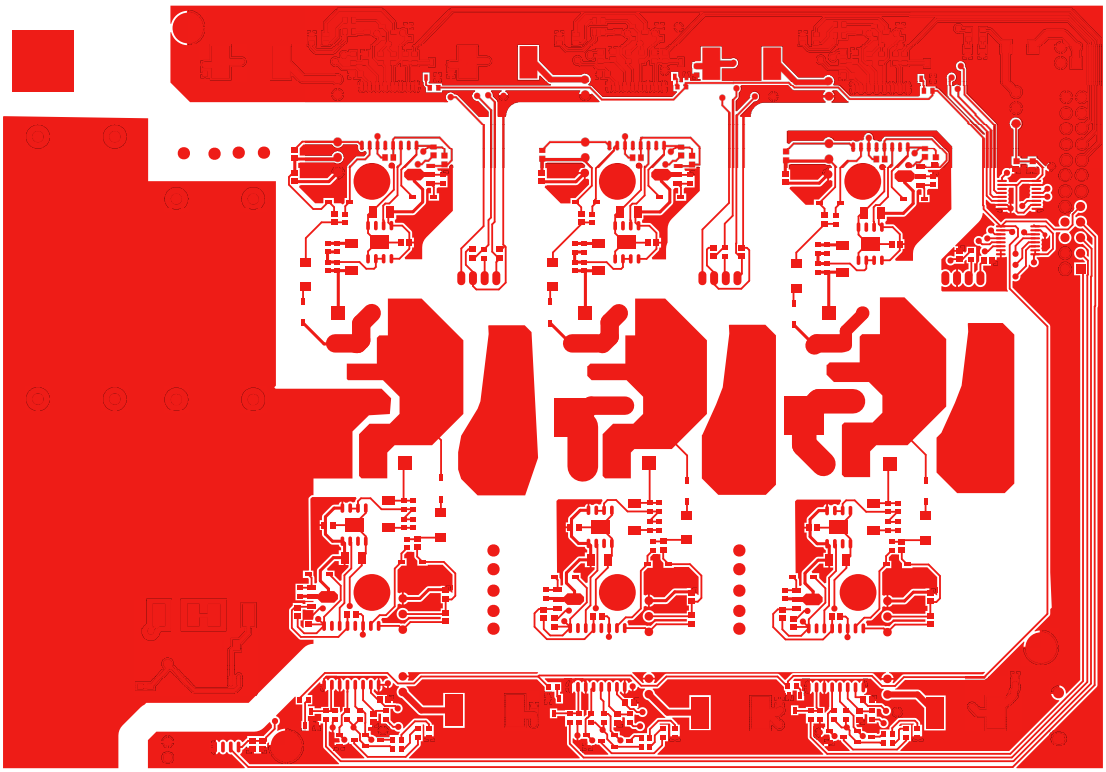


Figure B.1: Top Layer

## B.3 Bottom Layer

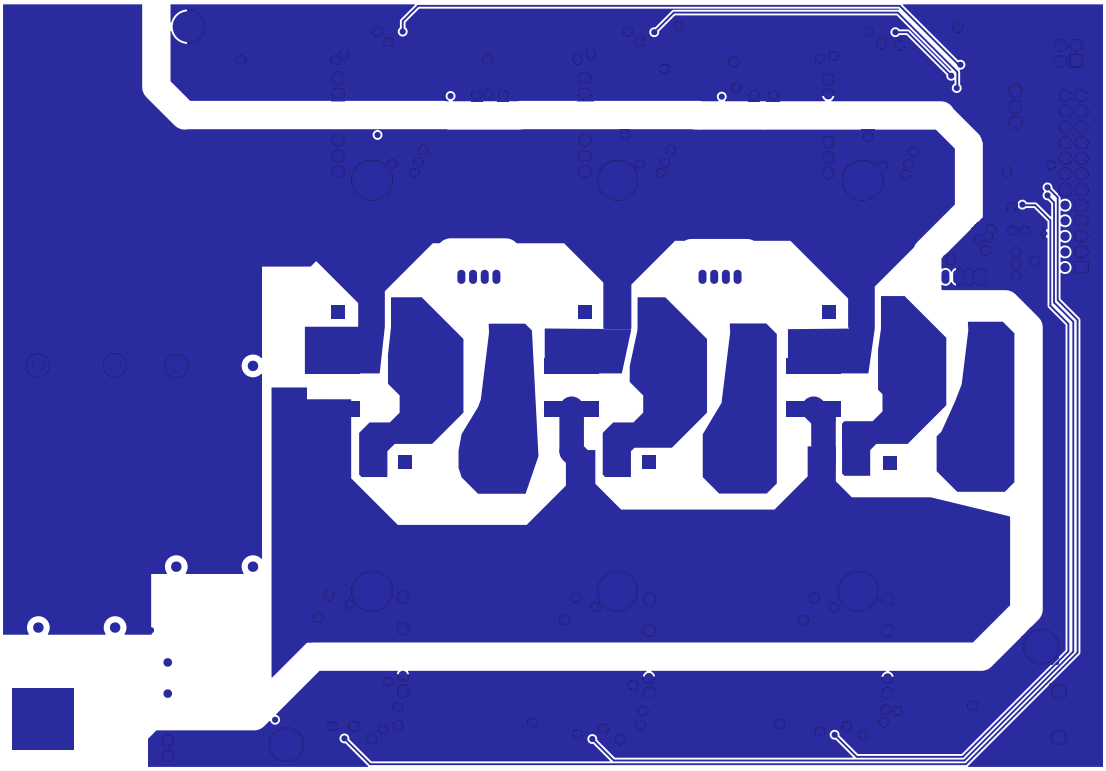


Figure B.2: Bottom Layer

## B.4 Inner Layer 1

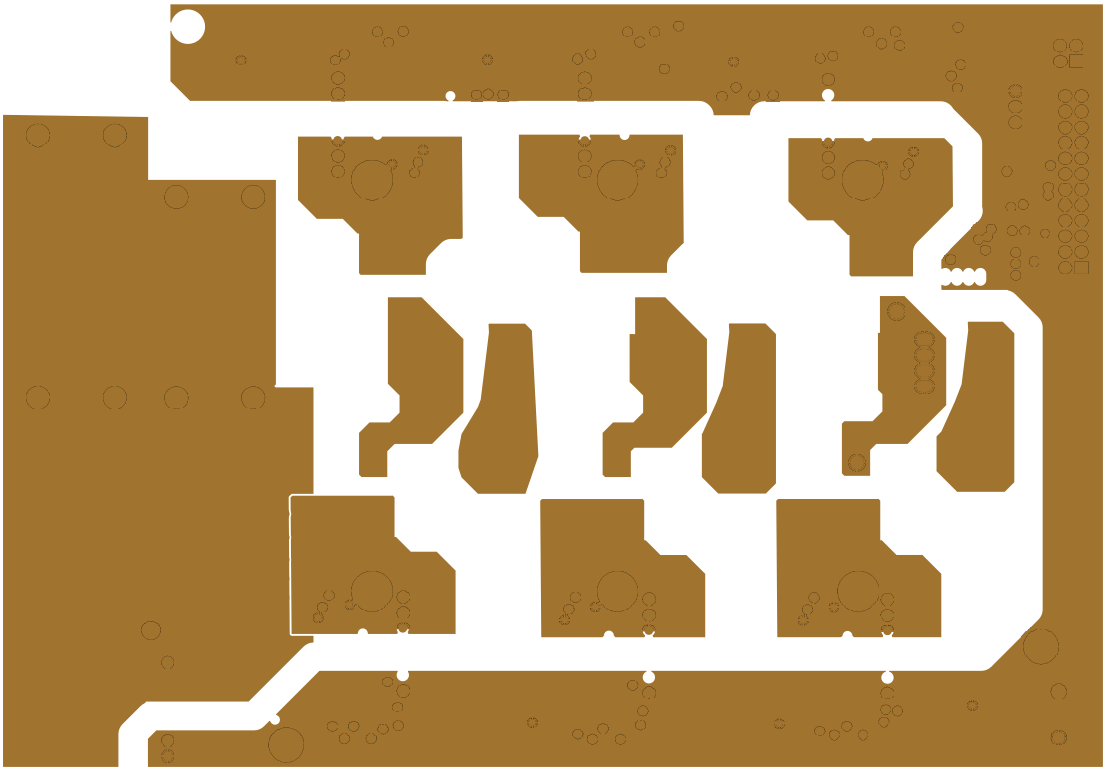


Figure B.3: Inner Layer 1

## B.5 Inner Layer 2

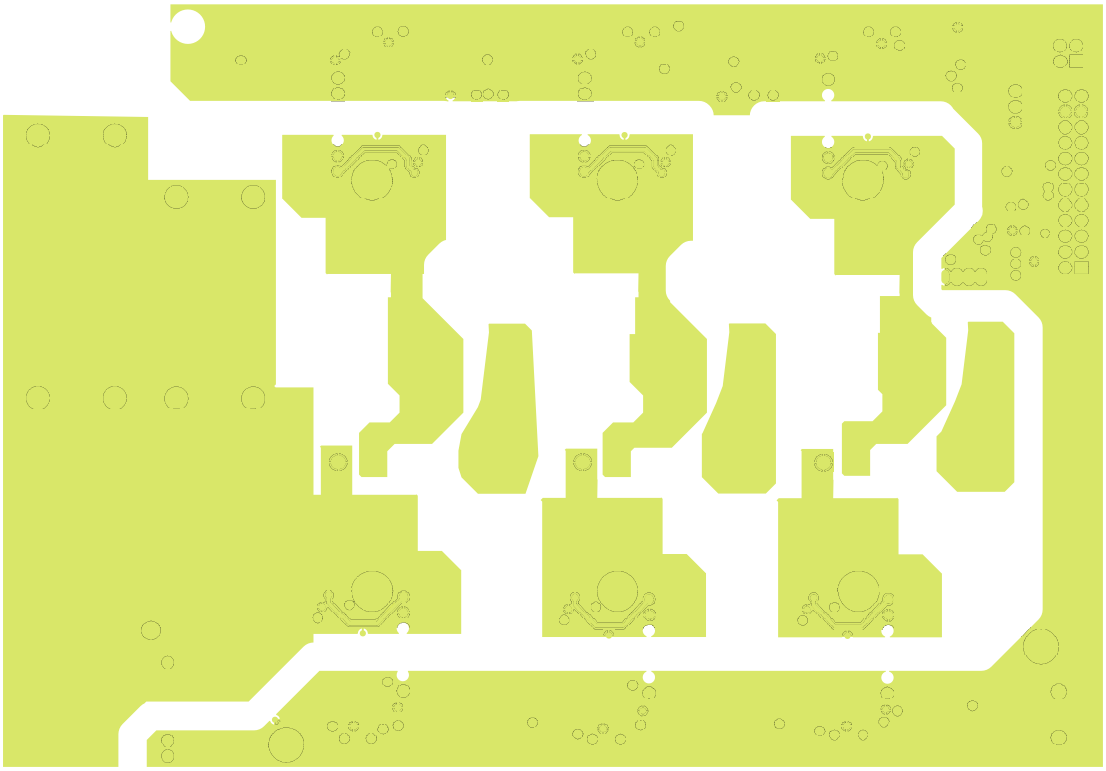


Figure B.4: Inner Layer 2

## B.6 Inner Layer 3

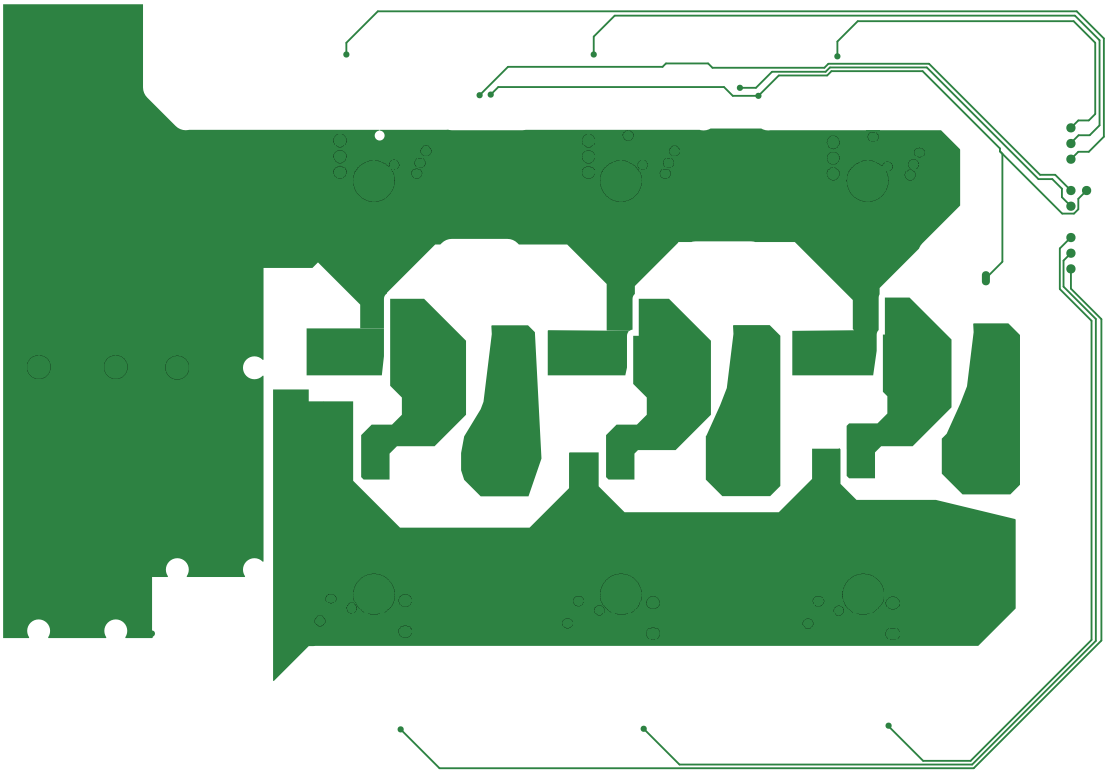


Figure B.5: Inner Layer 3

## B.7 Inner Layer 4

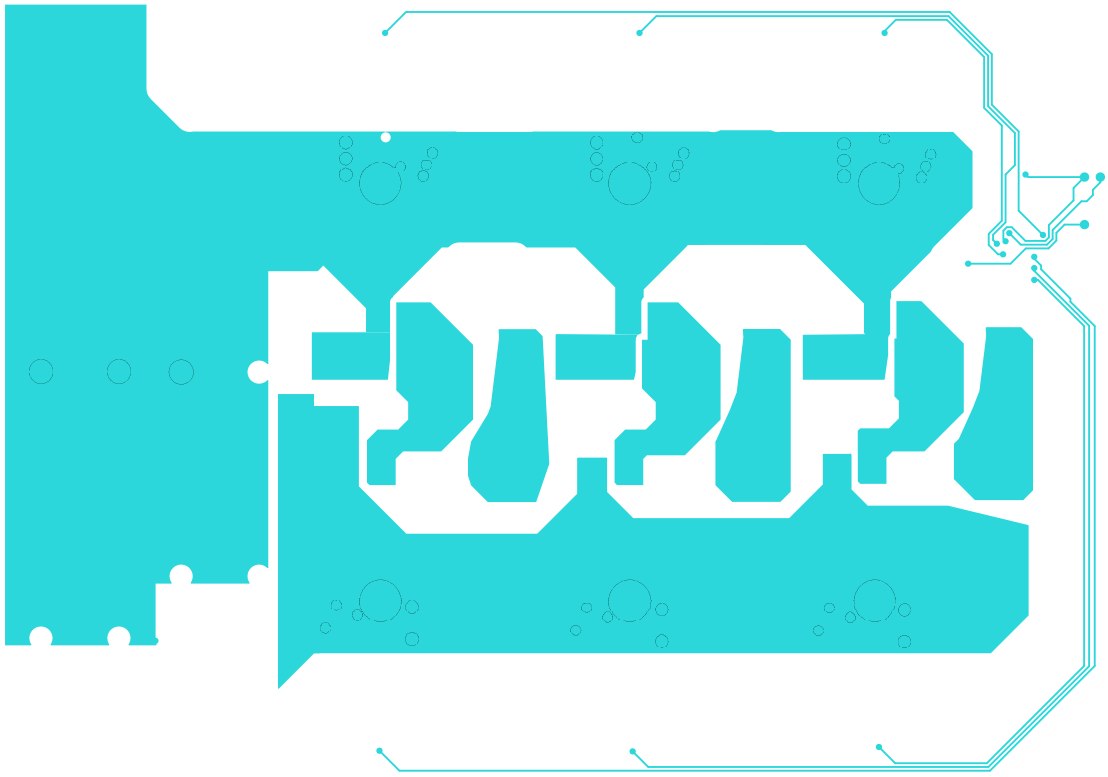


Figure B.6: Inner Layer 4

# Appendix C

# Technical Datasheets

## C.1 Technical Drawings

## C.2 Cooling Plate

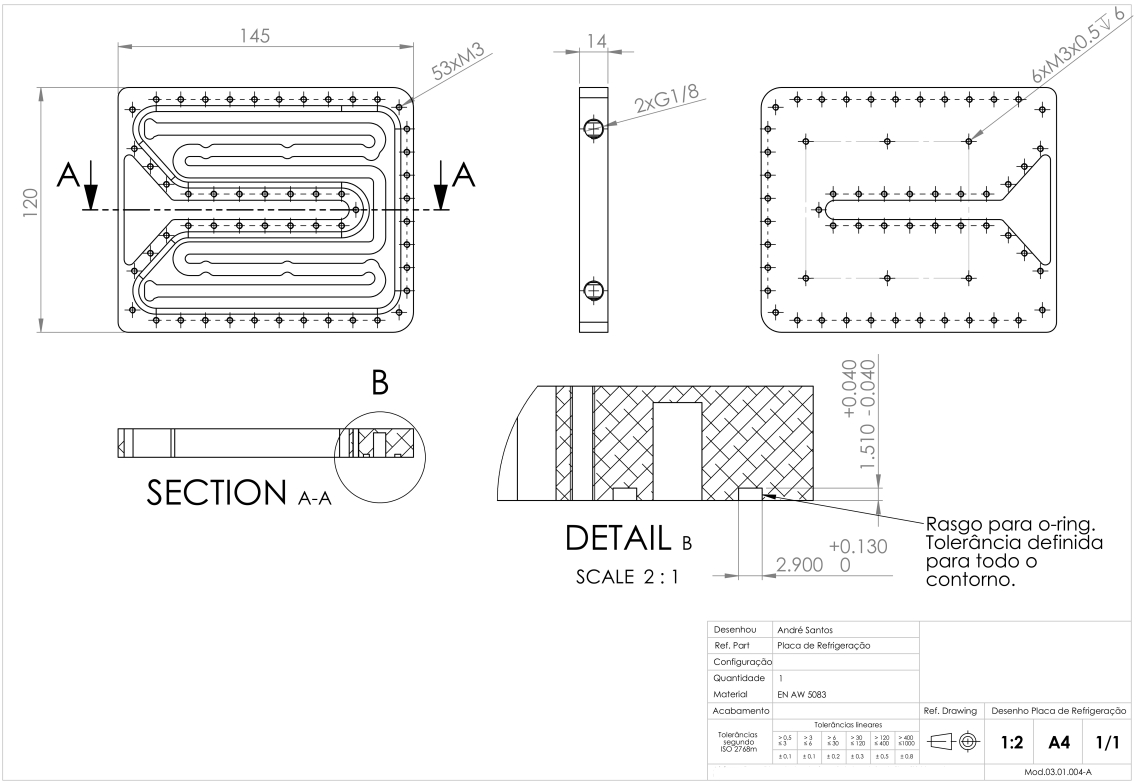



Figure C.1: Cooling Plate