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INSTITUTO SUPERIOR TÉCNICO

OPEN-END WINDING SYNCHRONOUS RELUCTANCE DRIVE BASED ON INDIRECT MATRIX CONVERTER WITH COMMON-MODE VOLTAGE REDUCTION

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Supervisor: Doctor José Fernando Alves da Silva

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Alexandre Bento, February 2023

ABSTRACT

This thesis focus in two key parts of a variable speed drive: 1) the power electronics converter topology and modulation methods, and 2) on the electrical machine itself by developing a novel Adaptive Field-Oriented Controller for Synchronous Reluctance Machines.

The power electronics converter topology under study combines an Indirect Matrix Converter with the Open-End Winding configuration of electrical machines. Such topology allows higher power density drives due to elimination of the intermediate dc-link energy storage electrolytic capacitors, which are one of the bulkier and lower lifetime components of traditional variable speed drive converters. Simultaneously by connecting the electrical machine in an Open-End Winding configuration, the Matrix converter voltage gain is increased to 1.5 eliminating one of the most prominent drawbacks, the low voltage gain, when using traditional Matrix converters to supply electrical machines. This thesis proposes a space vector modulation method for the Indirect Matrix Converter with a Dual Voltage Source Inverter output capable of reducing the Common Mode Voltage supplied to the electrical machine while improving input and output waveforms quality. In the situation where the modulated input power factor is unity, the proposed modulation method even eliminates the need for complex multistep commutation methods for switching the input stage bidirectional switches.

Regarding the control of the electrical machine, field-oriented controllers are often characterized as performing extremely well in steady state, showing lower torque ripple than other control strategies while allowing fixed switching frequency facilitating filter design. However, field-oriented controllers show poor dynamic response when exposed to drive disturbances or rapidly varying setpoints due to delays introduced by the Proportional Integral (PI) controllers used in their internal control loops. The approach proposed in this thesis eliminates the PI controllers, replacing them by adaptive non-linear backstepping controllers, whose stability is guaranteed by the Lyapunov 2nd method of stability. When compared to the traditional field-oriented controller, the proposed modified controller shows similar steady state performance and better dynamic behaviour by improving the varying speed tracking capability while achieving faster and more accurate response to the mechanical load step changes. This allows the conservation of the best steady state performance typical of traditional field-oriented controllers while achieving improved dynamic characteristic.

KEYWORDS

Indirect Matrix Converter; Open-End Windings; Synchronous Reluctance Machine; Common Mode Voltage reduction; Adaptive Field-Oriented Control

RESUMO

Esta dissertação foca-se no estudo de acionamentos eletromecânicos de velocidade variável com elevada fiabilidade e densidade de potência. Assim, o trabalho concentra-se em duas componentes fundamentais deste tipo de acionamentos: 1) a topologia e modulação do conversor eletrónico de potência, 2) o controlo por orientação de campo de máquinas síncronas de relutância.

No que diz respeito ao conversor eletrónico de potência, a topologia em estudo combina o conceito de conversores matriciais indiretos com esquemas de ligação de cargas elétricas em *open-end winding*. Esta topologia permite obter densidades de potência mais elevadas que as configurações tradicionais devido à eliminação dos condensadores eletrolíticos tipicamente utilizados no barramento de corrente contínua para armazenamento de energia de curta duração, sendo estes um dos componentes mais volumosos e com menor vida útil dos conversores eletrónicos de potência. Simultaneamente, ao utilizar a máquina elétrica num esquema *open-end winding*, o ganho de tensão do conversor matricial é aumentado para 1,5 face ao típico 0,866. Nesta dissertação, propõe-se um método de modulação por vetores espaciais para o conversor matricial indireto para cargas *open-end winding*. Este método consegue reduzir a tensão de modo comum injetada na máquina elétrica enquanto melhora a qualidade das formas de onda de entrada e saída do conversor. Na situação em que se pretende fator de potência de entrada unitário, o método de modulação elimina ainda a necessidade de métodos complexos de comutação em múltiplas etapas para a comutação dos interruptores bidirecionais do estágio de entrada.

Relativamente ao controlo da máquina síncrona de relutância, os controladores por orientação de campo são frequentemente caracterizados por terem um muito bom desempenho em regime permanente comparativamente a outras estratégias de controlo por apresentarem menor ondulação de binário e permitirem funcionamento a frequência de comutação fixa facilitando o projeto do filtro de entrada. Por outro lado, os controladores por orientação de campo são comummente criticados devido a proporcionarem respostas lentas aquando variações abruptas de carga ou de referências de velocidade devido aos atrasos introduzidos pelos controladores proporcionais integrais utilizados nas suas cadeias de controlo. A abordagem proposta neste trabalho consiste na substituição dos controladores proporcionais integrais por controladores adaptativos não lineares com *backstepping*, cuja estabilidade é garantida pelo segundo método de estabilidade de Lyapunov. Quando comparado com os controladores por orientação de

campo tradicionais, o controlador proposto consegue manter o excelente desempenho em regime permanente, enquanto permite obter uma melhoria significativa na performance dinâmica do acionamento de velocidade variável, apresentando melhores resultados em cenários de seguimento de referências de velocidade e em variações abruptas da carga mecânica aplicada ao eixo da máquina.

PALAVRAS-CHAVE

Conversor Matricial Indireto; Open-End Winding; Máquina Síncrona de Relutância; Tensão de Modo Comum; Controlo por Orientação de Campo Adaptativo

SYMBOL TABLE

Symbols

b	SynRM viscous friction coefficient divided by SynRM constant of inertia
CMV	Common Mode Voltage at the IMC output
C_f	IMC input filter capacitance (delta connection)
$\mathbf{C}$	Power Invariant Concordia Transformation
d	SynRM mechanical load torque divided by SynRM constant of inertia
e_ω	SynRM speed error
e_I	Integral of SynRM speed error in time
e_T	SynRM electromagnetic torque error
e_d	SynRM d axis current error
e_q	SynRM q axis current error
E_{sw}^R	Energy lost due to one switching (turn ON and turn OFF) obtained from catalogue at reference voltage (V^R) and current (I^R) for the GaN HEMT
E_{sw}	Energy lost due to one switching (turn ON and turn OFF) for the GaN HEMT
I^R	Reference current (I^R) for the GaN HEMT obtained from the manufacturer catalogue for computation of Energy lost due to one switching
i_A, i_B, i_C	IMC output currents
i_d, i_q, i_z	SynRM stator currents in the dqz rotor reference frame
$\mathbf{i_o}$	IMC output current vector
i_a, i_b, i_c	Electrical grid currents
i_{sa}, i_{sb}, i_{sc}	IMC input currents
i_{dc}	IMC soft dc-link current
J	SynRM constant of inertia
k_D	SynRM viscous friction coefficient
k_ω	Proportional gain of the Proposed Lyapunov speed controller
k_I	Integral gain of the Proposed Lyapunov speed controller
k_d	Proportional gain of the Proposed Lyapunov d axis current controller
k_q	Proportional gain of the Proposed Lyapunov q axis current controller
L_d, L_q, L_z	SynRM inductances in the dqz rotor reference frame
L_{lk}	SynRM leakage inductance
L_f	IMC input filter inductance
N_{sw}	IMC output stage upper switches turned ON

p	SynRM number of pole pairs
P_{sw}	IMC switching losses
P_{cond}^{CSR}	IMC input stage conduction losses
P_{cond}^{DVSI}	IMC output stage conduction losses
R_f	IMC input filter damping resistor
R_{ds}	Drain to Source resistance of the GaN HEMT device
R_s	SynRM stator winding resistances
S_{a+}, S_{b+}, S_{c+}	State of the IMC input stage upper bidirectional switches
S_{a-}, S_{b-}, S_{c-}	State of the IMC input stage lower bidirectional switches
$\mathbf{S_{CSR}}$	IMC input stage switching states matrix
$\mathbf{S_{DVSI}}$	IMC output stage switching matrix
S_{A1u}, S_{B1u}, S_{C1u}, S_{A2u}, S_{B2u}, S_{C2u}	State of the IMC output stage upper semiconductors
S_{A1d}, S_{B1d}, S_{C1d}, S_{A2d}, S_{B2d}, S_{C2d}	State of the IMC output stage lower semiconductors
T_e	SynRM electromagnetic torque
T_{load}	SynRM mechanical load torque
T_{rls}	RLS algorithm sampling time
T_s	Simulation time step
T_{sw}	SVM switching period
V_0	Lyapunov function for speed control without load torque estimation
V_1	Lyapunov function for speed control with load torque estimation
V_2	Lyapunov function for q axis current control with backstepping
V_3	Lyapunov function for d axis current control with backstepping
V^R	Reference voltage (V^R) for the GaN HEMT obtained from the manufacturer catalogue for computation of Energy lost due to one switching
v_{A1}, v_{A2}, v_{B1}, v_{B2}, v_{C1}, v_{C2}	IMC output arm voltages to ground
v_{A10}, v_{A20}, v_{B10}, v_{B20}, v_{C10}, v_{C20}	IMC output arm voltages to the dc-link midpoint
v_a, v_b, v_c	Electrical grid phase to ground voltages
v_A, v_B, v_C	IMC output phase voltages
$\mathbf{V_o}$	IMC output voltage vector
$\mathbf{V_o}^*$	IMC output voltage reference vector
v_d, v_q, v_z	SynRM stator voltages in the dqz rotor reference frame
v_{sa}, v_{sb}, v_{sc}	IMC input phase to ground voltages

v_{sd}, v_{sq}, v_{sz}	IMC input voltages in the *dqz* reference frame, synchronized with θ_s
$V_{ph\ rms}$	IMC root mean square value phase-to-phase input voltage
v_{dc}	IMC soft dc-link instantaneous voltage
V_{dc}	IMC soft dc-link average voltage during a full switching cycle
v_p	IMC dc-link '*p*' busbar to ground voltage
v_m	IMC dc-link '*m*' busbar to ground voltage
v_0	IMC soft dc-link midpoint to ground voltage
v_G	Instalation ground voltage
v_{0G}	IMC input stage contribution to Common Mode Voltage
v_{cm0}	IMC output stage contribution to Common Mode Voltage
α_i	SynRM current angle
$\boldsymbol{\alpha}$, $\boldsymbol{\beta}$, $\boldsymbol{\gamma}$	Unitary vectors of the Concordia reference frame
γ_d	Lyapunov controller gain for mechanical load torque estimation
δ	SynRM load angle
δ_ρ^R , δ_σ^R	IMC input stage duty cycles for vectors ρ and σ
δ_κ^I , δ_λ^I , δ_o^I , δ_{o1}^I , δ_{o2}^I	IMC output stage duty cycles for vectors κ, λ, o, o1 and *o2*
ζ	Damping ratio
θ_m	SynRM rotor angle in respect to stator phase *a* winding
θ_e	SynRM electrical angle in respect to stator phase *a* winding
θ_i	CSR input current phase reference
θ_s	CSR input voltages phase
κ	IMC output stage Active vector applied first in the SVM switching period
λ	IMC output stage Active vector applied second in the SVM switching period
ξ	SynRM saliency ratio
o	IMC output stage Null vector in the SVM switching period (DVSI group II vectors SVM strategy)
o1	IMC output stage Null vector applied first in the SVM switching period (DVSI group I vectors SVM strategy)
o2	IMC output stage Null vector applied second in the SVM switching period (DVSI group I vectors SVM strategy)
ρ	IMC input stage vector applied first in the SVM switching period
σ	IMC input stage vector applied second in the SVM switching period
ϕ_i	IMC modulated current-to-voltage displacement angle

φ_{ref}^{R}	IMC input stage reference phase for duty cycles computation
φ_{ref}^{I}	IMC output stage reference phase for duty cycles computation
ψ_d, ψ_q, ψ_z	SynRM stator flux linkages in the *dqz* rotor reference frame
ω_e	SynRM electrical velocity
ω_m	SynRM mechanical velocity

ACRONYMS

AC – Alternated Current

CMV – Common Mode Voltage

CSR – Current Source Rectifier

DC – Direct Current

DMC – Direct Matrix Converter

DTC – Direct Torque Control

DVSI – Dual Voltage Source Inverter

EMI – Electromagnetic Interference

EV – Electric Vehicle

FEA – Finite Element Analysis

FOC – Field Oriented Control

FPGA – Field Programmable Gate Array

GaN – Gallium Nitride

HEMT – Hight Electron Mobility Transistor

IM - Induction Machine

IC – Integrated Circuit

IM - Induction Machine

IMC – Indirect Matrix Converter

IMD – Integrated Motor Drive

LUT – Look up table

MPC – Model Predictive Controller

MPF – Maximum Power Factor

MTPA – Maximum Torque per Ampere

MTPkVA – Maximum Torque per kilo Volt-Ampere

MTPV – Maximum Torque per Volt

OEW – Open-End Winding

PI – Proportional Integral Controller

PMSM – Permanent Magnet Synchronous Machine

PWM – Pulse Width Modulation

RLS – Recursive Least Squares

Si – Silicon

SiC – Silicon Carbide

SoC – System on a Chip

SVM – Space Vector Modulation

SynRM – Synchronous Reluctance Machine

THD – Total Harmonic Distortion

VSD – Variable Speed Drive

VSI – Voltage Source Inverter

WBG – Wide-bandgap

ZSC – Zero sequence currents

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CHAPTER 1

INTRODUCTION

1.1 – Research Background

The global energy sector is going through a major transformation, where sustainability is the long run objective. The future milestones are different for every region and country, but the European Commission has already committed to achieve net-zero greenhouse gas emissions by 2050 [1]. In the European commission vision, for this to be possible, the electric power sector must play a much greater role in the final energy demand than it does nowadays and be largely based on renewable energy sources, complemented by nuclear power [2]. This will have an impact not only on how the electrical energy is generated, but also on how it is transported, distributed, consumed, and stored for later use [3]–[5].

On the energy generation side, the last two decades in the electric power sector were marked by a rapid and strong increase in the penetration of energy originated from non-traditional renewable energy sources such as wind and solar [5]. The industrial sector is seeing traditional fixed speed applications being replaced by variable speed systems due to its higher efficiency, improved performance, and increased system integration [6]–[9]. On the other hand, the transportation sector also represents a relevant fraction of the global CO_2 emissions, thus a significant part of transportation should become fully electric [10].

This continually growing demand in variable speed electric drives for such a large variety of applications greatly motivates research interest in topics related to electronic power converter topologies and its control, electrical machines design and its control and on semiconductors technologies [11], [12].

1.1.1 – Variable Speed Electric Drives

The typical state of the art structures of grid connected low voltage variable speed electric drives (VSD) are shown in Fig. 1.1. These structures can allow power to flow unidirectionally as

shown in Fig. 1.1(a) or with reversible power flow capability as shown in Fig. 1.1(b). The drive structure includes a grid connected rectifier stage responsible to guarantee direct current (DC) voltage at one or more DC - link capacitors. In the case of the bidirectional power flow converter of Fig. 1.1(b), it is often constituted by the association of two voltage source inverters (VSI) in a back-to-back configuration, allowing sinusoidal input alternated current (AC) currents at a convenient, adjustable power factor and controllable DC-link voltage. This stage is followed by the drive inverter stage that feeds the desired voltage waveform to a three-phase AC machine. The voltage waveform is a high frequency pulsed voltage with half-wave symmetry obtained from the DC-link voltage through a suitable modulator. Typically, due to practical reasons, the rectifier and inverter stages are placed inside a cabinet that is often relatively distant to the electric machine location. This adds a third element to the system, a cable to connect the inverter stage to the AC machine. The effects of the high frequency pulsed voltage waveform on the cable are strongly dependent on the cable length. The high frequency peak voltage at the machine terminals can be twice as high as the voltage at the output of the inverter stage which can damage the machine windings isolation and add extra electromagnetic interference (EMI) problems [13]. There are reported cases of direct grid connected machines operating for years without problems, but start failing when supplied from a electronic power drive [14]. A solution may be to place a filter at the input of the AC machine, or at the output of the power converter. However, the filter brings additional cost, losses, space requirements and adds complexity to the installation project due to the cable length dependence [15].

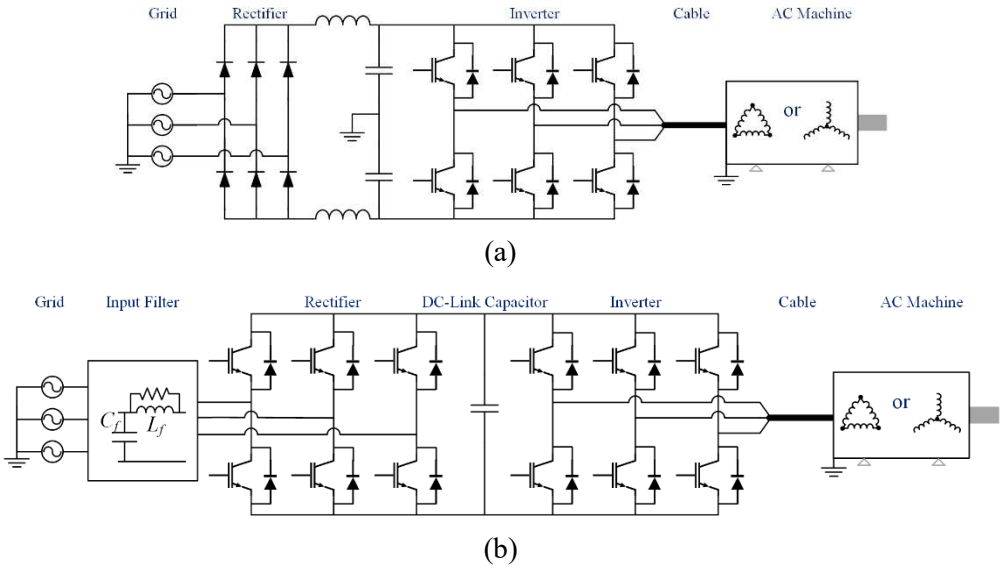


Fig. 1.1. Typical grid-connected variable speed drives: (a) for unidirectional power flow featuring a diode rectifier in the input stage (b) for bidirectional power flow, featuring two VSIs in a back-to-back configuration.

Another well-known issue in power electronic converter fed electric machines is the existence of bearing currents that in some cases lead to premature bearing failure [16]. A detailed study on bearing currents causes was performed in [17] where the inverter output common mode voltage (CMV) is concluded to be the source of inverter-induced bearing currents in power converter fed electric machines. These currents appear due to CMV exciting the capacitive couplings between different parts of the electrical machine leading to four different forms of currents. Capacitive bearing currents and electric discharge machining currents are related to the influence of CMV on the bearing voltage, while circulating bearing currents and rotor ground currents appear as result from the interaction of rapid variations of CMV and the stray capacitance between stator windings and motor frame. Generally, the parasitic capacitive couplings between machine parts are known as stray capacitances and are shown in Fig. 1.2, as the winding-to-frame capacitance (C_{wf}), the winding-to-rotor capacitance (C_{wr}), and the rotor - to - frame capacitance (C_{rf}) and bearing capacitance (C_b).

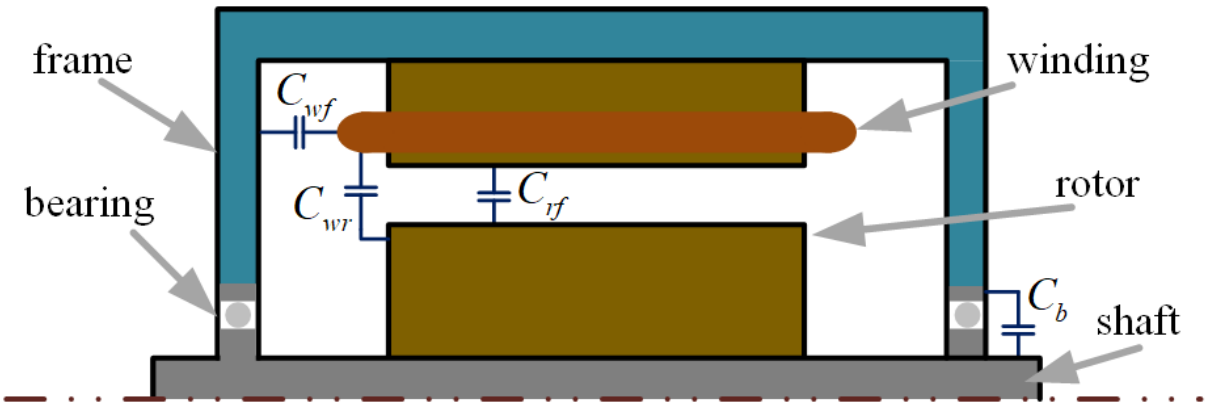


Fig. 1.2. Cross-sectional cut of an AC machine with indication of stray capacitances that originate bearing currents in the presence of high frequency CMV.

Even though different forms of bearing currents vary on impact according to the power level and speed ranges of the electric machines, it has been concluded that reducing the CMV either by filtering it [18], or by actively reducing its occurrence by developing new modulation schemes [19][20], are both effective countermeasures on the inverter side to reduce bearing currents and its impact in the electric drive lifespan [17].

1.1.2 – The Path for Integrated Motor Drives

With the new and more demanding applications for variable speed electric drives, over the last decade there has been a shift in interest, from the traditionally separated subsystems (drive, cable and motor) of the electric drive, to a more compact, efficient, and robust solution often named Integrated Motor Drive (IMD) [21]. The concept is opportune, with some prototypes demonstrated in the literature [22]–[26]. By integrating power converters and cables into the motor, it is possible to achieve a plug and play drive with increased power density and efficiency at lower cost, when compared with the traditional solution featuring separated machine and converter drive [21], [27].

Although the IMD concept is extremely attractive, the integration of the needed subsystems is very challenging. Not only the space inside an electrical machine is quite limited, but also the inherent harsh thermal conditions and constant mechanical vibrations are far from being ideal for the traditional drive components [27]. In terms of converter topologies, the typical back-to-back topology requires a bulky DC-link electrolytic capacitor that is not only hard to fit inside the machine but also limited to a maximum operating temperature typically around 120ºC [21].

Presently, most of the IMD literature is focused on electric vehicles (EV) and explores converter topologies with modular approaches that can reduce the required dc-link capacitance allowing the replacement of the electrolytic capacitors by film capacitors. This is achievable as the EVs power source is a battery, requiring a DC-link capacitance smaller when compared with a grid connected system. For grid connected applications, a different approach may be required. In [28], a grid connected IMD is accomplished by increasing the switching frequency, reducing the required DC-link capacitance. Still, most of the occupied drive volume is due to the passive components of both the input filter and DC-link capacitance. The authors of [29] thought of a different approach, a 30kW grid connected IMD without dc-link is developed by taking advantage of direct AC-AC conversion, a characteristic of matrix converters [30].

Matrix converters are a class of power converters that allow direct AC-AC conversion with minimal passive components requirements by being mainly based on semiconductors. There is extensive literature on this class of converters, mainly in topological variations, their control and modulation methods [31]. Although not requiring a dc-link capacitor while featuring the capability of obtaining input sinusoidal currents at adjustable power factor, their reduced voltage transfer ratio, increased number of semiconductors and control complexity are issues limiting their industrial applications [32]. However, since direct AC-AC conversion inherently

solves one of IMDs challenges, and by being able to achieve unparalleled power densities with high potential for modularity, matrix converters may represent an extremely viable solution for future generalization of grid connected IMDs.

In the search for more robust drives, significant effort has been done in the literature to develop topologies and modulation strategies with reduced CMV. Due to its improved fault tolerance, higher input to output voltage ratio, multilevel operation capability and higher reliability, the concept of open-end winding (OEW) configurations has caught the interest from several researchers, especially in DC-supplied systems. Authors of [33]–[36] focused on modulation methods for OEW converters supplied by a single DC-source, focusing on the suppression of zero sequence currents. In [37], a modulation method for a five-phase OEW drive supplied by two isolated DC-sources is proposed, allowing up to 17 levels of output voltage to be supplied to the load. The authors of [38] proposed a reconfigurable OEW topology with 4 isolated DC supplies that offer the possibility to vary the number of machine phases and number of poles (from 3 phases and 12 poles to 9 phases and 4 poles) during operation.

Regarding AC-supplied drives, the association of direct AC-AC conversion and OEW configurations has been receiving much attention in recent variable speed electric drives literature, as the association has the potential to mitigate one of the major drawbacks of matrix converters, the low voltage gain.

Considering the development of semiconductor technologies, the last decade was marked by a very significant number of research works on power electronic converters based on wide-bandgap (WBG) semiconductors [39]. WBG devices are a new generation of power devices that provide significant benefits over the traditional Silicon (Si) semiconductors and are presently commercially available. Within the group of WBG materials, Silicon Carbide (SiC) and Gallium Nitride (GaN) currently show the best trade-off between theoretical characteristics, commercial availability, and maturity of their technological processes [40]. WBG devices can operate with higher current density, faster switching at higher frequencies, with lower losses and under higher temperatures when compared with Si devices [40], [41]. Some authors consider that SiC will become the most suitable devices for high power applications above 1000V/1200V, while GaN will dominate the high frequency applications under that voltage level [21], [42], [43]. In variable speed electric drives, their capabilities of withstanding high current densities, higher temperatures and increased switching frequencies are favourable characteristics to achieve increased power density and efficiency of electric drives and will be part of the solution for IMD generalization [21], [44]. On the other hand, faster switching

characteristics result in higher *dv/dt* and *di/dt* that will amplify the previously mentioned effects of bearing currents, windings isolation aging and EMI [21], [44]. This enhances the future role of power electronics converter topologies and modulation techniques that allow multilevel operation and CMV reduction.

Regarding the electrical machine itself, in the past years the Synchronous Reluctance Machine (SynRM) has attracted great interest not only in the research community but also in industry, with ABB, KSB and Siemens releasing their line of SynRM drives, in some cases featuring efficiency classes IE4 (Super-Premium) and IE5 (Ultra-Premium) according to IEC600034-30-1 and IEC60034-30-2.

SynRM has been around for almost a century but did not get much attention in the past due to its poor power factor, low efficiency when directly fed from the grid and complex rotor design [45]–[47]. The usage of Finite Element Analysis (FEA) to design the machine greatly simplified the complex rotor analysis [48]. Also, when appropriately associated to a power electronic converter, the SynRM can achieve higher efficiencies than induction machines due to the absence of rotor currents [48], [49]. Although SynRM cannot achieve the efficiency and power density of Permanent Magnet Synchronous Machines (PMSM), SynRM does not rely in rare-earth materials. This detail became important after the incident in the early 2010 to mid-2011, when the price of rare-earth metal neodymium skyrocketed by a factor greater than 20:1 [50]. After this, significant research effort has been conducted in SynRM assisted by rare-earth free magnetic materials, such as ferrite, for applications where efficiency and power density are crucial [47], [50]. The SynRM is characterized by having a low cost and cold rotor structure due to the absence of rare-earth materials, windings, and currents in the rotor [47], [49]. These characteristics sound ideal for integration of the drive components into it, thus SynRM is a very good machine candidate for IMD. A detailed analysis of SynRMs is performed in chapter 3 of this thesis.

1.1.3 – Matrix Converters and its contribution towards innovation in electrical drives

Matrix converters allow direct AC-AC conversion, thus eliminating the need for intermediate energy storage used by back-to-back converters to decouple the dynamics of both input and output electrical quantities [51]. In other words, the input currents of a matrix converter are a filtered arrangement of the instantaneous output currents while the output voltages are

composed by arrangements of the instantaneous grid voltages, synthetized at a switching frequency much higher than both the input and output frequencies.

Matrix converters can be divided into two categories, single-stage or Direct Matrix Converters (DMC) and dual-stage or Indirect Matrix Converters (IMC). Within these categories, several topological variations have been proposed and extensively discussed in the literature [52]. The most common structures of both DMC and IMC families are presented in Fig. 1.3.

To achieve bidirectional power flow, matrix converters require bidirectional power semiconductor switches. These switches can operate at high frequency in the four-quadrants, by allowing control of current flow in both directions and providing capability of blocking positive and negative voltages.

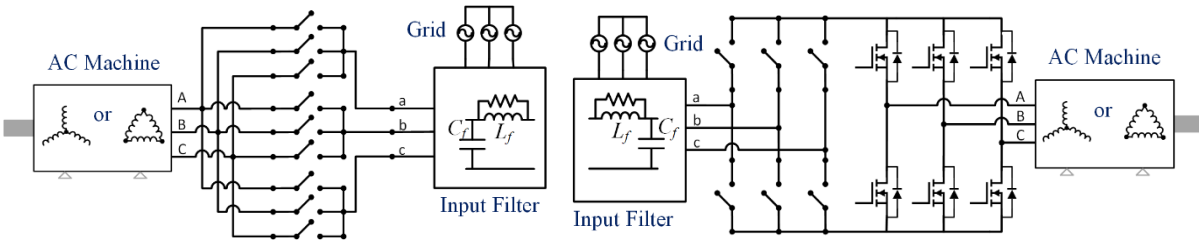


Fig. 1.3. Most common structures of the two matrix converter topologies categories. (a) DMC. (b) IMC.

Some of the possible configurations for 4-quadrant bidirectional switches are given in Fig. 1.4. The most common configurations are both the common collector and common emitter IGBT association with their corresponding antiparallel diodes, Fig. 1.4 (a) and Fig. 1.4 (b) respectively. With the growth of interest in WBG devices, there are already works reporting efficiency and power density gains by using SiC MOSFETs in a common source association instead of Si IGBTs, Fig. 1.4 (c) [53], [54]. The GaN Bidirectional switch device shown in Fig. 1.4 (d), is presented in [55] and [56] as a possible game changer for matrix converters popularity in future industrial applications by connecting two devices in series on the same die and thus reducing the conduction losses and the required PCB footprint. Still, such a device currently is not commercially available.

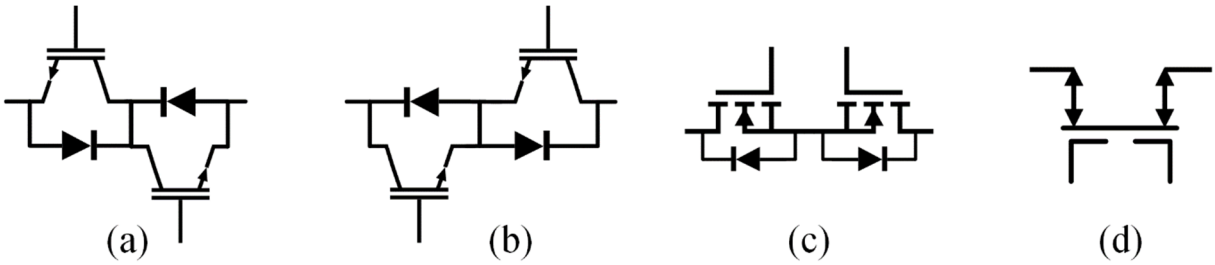


Fig. 1.4. Possible configurations for 4-quadrant bidirectional switches. (a) Common collector IGBTs. (b) Common emitter IGBTs. (c) Common source N-channel MOSFETs. (d) GaN bidirectional switch.

In contrast to VSIs used in back-to-back converters, where freewheeling current path for inductive load currents during switching dead times is provided through the diodes in anti - parallel with the switching devices, bidirectional switches cannot provide freewheeling capability without auxiliary circuitry or additional commutation logic. In other words, in the absence of clamping circuits, commutation between two bidirectional switches cannot be performed without previous knowledge of the commutation conditions. Therefore, to start the commutation, either the sign of the input line to line voltages or the sign of the inductive load currents must be known and will further dictate the sequence at which the commutation will take place.

The development of safe commutation strategies for matrix converters is a research field on its own. For a full commutation, these strategies are generally performed in either two steps or in four steps [31] and can either be based on the output load current, on the input line-to-line voltage or in a combination of both to decrease the frequency of appearance of critical situations [57]. Such situations appear in the zero crossings of either line-to-line voltages or output currents due to measurement errors and high frequency ripple, where the real sign of the physical quantity may be different from the measurement.

To illustrate the output current sign based and input voltage sign based four step commutation methods, an example of both, for the commutation of input phase ‘a’ to phase ‘b’, is presented in Fig. 1.5 and Fig. 1.6 respectively. Note that the duration of each step should be similar to the duration of deadtimes in traditional VSIs and that the fourth step corresponds to the final state of the switching process.

The two-step commutation techniques follow the same logic as the four-step methods but skip steps. The basic idea is to turn ON only the semiconductor in a bidirectional switch that will

carry the load current, while the other is kept open, using the parallel diode to provide path for current. There are versions of the two-step technique where every matrix semiconductor not blocking the current path is kept in the ON state reducing the converter conduction losses [57].

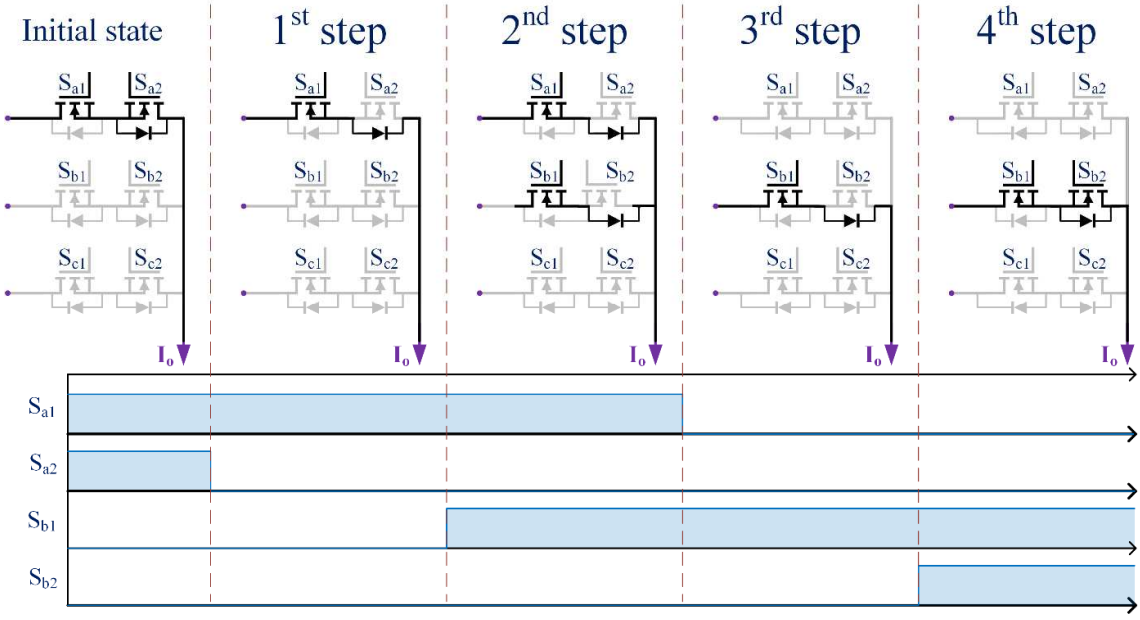


Fig. 1.5. Illustration of a four-step commutation method based on the sign of the output current. The scenario described presents the commutation from the input phase 'a' to phase 'b' with positive output current, I_0.

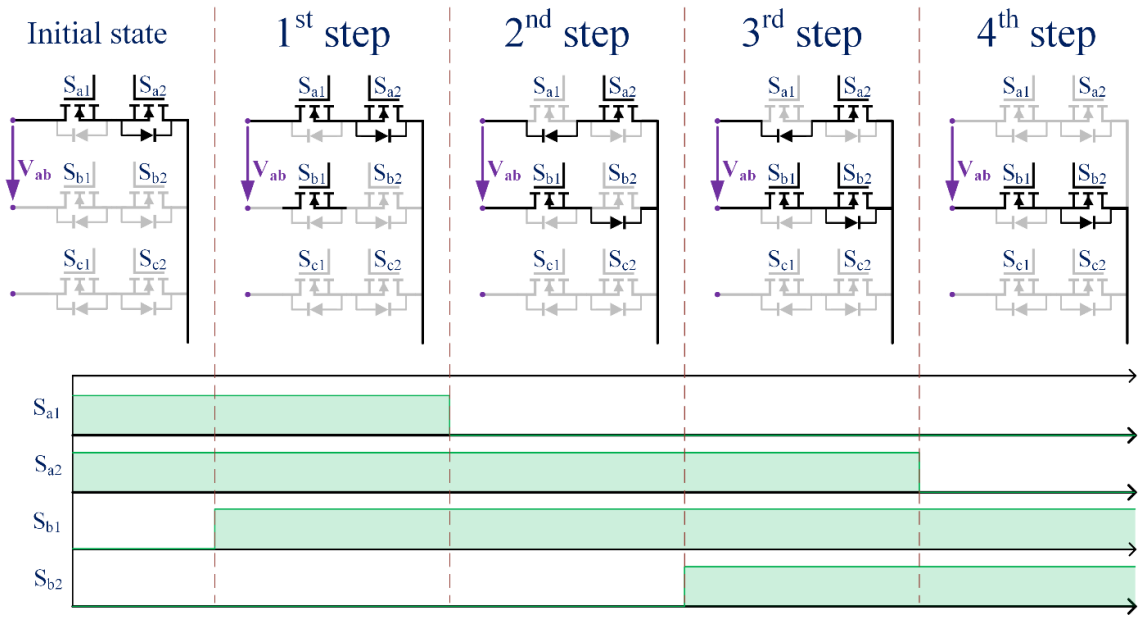


Fig. 1.6. Illustration of a four-step commutation method based on the sign of the input line-to-line voltage. The scenario described presents the commutation from the input phase 'a' to phase 'b' with positive V_{ab}.

Although the absence of freewheeling paths in bidirectional switches is something that every DMC must deal with, the same does not apply for IMCs. This happens because the output stage offers an extra degree of freedom in the form of a freewheeling current path, by making the "virtual dc-link" current null and allowing the bidirectional switches to commutate without interrupting the inductive load current. This is known in the literature as zero dc-link current commutation [58]. A modulation method that accounts for this, not only eliminates the need for complex multistep commutation methods but also allows for a reduction in the switching losses of the bidirectional switches in the input stage by enabling zero current switching [58].

Regarding research contributions of matrix converters towards electrical drives innovation, the last decade has been very rich, with several works published on matrix converter topologies for multiphase machine drives (more than three phases) and OEW drives. While both categories improve drive tolerance to fault, multiphase machines are generally associated to reduced torque ripple, higher power density and better efficiency than traditional drives [59], [60]. OEW configurations are known for allowing reduction of CMV, improved converter input to output voltage ratio and multilevel operation [16], [61]. In both cases, the switch count is increased which from one side offers more control flexibility but on the other requires more complex modulation methods. This might be the reason for the extensive research work in modulation techniques for Matrix based OEW and multiphase drives.

Direct Matrix Converter based multiphase and OEW drives research works

A single ended 3×*n* DMC based drive (three input phases and *n* output phases) allows for 3^n distinct switching states (called voltage vectors, or simply vectors). For $n > 3$, the number of voltage vectors easily attains a high value, adding complexity to the development of the modulation method. Thus, the first task on the development of any SVM strategy for such drives should be the selection of the group of vectors that best suits the priorities and objectives of the system. Vector based approaches have been proposed in the literature. In [62] a SVM technique for a 3×5 DMC, using just 93 out of the 243 available vectors, is found to be limited to a voltage gain of 0.788 in the linear modulation region. On 3×7 DMCs, a SVM method is proposed in [63], using 129 out of the 2187 available vectors, capable of achieving improved results in terms of output voltage and input current waveform quality in comparison with a counterpart scalar pulse width modulation (PWM) technique. On 3×9 DMCs, a scalar based PWM technique is proposed in [64] with capability to operate at unity power factor but is limited to a voltage gain of 0.762. A generalized theory for scalar techniques in *m*×*n* DMCs is presented in [65].

Although receiving attention in the literature, the limitations of single ended multiphase DMCs are the same as classic three phase DMCs when compared to back-to-back converters.

Regarding 3×3 DMCs connected in OEW, promising modulation strategies with the theoretical capability of eliminating CMV at machine terminals have been studied and proposed in [66]–[68]. The term theoretical is used because during the commutation between the selected switching states, the CMV is not null. These periods are very short, similar to deadtimes, and resulting CMV can be filtered with a small common mode filter, resulting in nearly zero CMV average and root mean square values. These techniques use the rotating space vectors, which by nature eliminate the CMV by applying each one of the grid voltages exactly once at every switching state. These SVM strategies can achieve a voltage gain of 1.5 while not adjusting the drive power factor. If drive power factor adjustment is pretended, the input to output voltage ratio slightly decreases.

Trying to incorporate the advantages of both, multiphase and OEW drives, a group of researchers has developed work on DMC based multiphase OEW drives. Such a topology is presented in Fig. 1.7, as a 3×*n* DMC OEW drive.

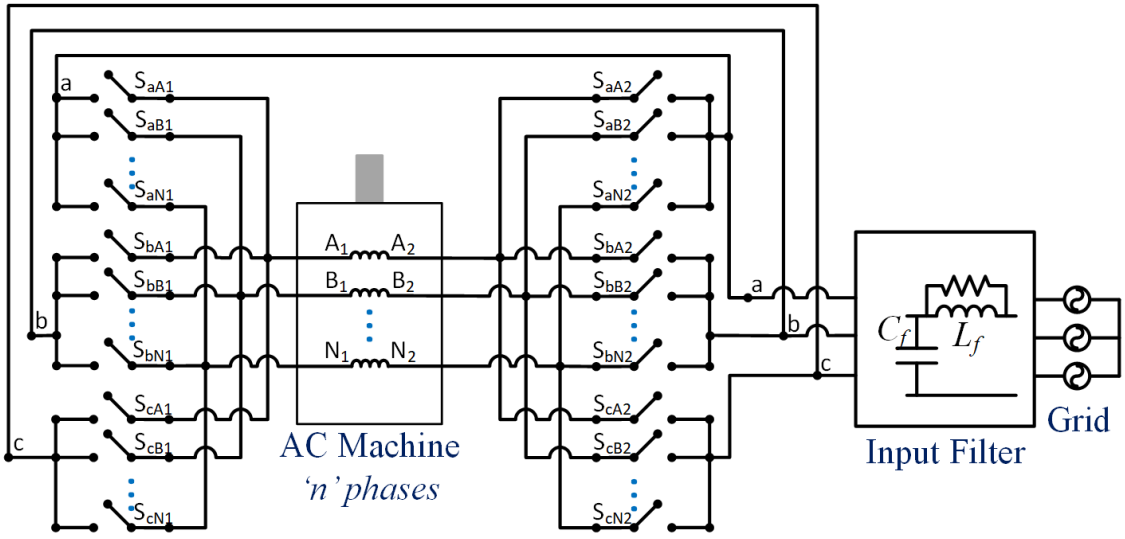


Fig. 1.7. DMC based OEW drive with three input phases and *n* output phases.

A generalized carrier based PWM technique for 3×*n* DMC for OEW is presented in [69], being able to achieve unity power factor operation and a voltage gain of 1.5. Vector based modulation strategies have been proposed for 3×5 DMC for OEW in [70]–[72] and 3×7 in [73] with capability of eliminating CMV and achieving a voltage gain of 1.5.

Indirect Matrix Converter based multiphase and OEW drives research works

By performing a two-stage conversion, creating a "virtual dc-rail", IMC based topologies allow the addition of a single arm per new phase in single ended drives, or the addition of two arms per new phase in OEW drives, as can be seen in the 3×*n* IMC OEW drive of Fig. 1.8. When compared with DMC based topologies the increment in switch count is greatly reduced and is similar to the increment in switch count in back-to-back OEW configurations. This means that drives based on IMC OEW configurations may become extremely competitive when compared with back-to-back OEW configurations by decreasing the gap in the relative semiconductor cost of both configurations while allowing elimination of bulky dc-link elements. In terms of CMV reduction, some DMC based topologies have the potential to fully eliminate the average and root mean square values of CMV while both IMC based topologies and back-to-back topologies have not. A detailed analysis of the CMV components in such topologies is provided in chapter 2 of this document.

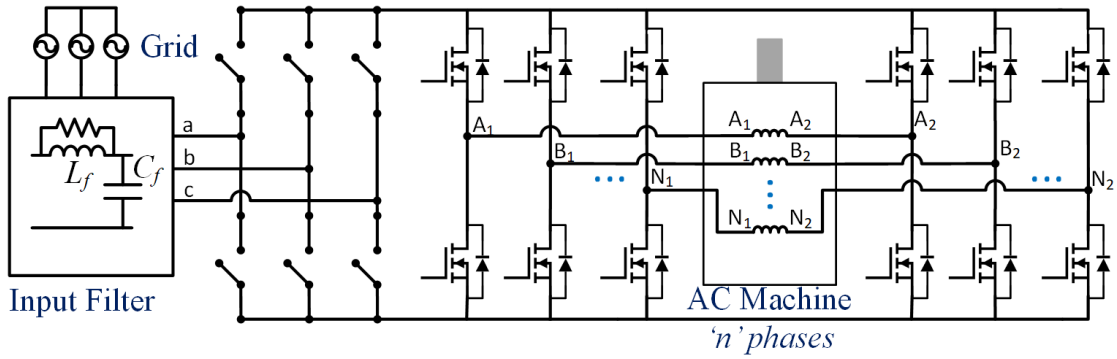


Fig. 1.8. IMC based OEW drive with three input phases and *n* output phases.

For single ended multiphase drives based in IMCs, carrier-based techniques for 3×5 IMC are proposed in [74], [75] achieving a maximum voltage gain of 0.7886. A space vector technique is proposed in [76] being limited to the same voltage gain but allowing the reduction of CMV in 29% while achieving improved THD by replacing the usage of null vectors in the modulation by the usage of two small and opposite vectors. Note that such technique does not allow zero current commutation in the input stage. The authors of [77] propose three SVM techniques for the overmodulation region achieving a boost in voltage transfer ratio from 0.7886 to 0.923 in all of them. The first technique uses only vectors with bigger amplitudes, the second technique selects the vectors depending on the amplitude of the desired output voltage, while the third

technique is improved by accounting for the variations of the virtual dc-link voltage, achieving the lowest THD among the three.

Although IMC based multiphase OEW drives combine relevant features that come handy when compared with back-to-back multiphase OEW topologies, to the best of the author knowledge, there are still no research contributions of such drives with more than three phases, making it a promising field of study in future research of multiphase OEW drives. On the other hand, some works have been presented for 3×3 IMC OEW drives, where a single dc rail is used to supply both ends of the machine, allowing a boost in voltage gain to 1.5 but creating low impedance paths for zero-sequence currents to flow. The elimination of the zero-sequence current should be considered when designing the controller and SVM technique. Authors of [78] propose a SVM strategy that only uses switching states that feature null zero-sequence voltage, resulting in null zero-sequence current. The same authors, later proposed in [79], [80] a SVM technique that minimizes the CMV by restricting the usable vectors to those eliminating the Dual Voltage Source Inverter (DVSI) contribution to CMV while removing the average value of zero-sequence voltage in each switching period by balancing the usage of two null vectors, one with positive contribution to the zero-sequence voltage and the other with negative contribution. This topology will be the object of study of this thesis chapter 2, where a detailed analysis of its switching states and SVM techniques will be performed. Authors of [81] propose a modification to this topology by eliminating one of the output arms, connecting the sixth terminal of the machine to an arm shared by two phases. The results were promising by achieving null zero-sequence currents and voltage transfer ratio of 1.5. This topology is further developed in [82], [83] where a SVM technique using three vectors for both input and output stages in each switching period is proposed. The utilization of three switching states on the rectifier stage keeps the average value of the virtual dc-link voltage constant in each switching period, improving the output waveforms quality when compared to the technique proposed in [81]. However, this comes at the cost of reducing the converter voltage transfer ratio when using the three-vector technique.

Variations of IMC based OEW drives research works

The 3×3 IMC OEW drives presented above come with a reduction in the switch count when compared with the 3×3 DMC OEW drives, but lack the ability to eliminate the CMV. This created space for two-stage topologies with higher switch count than those proposed in the IMC based OEW drive that try to incorporate fully or in part CMV reduction. The authors of [84], [85] proposed two topologies, the T-Type IMC and the I-Type IMC OEW converters, and

compared them to the 3×3 DMC OEW in [86]. Both topologies feature a rectifier stage that outputs three different voltage rails, one with the highest grid voltage, one with the second highest and a third with the minimum grid voltage. Such configuration allows the output stage to utilize the rotating space vectors, thus resulting in the theoretical elimination of the average and root mean square values of the CMV. Although both topologies require the same number of semiconductor devices as the 3×3 DMC OEW, the input stage of these topologies does not switch at high frequency, switching according to the grid voltage zones, therefore improving the converter efficiency.

A more similar configuration to the 3×3 IMC OEW topology is proposed by the author of this thesis in [87], where in one of the two output stages of the converter, instead of the standard VSI, a T-Type inverter is used with its bidirectional switches connected to the grid neutral through a filter, as presented in Fig. 1.9. This allows the usage of both, phase-to-phase and phase-to-neutral grid voltages in the machine windings. A non-linear control strategy for the converter is proposed in the same article, obtaining improvements in the quality of both input and output current waveforms when compared with the 3×3 IMC OEW. Although not completely eliminating the CMV, the proposed non-linear control strategy was able to reduce it in comparison to the 3×3 IMC OEW approach of limiting the usable output vectors to the ones that eliminate the contribution of the DVSI to the CMV proposed in [80]. Still, the Asymmetrical T-Type IMC OEW topology requires more switching devices than the 3×3 IMC OEW and the injection of load currents into the grid neutral conductor introduces a higher degree of complexity in developing a SVM strategy for fixed switching frequency operation.

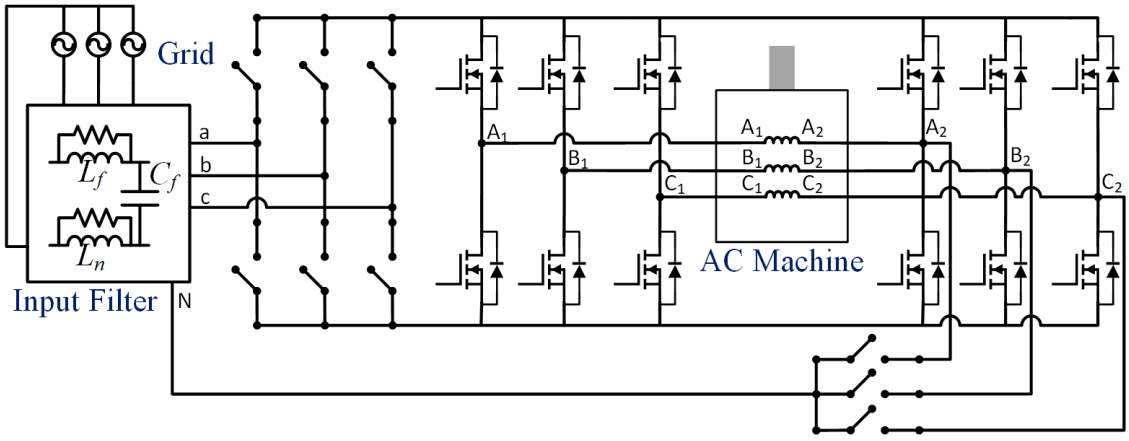


Fig. 1.9. Asymmetrical T-Type IMC OEW topology presented in [87].

1.2 – Motivation

The energy transition from traditional energy sources to renewable energies is challenging the paradigm in which the electrical grid operates, from a centralize perspective to a more decentralized manner. In such scenario, VSDs are key elements in the electricity sector transformation by playing major roles in applications such as industrial drives, renewable energy production (wind energy and tide energy), energy storage (flywheels and compressed air energy storage), heating, ventilation, and air conditioning (pumps, fans and compressors) and transportation (electric vehicles, hybrid electric vehicles, hydrogen fuel cell electric vehicles, and more electric aircrafts). Transversal to almost every of these applications is their high requirements in terms of power density, efficiency, and robustness.

VSDs are composed by a power electronic converter unit that interfaces the electric source/load and the electric machine. Regarding grid connected VSDs, the typical power electronics converter is composed by two power conversion stages, one that interfaces the grid and the DC-link (typically storing energy in a bulky electrolytic capacitor bank) and another that interfaces the DC-link and the electric machine. Both stages of power conversion are generally inside a cabinet which in some cases is placed relatively far from the electric machine. As discussed in the previous section, such solution results in high volume requirements, VSD reduced reliability and enhanced EMI problems.

The ambition of this thesis is to increase the power density of grid connected VSDs up to a point where the VSD may fit together with the machine inside a single unit, while enhancing its performance and lifetime. There are already a few research works in the literature that design the power converter to fit inside the electrical machine, being mostly focused for EVs applications. Such applications are supplied in DC, replacing the electrolytic capacitors by film capacitors, being more reliable under higher operation temperatures. Still, the approaches presented in the literature result in passive components making up for most of the volume of the proposed IMDs.

The approach proposed in this thesis focus on direct AC-AC conversion featuring high voltage gain without intermediate energy storage devices combined with adaptive non-linear field-oriented controllers for SynRMs, a type of machine that due to its cold rotor sounds ideal for integration of power converters.

1.3 – Thesis Objectives and Contributions

The main objective of this work is the increase of power density of VSDs while extending the voltage range and reducing high frequency parasitic effects that are prompt to cause the VSD premature failure and enhance EMI problems. The unlocking of such features is crucial for the generalization of grid connected IMD concept.

To achieve higher power density, the proposed approach makes use of direct AC-AC conversion, eliminating the need for intermediate energy storage. On the output stage, an OEW configuration is proposed to increase the converter input-to-output voltage gain while providing extra degrees of freedom that allow the decrease of the drive high frequency parasitic effects by means of suitable modulation methods.

To control the machine torque and speed, a novel field-oriented controller is proposed, using adaptive non-linear backstepping with stability guaranteed by the Lyapunov 2nd method of stability.

As an application example, this thesis considers a grid connected drive supplying a three phase SynRM machine, requiring bidirectional power flow capability with sinusoidal input currents and adjustable power factor. The SynRM features very promising characteristics by possessing a cold and cheap rotor structure due to the absence of currents and permanent magnets of rare-earth materials, making it an ideal candidate for IMDs.

Thus, in this context the objectives of this thesis are the following:

1. Study direct AC-AC conversion in VSDs that combine high power density with bidirectional power flow, sinusoidal input currents and high input-to-output voltage gain;
2. Study SVM techniques for direct AC-AC converters that can reduce the high frequency parasitic effects responsible for premature failures of electric machines;
3. Study the SynRM state of the art control methods and combine them with adaptive non-linear field-oriented controllers to improve the VSD dynamic response and tolerance to parameter variations and load disturbances;
4. Build a simulation model of the proposed VSD and analyse its results in terms of input-to-output voltage gain, high frequency CMV, input and output waveforms quality, and SynRM behaviour in steady state and dynamic scenarios.

5. Design and build the proposed VSD laboratory prototype;
6. Implement the proposed control algorithms and modulation methods in a System on a Chip platform, combining the capabilities of Field Programmable Gate Arrays (FPGA) and Arm-based processors into a single package;
7. Obtain laboratory results of the proposed drive.

1.4 – Contributions

Taking into consideration the scenario described above, this work is devoted to the development of a SynRM based OEW Drive well suited to fit inside the electrical machine by featuring direct AC-AC conversion, and capability of reducing CMV at the machine terminals while achieving high input to output voltage ratio. The topology under study is the Indirect Matrix Converter (IMC) with a DVSI on the output. A novel Space Vector Modulation (SVM) technique is proposed that can reduce the CMV without the need to regulate zero sequence currents. A comparison with the existent literature approach for reducing the CMV is performed.

On the SynRM perspective, this thesis introduces a modified Field Oriented Control (FOC) structure by replacing the classic linear controllers by a non-linear adaptive backstepping controller based on Lyapunov control theory featuring SynRM electrical parameters estimation. By estimating the machine parameters, the controller takes iron saturation into account resulting in more accurate and faster responses. Simultaneously, the parameter estimations connects very well with the concept of Smart Factory introduced by Industry 4.0, by providing the drive with the ability to deliver up to date data to a higher hierarchy layer of the system, which may result in earlier failure detection and optimized maintenance routines.

This thesis contributions resulted in the following publications:

[Paper I] **A. Bento**, R. Luís and J. F. Silva, "LCL filter design for a grid connected telecom station AC-DC converter using SiC devices," 2018 International Young Engineers Forum (YEF-ECE), Costa da Caparica, Portugal, 2018, pp. 61-66, doi: 10.1109/YEF-ECE.2018.8368940.

[Paper II] **A. Bento**, R. Luís, S. Pinto and J. F. Silva, "A Novel Multilevel T-Type Indirect Matrix Converter for Three-phase Open-end AC Loads," IECON 2019 - 45th Annual

Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, 2019, pp. 6575-6580, doi: 10.1109/IECON.2019.8927541.

[Paper III] **A. Bento**, R. Luís, S. Pinto and J. F. Silva, "Open-end Winding Synchronous Reluctance Sensorless Drive based on Indirect Matrix Converter with Dual VSI Output," PEMD 2020 – The 10th International Conference on Power Electronics, Machines and Drives, Nottingham, United Kingdom, 2020, pp. 995-1000, doi: 10.1049/icp.2021.1159.

[Paper IV] **A. Bento**, G. Paraíso, P. Costa, L. Zhang, T. Geury, S. F. Pinto, and J. F. Silva, "On the Potential Contributions of Matrix Converters for the Future Grid Operation, Sustainable Transportation and Electrical Drives Innovation," Applied Sciences, vol. 11, no. 10, p. 4597, May 2021. doi: 10.3390/app11104597.

1.5 – Thesis Outline

The document is organized in six chapters, including this introduction about research background in variable speed drive technologies and recent matrix converter topologies.

Chapter two provides an in-depth analysis of the IMC with DVSI output, its current SVM techniques, required commutation logic and CMV at load terminals.

Chapter three is focused in the SynRM mathematical model and in providing an overview of the different control strategies and operation trajectories for SynRM based drives.

Chapter four introduces the novelties proposed in this thesis. The first section presents the derivation of a novel non-linear backstepping controller for SynRM featuring adaptive mechanisms for improved response characteristic and further integration within the smart factory concept of Industry 5.0. On the second section, a novel SVM strategy for the IMC with DVSI output is proposed. This technique has special emphasis in reducing CMV at the load terminals while improving the input and output waveforms quality. The proposed techniques are then implemented in simulation in section 3 of chapter 4.

The fifth chapter describes the construction of the laboratory prototype and presents experimental results for the novelties proposed in the previous chapter.

The sixth and last chapter presents the main conclusions of this thesis and proposes future works within the field of research of this thesis.

CHAPTER 2

INDIRECT MATRIX CONVERTER WITH A DVSI OUTPUT

This chapter focus on the analysis of the dual-stage matrix converter with an OEW output for three phase AC machines, whose topology is shown in Fig. 2.1.

The input stage is constituted by 6 bidirectional switches and is commonly referred in the literature as the current source rectifier (CSR) stage, while the output stage is a DVSI feeding an OEW 3 phase AC machine. Note that due to the absence of energy storage devices in the interconnection of both converter stages. The so-called dc-link voltage, v_{dc}, is pulsed voltage with positive average value according to the switching state of the CSR and the instantaneous grid voltages. For this reason, the dc-link in this topology is often called virtual dc-link or soft dc-link.

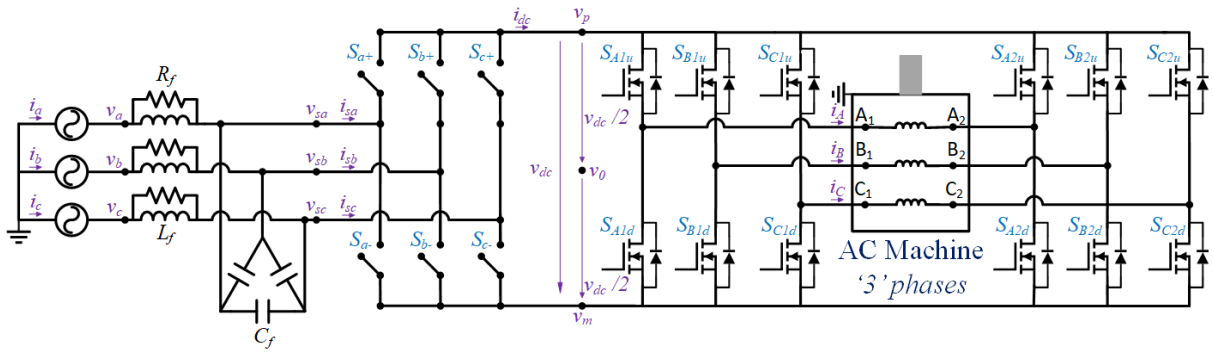


Fig. 2.1. Indirect Matrix Converter with a DVSI Output for 3 phase OEW AC machines

Throughout the document, the following considerations are made:

- The input stage physical quantities and devices (grid side) are identified with small letter subscript, while quantities in the output stage (machine side) are denoted with a capital letter subscript.
- The input stage bidirectional switches must be constituted by one of the arrangements presented in Fig. 1.4 allowing bidirectional controllability and power flow, and in the absence of further information, requiring multistep commutation logic as presented in

Fig. 1.5 or Fig. 1.6. To simplify the analysis, bidirectional switches will simply be considered as single ideal switches with states S_{a+}, S_{b+}, S_{c+}, S_{a-}, S_{b-}, S_{c-}.

- When a switching device is in the ON state, the correspondent variable state (S_{a+}, S_{b+}, S_{c+}, S_{a-}, S_{b-}, S_{c-}) is represented as 1, while when in the OFF state the variable state is denoted as 0.
- Not more than one bidirectional switch can be connected at a given instant to any of the virtual dc-link buses, v_p and v_m ($S_{a+}+S_{b+}+S_{c+} = S_{a-}+S_{b-}+S_{c-} \leq 1$). This rule prevents short circuiting the AC filter capacitors.
- Output currents cannot be instantaneously extinguished due to their inductive nature. If there are no freewheeling paths for the currents in the DVSI side ($I_{dc} \neq 0$), the bidirectional switches from the input side must allow the load currents to freewheel. In such scenario, the CSR states must guarantee ($S_{a+}+S_{b+}+S_{c+} = S_{a-}+S_{b-}+S_{c-} = 1$).
- It must be guaranteed that the dc-link voltage is always positive. This rule prevents the AC filter capacitors from being short circuited through the DVSI diodes.

2.1 – Common Mode Voltage Computation

As introduced in subsection 1.1.1, the presence of CMV is responsible for originating bearing currents that may result in bearing premature failure. Thus, it is important to take a closer look at how CMV is originated in this specific topology. The CMV in an OEW configuration is given by (2.1), where v_{xyG} is the voltage from the terminal 'y' of the output phase 'x' in respect to the installation ground [87].

$$CMV = \frac{1}{6}\left(v_{A1G} + v_{B1G} + v_{C1G} + v_{A2G} + v_{B2G} + v_{C2G}\right) \tag{2.1}$$

Note that v_{xyG} can be decomposed into two components as shown in (2.2). The first, v_{xy0}, corresponds to the contribution of the output arm in respect to the virtual dc-link midpoint voltage, indicated in Fig. 2.1 as v_0. The second component is due to the contribution of the CSR state that corresponds to the difference between the virtual dc-link midpoint voltage relative to the installation ground, v_{0G}.

$$v_{xyG} = v_{xy} - v_G = v_{xy} - v_G + v_0 - v_0 = v_{xy0} + v_{0G} \tag{2.2}$$

Replacing (2.2) into (2.1), a different expression for CMV can be obtained given by (2.3), where v_{cm0} is defined as the DVSI contribution to CMV. This new expression decouples the contribution of both input and output stages to the global CMV.

$$CMV = v_{0G} + \frac{1}{6}\left(v_{A10} + v_{B10} + v_{C10} + v_{A20} + v_{B20} + v_{C20}\right) = v_{0G} + v_{cm0} \tag{2.3}$$

The CSR Contribution is given by (2.4), where v_{sa}, v_{sb} and v_{sc} are the voltages at the input of the CSR.

$$v_{0G} = \frac{1}{2}\left[v_{as}\left(S_{a+} + S_{a-}\right) + v_{bs}\left(S_{b+} + S_{b-}\right) + v_{cs}\left(S_{c+} + S_{c-}\right)\right] \tag{2.4}$$

The DVSI contribution can be put as function of both, the virtual dc-link voltage, v_{dc}, and the number of DVSI upper switches turned ON at a given instant, N_{sw}, as indicated by (2.5). The number of DVSI upper switches turned ON is obtained from (2.6), where S_{Au1}, S_{Bu1}, S_{Cu1}, S_{Au2}, S_{Bu2} and S_{Cu2} are the states of the DVSI upper switches indicated in Fig. 2.1.

$$v_{cm0} = \frac{1}{6}\left[N_{sw}\frac{v_{dc}}{2} - \left(6 - N_{sw}\right)\frac{v_{dc}}{2}\right] = \frac{v_{dc}}{6}\left[N_{sw} - 3\right] \tag{2.5}$$

$$N_{sw} = S_{Au1} + S_{Bu1} + S_{Cu1} + S_{Au2} + S_{Bu2} + S_{Cu2} \tag{2.6}$$

The author of [88] proposed a SVM approach for CMV reduction in this topology. This was performed by limiting the group of output usable switching states to the combinations where exactly three DVSI upper switches are turned ON. This eliminates the contribution of the DVSI to the CMV, leaving only the contribution of the CSR. This strategy derived in section 2.3.2.

The soft dc-link voltage is obtained through (2.7) as function of the CSR input voltages and its switching state. This means that even though often designated as DVSI contribution to CMV, v_{cm0} also depends on the CSR state as shown in (2.8).

$$v_{dc} = v_{sa}\left(S_{a+} - S_{a-}\right) + v_{sb}\left(S_{b+} - S_{b-}\right) + v_{sc}\left(S_{c+} - S_{c-}\right) \tag{2.7}$$

$$v_{cm0} = \frac{1}{6}\left[v_{sa}\left(S_{a+} - S_{a-}\right) + v_{sb}\left(S_{b+} - S_{b-}\right) + v_{sc}\left(S_{c+} - S_{c-}\right)\right]\left(N_{sw} - 3\right) \tag{2.8}$$

By replacing (2.4) and (2.8) into (2.3), after some algebraic manipulations, the CMV can be further expanded into (2.9).

$$CMV = \left[v_{sa}S_{a-} + v_{sb}S_{b-} + v_{sc}S_{c-}\right] + \frac{N_{sw}}{6}\left[v_{sa}\left(S_{a+} - S_{a-}\right) + v_{sb}\left(S_{b+} - S_{b-}\right) + v_{sc}\left(S_{c+} - S_{c-}\right)\right] \tag{2.9}$$

Taking a closer look at (2.9), one may observe that the resulting CMV is the sum of two main terms. The first term results in one of the grid line-to-ground voltages, while the second is the soft dc-link voltage scaled by one sixth of the number of DVSI upper switches turned ON. The dc-link instantaneous voltage is either one of the grid line-to-line voltages or is zero when both switches of the same input phase are turned ON. Since N_{sw} is an integer, the relation between a line-to-line voltage and a line-to-ground voltage cannot be exactly matched by discrete adjustment of N_{sw}. This proves that it is impossible to eliminate the instantaneous CMV in this topology, in contrast to the case of OEW DMC where the rotating space vectors naturally eliminate the CMV [67][68].

2.2 – Input Stage (Current Source Rectifier)

As introduced in subsection 1.1.3, the topology adopted in this thesis is classified as a dual-stage Matrix converter. IMC SVM methods are generally based on separate and individual modulations for the input and output stages, followed by a synchronized combination of the duty-cycles from both stages [89].

Identically to the conventional IMC, the input stage is composed by a CSR as presented in Fig. 2.2. This stage is responsible for maintaining sinusoidal input currents on the grid side while providing positive dc-link voltage to the output stage.

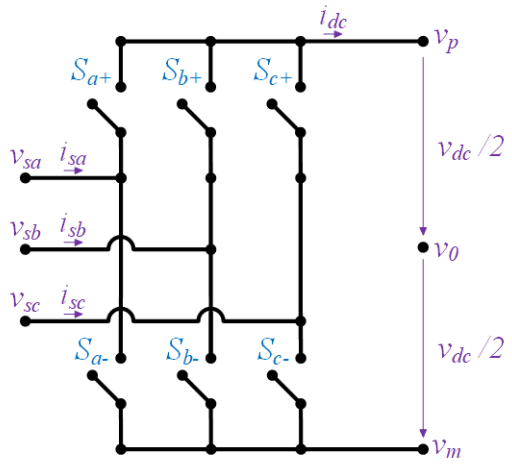


Fig. 2.2. IMC Input stage. Grid side is on the left, soft dc-link side is on the right.

Voltages and currents on the AC side of the CSR and voltages and currents on the soft dc-link are related by a CSR switching matrix, $\mathbf{S_{CSR}}$, given by (2.10). As previously stated, the states of the switches can either be 1 when the switch is ON, or 0 when the switch is OFF.

$$\mathbf{S_{CSR}} = \begin{bmatrix} S_{a+} & S_{b+} & S_{c+} \\ S_{a-} & S_{b-} & S_{c-} \end{bmatrix} \tag{2.10}$$

The voltage of each of the busbars, v_p and v_m, in the soft dc-link can be obtained through (2.11). The dc-link voltage is then obtained considering $v_{dc} = v_p - v_m$, in accordance to (2.7).

$$\begin{bmatrix} v_p & v_m \end{bmatrix}^T = \mathbf{S_{CSR}} \begin{bmatrix} v_{sa} & v_{sb} & v_{sc} \end{bmatrix}^T \tag{2.11}$$

The input currents can be related to the dc-link currents through (2.12).

$$\begin{bmatrix} i_{sa} & i_{sb} & i_{sc} \end{bmatrix}^T = \mathbf{S}_{\mathbf{CSR}}^T \begin{bmatrix} i_{dc} & -i_{dc} \end{bmatrix}^T \tag{2.12}$$

As introduced in the beginning of this chapter, there are some conditions that the CSR must guarantee:

- Not more than one upper switch and one bottom switch can be turned ON to avoid short-circuiting the input phases.
- Soft dc-link voltage must be always positive to avoid short-circuiting the dc-link through the diodes of the output stage.
- There must be always one upper switch and one bottom switch both turned ON to provide path for inductive load currents.

Considering the above-mentioned rules, the 6 bidirectional switches that constitute the CSR can be arranged in 9 different switching configurations, indicated in Table 2.1 along with their resulting instantaneous quantities: input current contribution, soft dc-link voltage, and CSR contribution to CMV.

For the control of AC variables in three phase systems, it is common to take advantage of frame transformations which may allow a reduction in the number of controlled variables in case of balanced systems.

The nine switching states can be represented in the $\alpha\beta\gamma$ stationary reference frame by taking advantage of the power invariant Concordia Transformation [90], given by (2.13). A given

variable, $\mathbf{x}=[\,x_a \quad x_b \quad x_c\,]^T$, in the grid *abc* frame is transformed to the *αβγ* frame by (2.14), and the inverse transformation is possible using (2.15).

Table 2.1: CSR switching table with their corresponding input current, dc-link voltage, and contribution to CMV

State	S_{a+}	S_{a-}	S_{b+}	S_{b-}	S_{c+}	S_{c-}	$(i_{sa}; i_{sb}; i_{sc})$	v_{dc}	v_{0G}
1	1	0	0	1	0	0	$(i_{dc};\ -i_{dc}; 0)$	v_{sab}	$(v_{sa}+v_{sb})/2$
2	1	0	0	0	0	1	$(i_{dc};\ 0; -i_{dc})$	v_{sac}	$(v_{sa}+v_{sc})/2$
3	1	1	0	0	0	0	$(0;\ 0; 0)$	0	v_{sa}
4	0	1	1	0	0	0	$(-i_{dc};\ i_{dc}; 0)$	v_{sba}	$(v_{sa}+v_{sb})/2$
5	0	0	1	0	0	1	$(0;\ i_{dc}; -i_{dc})$	v_{sbc}	$(v_{sb}+v_{sc})/2$
6	0	0	1	1	0	0	$(0;\ 0; 0)$	0	v_{sb}
7	0	1	0	0	1	0	$(-i_{dc};\ 0; i_{dc})$	v_{sca}	$(v_{sa}+v_{sc})/2$
8	0	0	0	1	1	0	$(0;\ -i_{dc}; i_{dc})$	v_{scb}	$(v_{sb}+v_{sc})/2$
9	0	0	0	0	1	1	$(0;\ 0; 0)$	0	v_{sc}

$$\mathbf{C}=\sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{2.13}$$

$$\begin{bmatrix} x_\alpha & x_\beta & x_\gamma \end{bmatrix}^T = \mathbf{C}\begin{bmatrix} x_a & x_b & x_c \end{bmatrix}^T \tag{2.14}$$

$$\begin{bmatrix} x_a & x_b & x_c \end{bmatrix}^T = \mathbf{C}^T\begin{bmatrix} x_\alpha & x_\beta & x_\gamma \end{bmatrix}^T \tag{2.15}$$

The CSR input current space vectors are given by Table 2.2 as function of the soft dc-link current. Note that when the dc-link current is negative, the argument of the input current vector is shifted by 180 degrees. A graphical representation of these vectors is provided in Fig. 2.3.

It is possible to observe in Table 2.1 and Table 2.2 that the switching states connecting the same input phase to both dc-link busbars result in null dc-link voltage and in null input current space vector. Due to this reason, these vectors are designated as CSR null vectors. The remaining six

vectors, often named as CSR active vectors, are spaced by 60 degrees with the same amplitude in the $\alpha\beta\gamma$ stationary reference frame.

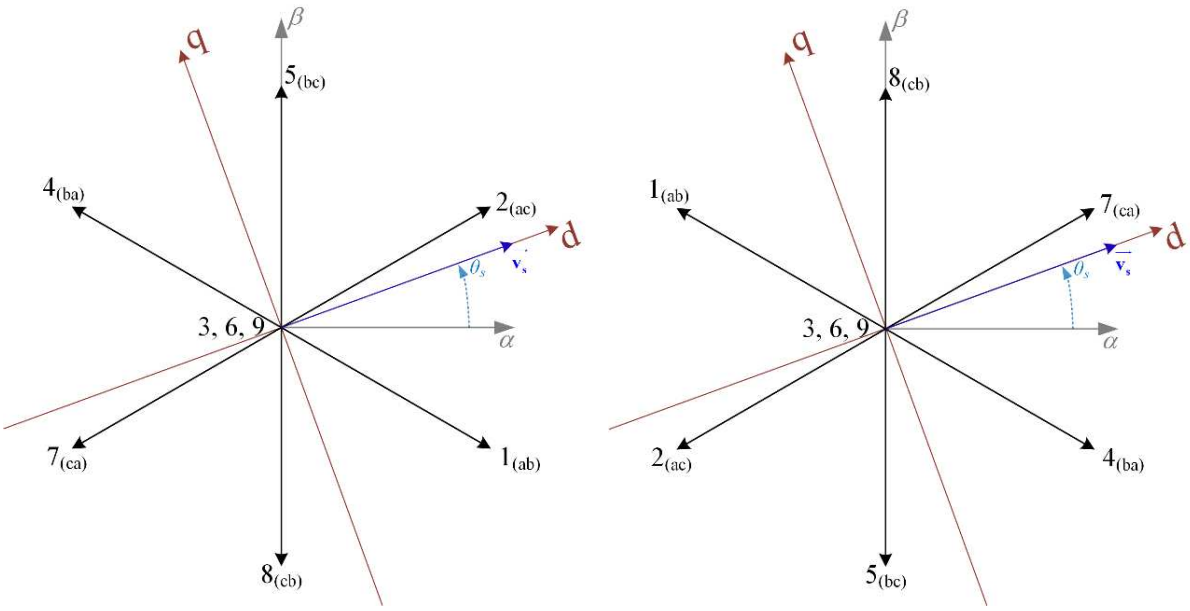


Fig. 2.3. Space vector representation of the CSR input current vectors and its input current sectors in the $\alpha\beta\gamma$ frame for its switching states. (a) Situation with $i_{dc} > 0$. (b) Situation with $i_{dc} < 0$.

Table 2.2: CSR input current space vectors in the αβγ.

State	$\lvert\mathbf{i}_{s\,\alpha\beta}\rvert$	$\measuredangle(\mathbf{i}_{s\,\alpha\beta}),\{i_{dc}>0\}$	$\measuredangle(\mathbf{i}_{s\,\alpha\beta}),\{i_{dc}<0\}$
1	$\sqrt{2}\,\lvert i_{dc}\rvert$	$-\pi/6$	$5\pi/6$
2	$\sqrt{2}\,\lvert i_{dc}\rvert$	$\pi/6$	$-5\pi/6$
3	0	0	0
4	$\sqrt{2}\,\lvert i_{dc}\rvert$	$5\pi/6$	$-\pi/6$
5	$\sqrt{2}\,\lvert i_{dc}\rvert$	$\pi/2$	$-\pi/2$
6	0	0	0
7	$\sqrt{2}\,\lvert i_{dc}\rvert$	$-5\pi/6$	$\pi/6$
8	$\sqrt{2}\,\lvert i_{dc}\rvert$	$-\pi/2$	$\pi/2$
9	0	0	0

It is possible to obtain the contribution of the CSR switching states in a *dqz* reference frame synchronized with the CSR input voltages phase, θ_s. This synchronized reference frame is

obtained by using the Park transformation matrix, given by (2.16), rotating the *αβγ* stationary reference frame with angular velocity $\omega_i = d\theta_s/dt$. A given variable $\mathbf{x_s} = [\, x_{s\alpha} \;\; x_{s\beta} \;\; x_{s\gamma} \,]^T$, in the *αβγ* stationary reference frame is transformed to the *dqz* frame synchronized with the CSR input voltages phase by (2.17), and the reverse operation is performed using (2.18).

$$\mathbf{P}_s = \begin{bmatrix} \cos(\theta_s) & \sin(\theta_s) & 0 \\ -\sin(\theta_s) & \cos(\theta_s) & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{2.16}$$

$$\begin{bmatrix} x_{sd} & x_{sq} & x_{sz} \end{bmatrix}^T = \mathbf{P}_s \begin{bmatrix} x_{s\alpha} & x_{s\beta} & x_{s\gamma} \end{bmatrix}^T \tag{2.17}$$

$$\begin{bmatrix} x_{s\alpha} & x_{s\beta} & x_{s\gamma} \end{bmatrix}^T = \mathbf{P}_s^T \begin{bmatrix} x_{sd} & x_{sq} & x_{sz} \end{bmatrix}^T \tag{2.18}$$

In this *dqz* frame synchronized with θ_s, the instantaneous power, $p_s(t)$, and reactive power, $q_s(t)$, are given by (2.19). Note that due to the absence of neutral connection, there are no zero sequence currents ($i_{sa} + i_{sb} + i_{sc} = 0 \rightarrow i_{sz} = 0$).

$$\begin{aligned} p_s(t) &= v_{sd} i_{sd} + v_{sq} i_{sq} + v_{sz} i_{sz} \\ q_s(t) &= \mathrm{v}_{sd}\, i_{sq} - v_{sq} i_{sd} \end{aligned} \tag{2.19}$$

2.2.1 – IMC input current modulation

Even though the CSR features six non-null current vectors, those are not all admissible at a given time instant. This is easy to understand from Table 2.1, by noting that the resulting dc-link voltage of one switching state is symmetric to another (take switching states $1_{(ab)}$ and $4_{(ba)}$ as example), meaning that if one leads to positive dc-link voltage, the symmetric vector will lead to negative dc-link voltage, which is not admissible due to the output inverter stage diodes.

The usage of the CSR null vectors is avoidable because the same effect may be accomplished using the null vectors of the inverter output stage. Authors of [91] clearly describe the usage of null vectors for the conventional IMC on the input stage versus its usage in the output stage. It was concluded that the usage of null vectors in the output inverter stage would allow the CSR to switch with zero current without requiring any of the dedicated commutation logics presented in subsection 1.1.3, while the usage of CSR null vectors would allow the output inverter stage to switch with zero dc-link voltage but requiring multi-step commutation logic on the input stage. Thus, conventional IMCs SVM strategies commonly shift the usage of null vectors to the output inverter stage of the converter [91]. Note that the avoidance of dedicated commutation

logic for bidirectional switches is dependent on the condition that the dc-link current is kept null at the time of commutation.

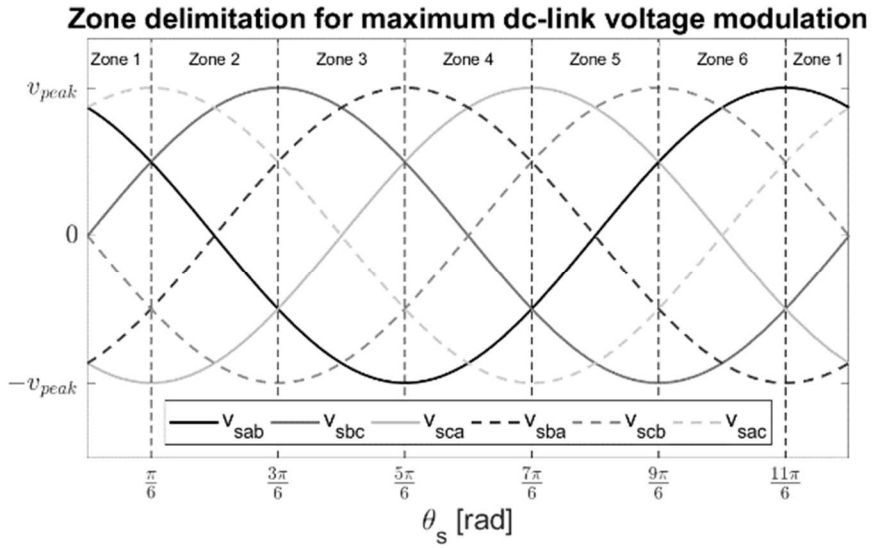
Regarding the active vectors, for any given time instant, the CSR has three usable switching states that differ on the amplitude of the dc-link voltage but also on the input current contribution. Even though there are SVM strategies to modulate the CSR input current using the three available active vectors such as the one presented in [83], where improved output current waveforms are obtained with a constant dc-link average voltage, at the cost of reducing the converter voltage gain and decreasing efficiency. However, in most research works the CSR input current modulation is performed employing only two out of the three usable active switching states.

Using only two active vectors while disregarding the null vectors, the input stage modulation is responsible for the CSR input current phase, θ_i, leaving the magnitude of this vector dependent on the dc-link current which is imposed by the output inverter stage modulation [89][92].

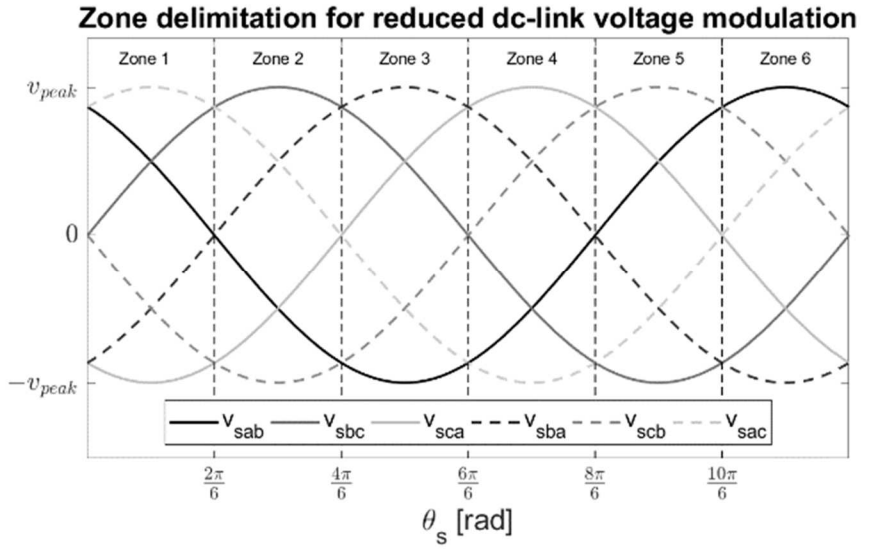
Two different SVM strategies are commonly used to modulate the IMC input current and maintain positive dc-link voltage. The first strategy maximizes the average dc-link voltage while the second strategy results in a noticeable reduction in the average dc-link voltage. The strategy that reduces the average value of the dc-link voltage, resulting in reduced converter voltage gain, is needed in situations where the output inverter stage requires a very low output voltage, allowing the DVSI to switch with lower dc-link voltages, reducing the switching losses of the output inverter stage [78].

In both strategies, the CSR input voltages can be mapped into six zones according to the location of θ_s. The six zones limits depend on the selected modulation strategy (maximum dc-link voltage or reduced dc-link voltage), as shown in Fig. 2.4. Observing Fig. 2.4(a), it can be noted that the zone transition logic detects when one of the two higher input CSR voltages changes. To obtain maximum dc-link average voltage within each zone, the CSR input current is modulated prioritizing the vectors that lead to higher output voltage. For reduced dc-link voltage strategy the opposite situation occurs, see Fig. 2.4(b). A given zone ends when one of the two AC voltages leading to the least positive dc-link voltage is succeeded by the following AC voltage. The CSR input current regulation in this modulation scheme is performed prioritizing the switching states that lead to lower dc-link voltage.

The same sector transition logic may be applied to the stationary reference frame and to the reference input current vector. Its location may be mapped into current sectors, with the sector limits coincident with the input voltages zones limits when $i_{dc} > 0$, but shifted by 180 degrees when $i_{dc} < 0$, as indicated in Fig. 2.5 for maximum dc-link voltage strategy and in Fig. 2.6 for reduced dc-link voltage strategy.



(a)



(b)

Fig. 2.4. Input CSR voltage zone delimitation depending on the selected modulation method. (a) for strategy with maximum dc-link voltage. (b) for strategy with reduced dc-link voltage.

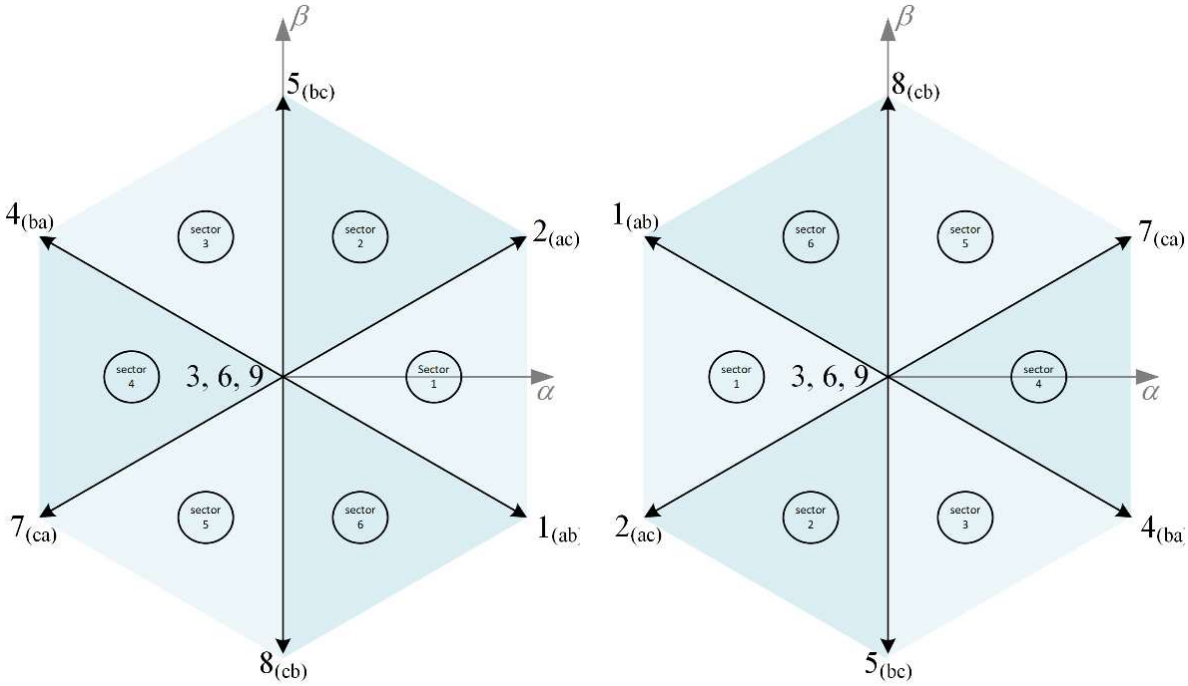


Fig. 2.5. Maximum dc-link voltage strategy input current reference sectors depending on the signal of i_{dc}. (a) $i_{dc} > 0$. (b) $i_{dc} < 0$.

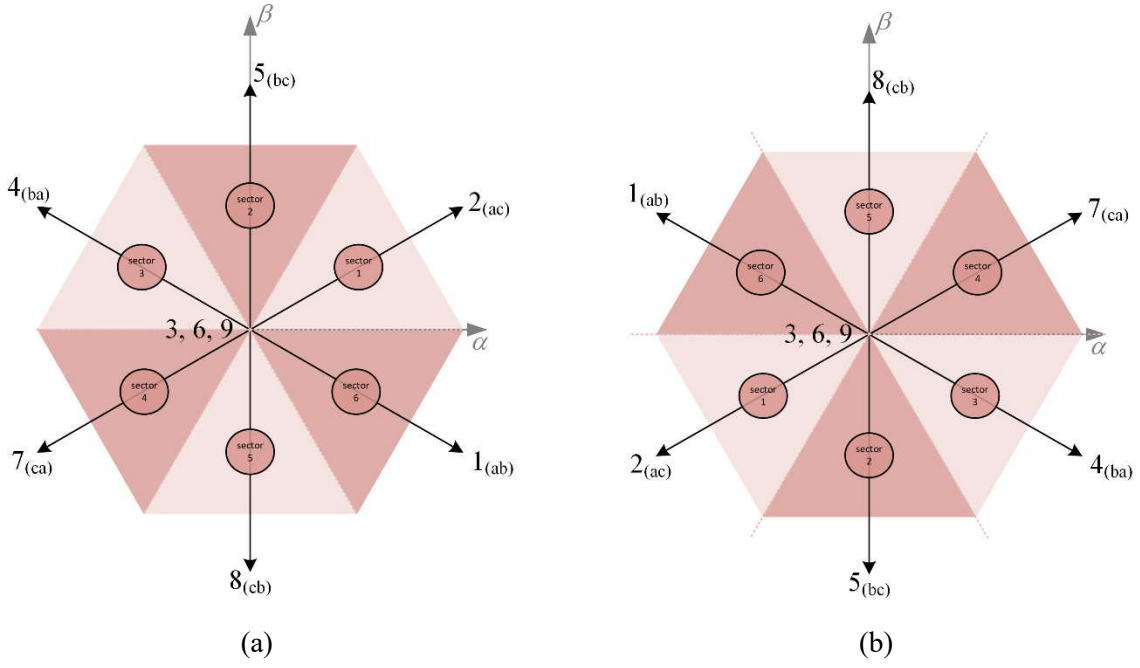


Fig. 2.6. Reduced dc-link voltage strategy input current reference zones depending on the signal of the i_{dc}. (a) $i_{dc} > 0$. (b) $i_{dc} < 0$.

2.2.2 – IMC input current modulation for maximum dc-link voltage

In this modulation strategy the input voltage sector limits are coincident with the location of the input current vectors in the *αβγ* stationary reference frame. The analysis presented hereafter presumes that the switching frequency is high enough so that the CSR input voltages remain nearly constant within the duration of the switching period.

The input current reference is synthetized by two adjacent current vectors. A graphical representation is provided in Fig. 2.7 for a situation where both the input voltage vector (coincident with the *d axis*) and input current reference are inside zone 1. Note that in this situation, the two current vectors that are adjacent to the input current reference, $\mathbf{i}_i$, result from the CSR switching state 1 ($v_{dc}=v_{s\,ab}$) and 2 ($v_{dc}=v_{s\,ac}$). The analytical expression for the resulting current vectors of these switching states is obtained using Table 2.2, given by (2.20) where **α** and **β** are unit vectors of the stationary reference frame.

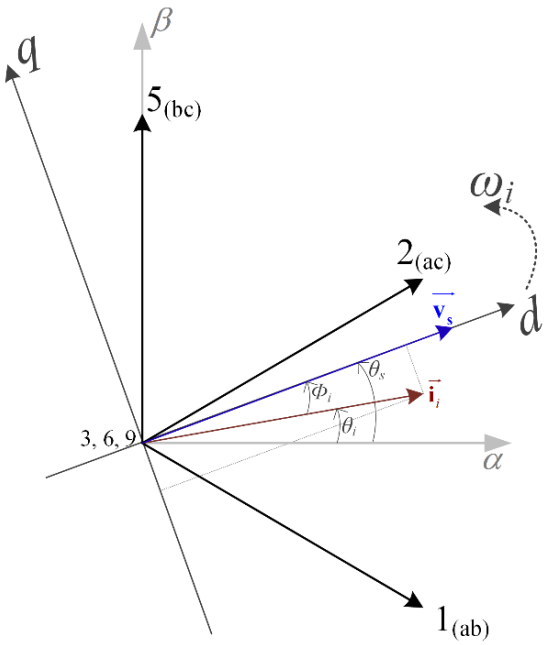


Fig. 2.7. Usable current space vectors for the situation with both CSR input voltage vector and reference input current vector are within the 1st zone of the grid.

$$\begin{cases} \mathbf{i}_1 = \sqrt{2} i_{dc} \left[\cos\left(-\frac{\pi}{6}\right)\boldsymbol{\alpha} + \sin\left(-\frac{\pi}{6}\right)\boldsymbol{\beta} \right] \\ \mathbf{i}_2 = \sqrt{2} i_{dc} \left[\cos\left(\frac{\pi}{6}\right)\boldsymbol{\alpha} + \sin\left(\frac{\pi}{6}\right)\boldsymbol{\beta} \right] \end{cases} \tag{2.20}$$

The input current reference vector is synthetized by a weighted average of both switching states, being δ_1^R and δ_2^R the corresponding portion of the switching period where each CSR switching state is selected. The resulting input current vector is given by (2.21).

$$\mathbf{i_i} = \delta_1^R \mathbf{i_1} + \delta_2^R \mathbf{i_2} = \sqrt{2} i_{dc} \left[\frac{\sqrt{3}}{2} \left(\delta_1^R + \delta_2^R \right) \boldsymbol{\alpha} + \frac{1}{2} \left(\delta_2^R - \delta_1^R \right) \boldsymbol{\beta} \right] \tag{2.21}$$

Note that by shifting the null vectors to the output stage of the IMC, the entire switching period is occupied by the two adjacent current vectors, $\delta_1^R + \delta_2^R = 1$. At the same time, it is possible to relate the phase of the input current with its **α** and **β** components. Solving the system in order to δ_1^R and δ_2^R, the duty-cycles of each CSR switching states, leading to an averaged current vector with phase θ_i, are given by (2.22). The average soft dc-link voltage within a switching period can be computed using (2.23).

$$\begin{cases} \theta_i = \arctan\left(\dfrac{\frac{1}{2}\left(\delta_2^R - \delta_1^R \right)}{\frac{\sqrt{3}}{2}\left(\delta_1^R + \delta_2^R \right)} \right) \\ 1 = \delta_1^R + \delta_2^R \end{cases} \Rightarrow \begin{cases} \delta_1^R = \dfrac{1}{2} - \dfrac{\sqrt{3}}{2} \tan\left(\theta_i \right) \\ \delta_2^R = \dfrac{1}{2} + \dfrac{\sqrt{3}}{2} \tan\left(\theta_i \right) \end{cases} \tag{2.22}$$

$$V_{dc} = \delta_1^R v_{sab} + \delta_2^R v_{sac} \tag{2.23}$$

This equation considers the input reference current vector in the first current sector ($-\pi/6 \leq \theta_i \leq \pi/6$). To generalize (2.22) to the six reference current sectors it is needed:

1. To transform the θ_i angle according to the reference current sector into the equivalent angle φ_{ref}^R;
2. To change the active vectors that modulate the input current vector.

The duty-cycles are then computed through (2.24), with the active switching states and the reference angle φ_{ref}^R indicated in Table 2.3. The average dc-link voltage during the switching period is given by (2.25).

$$\begin{cases} \delta_\rho^R = \dfrac{1}{2} - \dfrac{\sqrt{3}}{2} \tan\left(\varphi_{ref}^R \right) \\ \delta_\sigma^R = \dfrac{1}{2} + \dfrac{\sqrt{3}}{2} \tan\left(\varphi_{ref}^R \right) \end{cases} \tag{2.24}$$

$$V_{dc} = \delta_{\rho}^{R} v_{s}^{\rho} + \delta_{\sigma}^{R} v_{s}^{\sigma} \tag{2.25}$$

Table 2.3: Generalization of the duty-cycles for the maximum dc-link voltage strategy.

Current Sector	Vector ρ	Vector σ	φ_{ref}^{R}
1	$1_{(ab)}$	$2_{(ac)}$	θ_i
2	$2_{(ac)}$	$5_{(bc)}$	$\theta_i - \pi/3$
3	$5_{(bc)}$	$4_{(ba)}$	$\theta_i - 2\pi/3$
4	$4_{(ba)}$	$7_{(ca)}$	$\theta_i - \pi$
5	$7_{(ca)}$	$8_{(cb)}$	$\theta_i - 4\pi/3$
6	$8_{(cb)}$	$1_{(ab)}$	$\theta_i - 5\pi/3$

It is important to note that for non-null current-to-voltage displacement angles ($\Phi_i \neq 0$), there are instants where the input voltage vector zone is different than the sector of the input current reference vector. In those situations, to allow the modulation of the input current vector the switching states that are used do not result in the two higher input voltages.

An example of this situation happens in the following scenario: for the instant $\theta_s = \pi/4$ with $\Phi_i = \pi/8 \rightarrow \theta_i = \theta_s - \Phi_i = \pi/8$. The CSR input voltage is in the second zone where the maximum dc-link would be obtained with the CSR switching states $2_{(ac)}$ and $5_{(bc)}$. On the other hand, to allow modulation of the input current in the first current sector, it is required to use a combination of switching states $1_{(ab)}$ and $2_{(ac)}$. Thus, a reduction in the average dc-link voltage in respect to the situation with null current-to-voltage displacement angle appears. The minimum dc-link voltage averaged within each switching period as function of the current-to-voltage displacement angle is given by (2.26).

$$V_{dc\,\min} = \frac{3}{\sqrt{2}} v_{s\,rms} \cos(\phi_i) \tag{2.26}$$

Thus, when processing sufficient active power, the IMC allows control of the input power factor at the cost of losing converter voltage gain [91][93].

2.2.3 – IMC input current modulation for reduced dc-link voltage

The strategy to obtain a reduced dc-link average voltage, similarly with the previous approach divides the stationary reference frame into six sectors with distinct limits regarding the previous approach. Again, for this analysis, it is considered that the switching frequency is high enough, so that the CSR input voltages remain nearly constant during the switching period.

Contrary to the strategy that maximizes the dc-link voltage, in this method the input current reference is not synthetized by the two adjacent current vectors. Instead, the single vector inside the current reference sector is not utilized. Consider the scenario presented in Fig. 2.8, where the input voltage vector is in zone 1 ($0 \leq \theta_s < \pi/3$) and the reference displacement current-to-voltage angle is zero ($\Phi_i = 0 \rightarrow \theta_i = \theta_s - \Phi_i = \theta_s$). The reference input current vector in this scenario is synthetized by switching states 1 ($v_{dc} = v_{s\,ab}$) and 5 ($v_{dc} = v_{s\,bc}$). The analytical expression for these current vectors is given by (2.27). The resulting input current vector is given in (2.28).

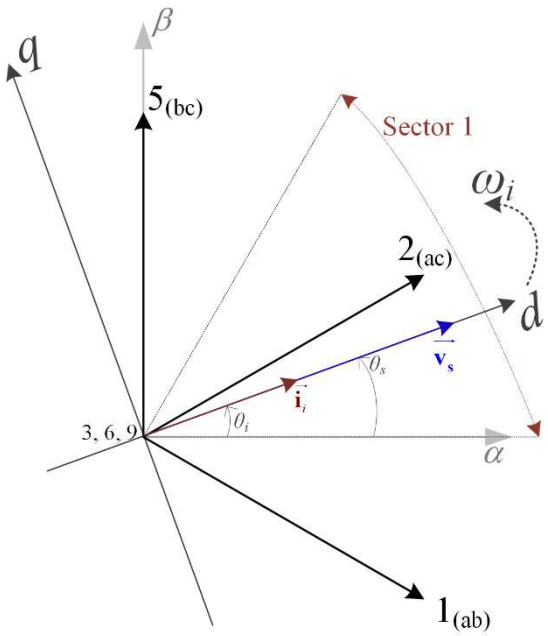


Fig. 2.8. Usable current space vectors for the situation with both CSR input voltage vector and reference input current vector are within the 1st zone of the grid.

$$\begin{cases} \mathbf{i_1} = \sqrt{2} i_{dc} \left[\cos\left(-\frac{\pi}{6}\right)\boldsymbol{\alpha} + \sin\left(-\frac{\pi}{6}\right)\boldsymbol{\beta} \right] \\ \mathbf{i_5} = \sqrt{2} i_{dc} \left[\cos\left(\frac{\pi}{2}\right)\boldsymbol{\alpha} + \sin\left(\frac{\pi}{2}\right)\boldsymbol{\beta} \right] \end{cases} \tag{2.27}$$

$$\mathbf{i_i} = \delta_1^R \mathbf{i_1} + \delta_5^R \mathbf{i_5} = \sqrt{2} i_{dc} \left[\frac{\sqrt{3}}{2} \delta_1^R \boldsymbol{\alpha} + \left(\delta_5^R - \frac{\delta_1^R}{2} \right) \boldsymbol{\beta} \right] \tag{2.28}$$

Considering the utilization of null vectors as a part of the output inverter stage modulation, $\delta_1^R + \delta_5^R = 1$, the corresponding duty-cycles of each switching state are obtained by (2.29). Again, shifting the null vectors to the output stage, makes the input current vector amplitude dependent exclusively on i_{dc}. The soft dc-link average voltage for this scenario can be computed using (2.30).

$$\begin{cases} \theta_i = \arctan\left(\dfrac{\delta_5^R - \dfrac{\delta_1^R}{2}}{\dfrac{\sqrt{3}}{2}\delta_1^R} \right) \\ 1 = \delta_1^R + \delta_5^R \end{cases} \Rightarrow \begin{cases} \delta_1^R = \dfrac{2}{\sqrt{3}\tan(\theta_i) + 3} \\ \delta_5^R = \dfrac{\sqrt{3}\tan(\theta_i) + 1}{\sqrt{3}\tan(\theta_i) + 3} \end{cases} \tag{2.29}$$

$$V_{dc} = \delta_1^R v_{sab} + \delta_5^R v_{sbc} \tag{2.30}$$

Similarly to the previous technique, the duty-cycle computation is generalized to the defined current sectors by (2.31), which adapts the switching states and φ_{ref}^R according to Table 2.4.

$$\begin{cases} \delta_\rho^R = \dfrac{2}{\sqrt{3}\tan\left(\varphi_{ref}^R\right) + 3} \\ \delta_\sigma^R = \dfrac{\sqrt{3}\tan\left(\varphi_{ref}^R\right) + 1}{\sqrt{3}\tan\left(\varphi_{ref}^R\right) + 3} \end{cases} \tag{2.31}$$

Table 2.4. Generalization of the duty-cycles for the minimum dc-link voltage strategy.

Current Sector	**Vector** ρ	**Vector** σ	φ_{ref}^R
1	$1_{(ab)}$	$5_{(bc)}$	θ_i
2	$2_{(ac)}$	$4_{(ba)}$	$\theta_i - \pi/3$
3	$5_{(bc)}$	$7_{(ca)}$	$\theta_i - 2\pi/3$
4	$4_{(ba)}$	$8_{(cb)}$	$\theta_i - \pi$
5	$7_{(ca)}$	$1_{(ab)}$	$\theta_i - 4\pi/3$
6	$8_{(cb)}$	$2_{(ac)}$	$\theta_i - 5\pi/3$

The minimum dc-link voltage averaged within each switching period as function of the current-to-voltage displacement angle is given by (2.32).

$$V_{dc\,\min} = \frac{\sqrt{3}}{\sqrt{2}} v_{s\,rms} \cos(\phi_i) \tag{2.32}$$

It is worth mentioning that near the zone transitions, one of the vectors used in this modulation strategy may reach null voltage, this is visible in Fig. 2.4.(b). Even though for the computation of the duty cycles it was assumed that the input voltages and output currents are nearly constant during the switching period, in practical terms this may lead to negative dc-link voltage and consequently a short-circuit through the output stage diodes. This means that near the zone transition of the minimum dc-link voltage strategy, it may be required to change the input stage modulation strategy for the maximum dc-link voltage strategy to avoid negative dc-link voltages. Note that when the current-to-voltage displacement angle is non null, this situation happens every time the current reference vector sector is different than the voltage sector.

2.3 – Output Stage (Dual Voltage Source Inverter)

The output inverter stage of this topology is composed by an association of two VSIs sharing the same dc-link supply, as presented in Fig. 2.9. Regarding the bidirectional switches in the input CSR stage, this output inverter does not require special commutation logic other than the common deadtimes, as the dc-link voltage cannot be negative due to the presence of antiparallel diodes that ensure freewheeling paths for the inductive load currents.

At any given instant, if the upper switch of a given arm is ON (*xy*, for terminal *y* of output phase *x*), then the arm bottom switch must be OFF, $S_{xyu} = 1 \rightarrow S_{xyd} = 0$, and vice versa, $S_{xyd} = 1 \rightarrow S_{xyu} = 0$, to avoid short circuiting the dc-link. This allows the creation of a DVSI switching matrix, $\mathbf{S_{DVSI}}$, given by (2.33).

$$\mathbf{S_{DVSI}} = \begin{bmatrix} S_{A1u} - S_{A2u} \\ S_{B1u} - S_{B2u} \\ S_{C1u} - S_{C2u} \end{bmatrix} \tag{2.33}$$

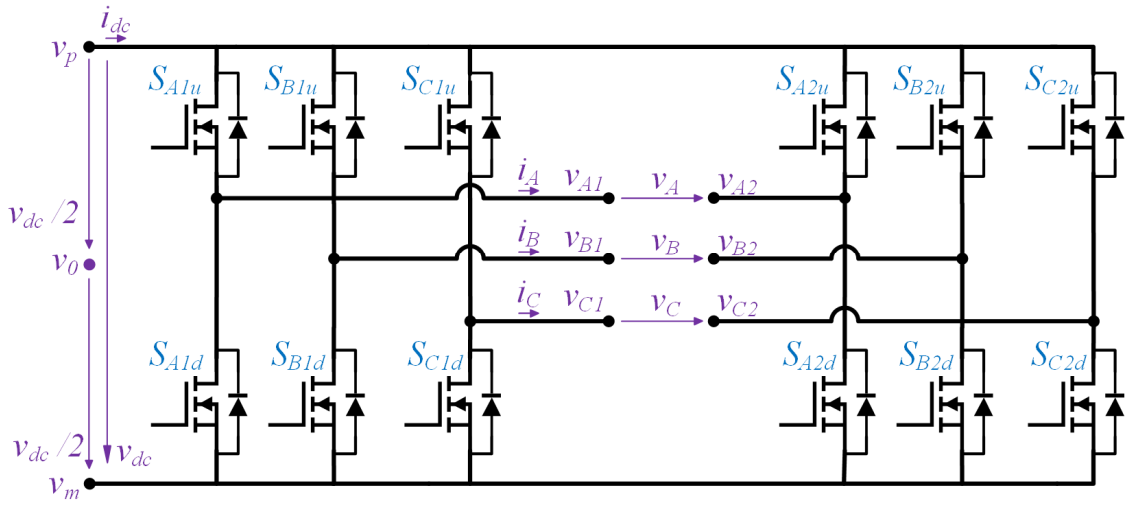


Fig. 2.9. Output stage topology based on DVSI sharing the same dc-bus.

The relations between the soft dc-link quantities and the output quantities are given by (2.34) for the voltages, where $\mathbf{v_{out}}$ is the output voltage vector, and by (2.35) for the currents, where $\mathbf{i_{out}}$ is the output current vector.

$$\mathbf{v_{out}} = \begin{bmatrix} v_A & v_B & v_C \end{bmatrix}^T = \mathbf{S_{DVSI}} v_{dc} \tag{2.34}$$

$$i_{dc} = \mathbf{S}_{\mathbf{DVSI}}^T \begin{bmatrix} i_A & i_B & i_C \end{bmatrix}^T = \mathbf{S}_{\mathbf{DVSI}}^T \mathbf{i_{out}} \tag{2.35}$$

The existence of six output arms allows 64 (2^6) different switching states that can be represented in an output stationary $\alpha\beta\gamma$ reference frame by using the Concordia transformation, (2.13), (2.14). The output voltage vector in the machine stationary $\alpha\beta\gamma$ reference frame is given by (2.36).

$$\mathbf{v_{out\,\alpha\beta\gamma}} = \mathbf{C v_{out}} = \mathbf{C S_{DVSI}} v_{dc} \tag{2.36}$$

As the two VSIs are supplied by a common dc-link, there are low impedance paths for zero sequence currents (ZSC) to flow [34][35]. These currents are originated by the zero-sequence voltage (the $\boldsymbol{\gamma}$ component of the output voltage vector). On conventional single-VSI variable speed drives, the $\boldsymbol{\gamma}$ component is also present in the output voltage vector but there are no paths for the ZSC to flow, not requiring special attention. On the other hand, maintaining the ZSC null must be enforced in the control of the IMC featuring a DVSI output with a common dc-bus [88].

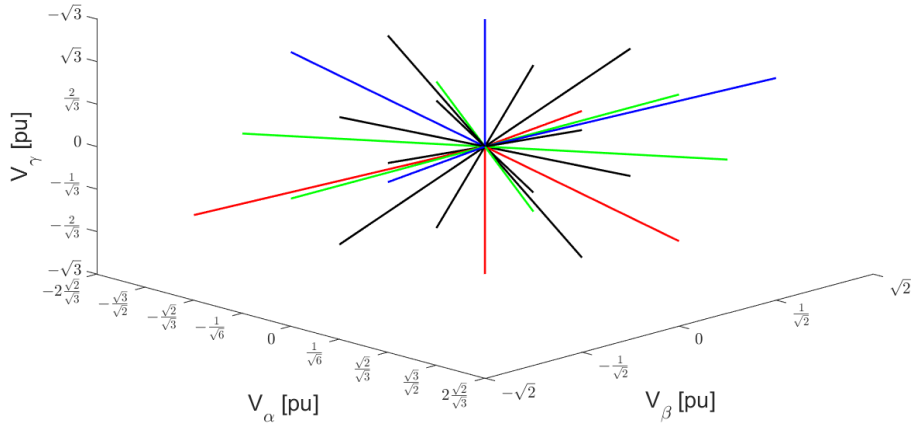
The resulting 64 output DVSI voltage vectors are presented in Table 2.5 along with their corresponding switching combinations, the output voltage in $\alpha\beta\gamma$ components in per units (p.u. with base voltage V_{dc}), their amplitude and argument in the $\alpha\beta$ plane, resulting soft dc-link current and corresponding DVSI contribution to CMV, v_{cm0}, obtained by (2.5). These vectors may be divided into three different groups according to their specific properties.

The first, Group I, corresponds to the switching states between 1 and 20, coloured as blue and red vectors in both Table 2.5 and Fig. 2.10 according to their zero-sequence voltage contribution (blue vectors have positive zero-sequence component, while red vectors possess negative zero-sequence component). This group of switching combinations allows the cancelation of the DVSI contribution to CMV ($v_{cm0} = 0$). On the other hand, these vectors have non-null zero-sequence voltage component ($\mathbf{v_{out\,\gamma}} \neq 0$) and their null vectors feature non-null dc-link current, requiring dedicated multistep commutation logic for the bidirectional switches safe commutation.

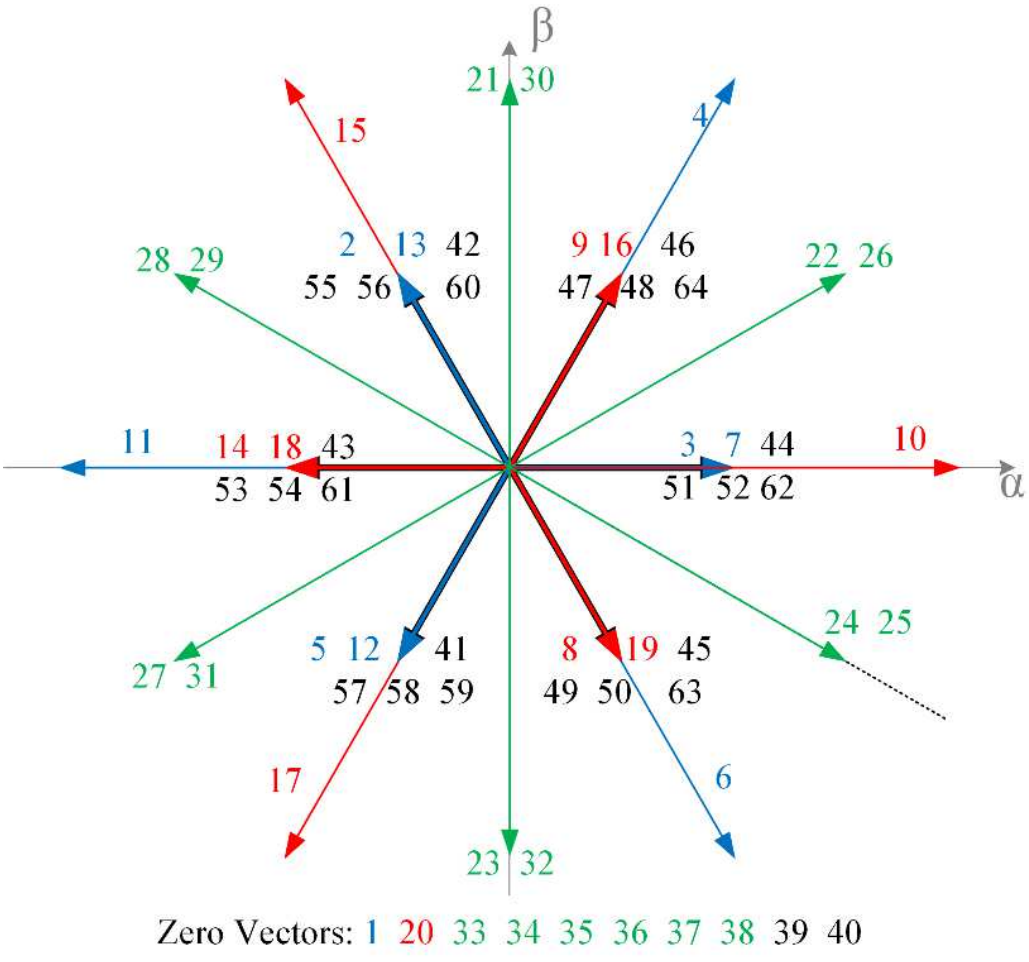
The second, Group II, corresponds to the switching states between 21 and 38, coloured as green vectors. These vectors are characterized by not originating ZSC as they show null zero-sequence voltage component. Within this group, there are pairs of two vectors that feature the same output voltage with symmetric DVSI contribution to CMV. An example of this is the pair composed by switching states 24 and 25. Another particularity of this group is that its null vectors result in null dc-link current.

The third and last, Group III, corresponds to the switching states between 39 and 64, black coloured. Vectors within this group are identical to the small vectors of Group I in terms of the output voltage vector in the $\alpha\beta$ plane. This third group of vectors have both non-zero contribution to the CMV and non-zero component of zero-sequence voltage, while their null vectors feature null dc-link current.

A three-dimensional graphic representation of these 64 switching states is presented in Fig. 2.10(a), where it is possible to visualize that these voltage vectors present distinct zero-sequence voltage components, in accordance with Table 2.5. A two-dimensional representation of these voltage vectors in the $\alpha\beta$ plane is shown in Fig. 2.10(b). Given that the groups of switching states feature different characteristics, by limiting the usable output vectors to a single group, it is possible to obtain different outcomes in terms of ZSC and CMV. Two modulation methods capable of achieving the full converter input to output voltage ratio have been proposed in the literature, one that only considers the vectors of group two ($\mathbf{v_{out\,\gamma}} = 0$) and a second with the objective of minimizing CMV that only considers the voltage vectors from Group I ($v_{cm0} = 0$).



(a)



(b)

Fig. 2.10. DVSI output voltage vectors coloured according to their group classification. (a) three-dimensional representation. (b) two-dimensional representation in the αβ plane.

Table 2.5: DVSI switching table with their corresponding output voltage in the machine stationary $\alpha\beta\gamma$ frame ($1pu = v_{dc}$), soft dc-link current, and contribution to CMV.

State	$[S_{A1u}\ S_{B1u}\ S_{C1u}\ S_{A2u}\ S_{B2u}\ S_{C2u}]$	$[v_{out\,\alpha};\ v_{out\,\beta};\ v_{out\,\gamma}]$ [pu]	$[v_{out\,\alpha\beta\gamma}]$ [pu]	$\measuredangle(v_{out\,\alpha\beta\gamma})$	i_{dc}	v_{cm0}
1	[1 1 1 0 0 0]	$[0;\ 0;\ \sqrt{3}]$	0	0	$i_A+i_B+i_C$	0
2	[1 1 0 1 0 0]	$[-1/\sqrt{6};\ 1/\sqrt{2};\ 1/\sqrt{3}]$	$\sqrt{2/3}$	$2\pi/3$	i_B	0
3	[1 1 0 0 1 0]	$[\sqrt{2/3};\ 0;\ 1/\sqrt{3}]$	$\sqrt{2/3}$	0	i_A	0
4	[1 1 0 0 0 1]	$[\sqrt{2/3};\ \sqrt{2};\ 1/\sqrt{3}]$	$2\sqrt{2/3}$	$\pi/3$	$i_A+i_B-i_C$	0
5	[1 0 1 1 0 0]	$[-1/\sqrt{6};\ -1/\sqrt{2};\ 1/\sqrt{3}]$	$\sqrt{2/3}$	$-2\pi/3$	i_C	0
6	[1 0 1 0 1 0]	$[\sqrt{2/3};\ -\sqrt{2};\ 1/\sqrt{3}]$	$2\sqrt{2/3}$	$-\pi/3$	$i_A-i_B+i_C$	0
7	[1 0 1 0 0 1]	$[\sqrt{2/3};\ 0;\ 1/\sqrt{3}]$	$\sqrt{2/3}$	0	i_A	0
8	[1 0 0 1 1 0]	$[1/\sqrt{6};\ -1/\sqrt{2};\ -1/\sqrt{3}]$	$\sqrt{2/3}$	$-\pi/3$	$-i_B$	0
9	[1 0 0 1 0 1]	$[1/\sqrt{6};\ 1/\sqrt{2};\ -1/\sqrt{3}]$	$\sqrt{2/3}$	$\pi/3$	$-i_C$	0
10	[1 0 0 0 1 1]	$[2\sqrt{2/3};\ 0;\ -1/\sqrt{3}]$	$2\sqrt{2/3}$	0	$i_A-i_B-i_C$	0
11	[0 1 1 1 0 0]	$[-2\sqrt{2/3};\ 0;\ 1/\sqrt{3}]$	$2\sqrt{2/3}$	π	$-i_A+i_B+i_C$	0
12	[0 1 1 0 1 0]	$[-1/\sqrt{6};\ -1/\sqrt{2};\ 1/\sqrt{3}]$	$\sqrt{2/3}$	$-2\pi/3$	i_C	0
13	[0 1 1 0 0 1]	$[-1/\sqrt{6};\ 1/\sqrt{2};\ 1/\sqrt{3}]$	$\sqrt{2/3}$	$2\pi/3$	i_B	0
14	[0 1 0 1 1 0]	$[-\sqrt{2/3};\ 0;\ -1/\sqrt{3}]$	$\sqrt{2/3}$	π	$-i_A$	0
15	[0 1 0 1 0 1]	$[-\sqrt{2/3};\ \sqrt{2};\ -1/\sqrt{3}]$	$2\sqrt{2/3}$	$2\pi/3$	$-i_A+i_B-i_C$	0
16	[0 1 0 0 1 1]	$[1/\sqrt{6};\ 1/\sqrt{2};\ -1/\sqrt{3}]$	$\sqrt{2/3}$	$\pi/3$	$-i_C$	0
17	[0 0 1 1 1 0]	$[-\sqrt{2/3};\ -\sqrt{2};\ -1/\sqrt{3}]$	$2\sqrt{2/3}$	$-2\pi/3$	$-i_A-i_B+i_C$	0
18	[0 0 1 1 0 1]	$[-\sqrt{2/3};\ 0;\ -1/\sqrt{3}]$	$\sqrt{2/3}$	π	$-i_A$	0
19	[0 0 1 0 1 1]	$[1/\sqrt{6};\ -1/\sqrt{2};\ -1/\sqrt{3}]$	$\sqrt{2/3}$	$-\pi/3$	$-i_B$	0
20	[0 0 0 1 1 1]	$[0;\ 0;\ -\sqrt{3}]$	0	0	$-i_A-i_B-i_C$	0
21	[1 1 0 1 0 1]	$[0;\ \sqrt{2};\ 0]$	$\sqrt{2}$	$\pi/2$	i_B-i_C	$v_{dc}/6$
22	[1 1 0 0 1 1]	$[\sqrt{3/2};\ 1/\sqrt{2};\ 0]$	$\sqrt{2}$	$\pi/6$	i_A-i_C	$v_{dc}/6$
23	[1 0 1 1 1 0]	$[0;\ -\sqrt{2};\ 0]$	$\sqrt{2}$	$-\pi/2$	$-i_B+i_C$	$v_{dc}/6$
24	[1 0 1 0 1 1]	$[\sqrt{3/2};\ -1/\sqrt{2};\ 0]$	$\sqrt{2}$	$-\pi/6$	i_A-i_B	$v_{dc}/6$
25	[1 0 0 0 1 0]	$[\sqrt{3/2};\ -1/\sqrt{2};\ 0]$	$\sqrt{2}$	$-\pi/6$	i_A-i_B	$-v_{dc}/6$
26	[1 0 0 0 0 1]	$[\sqrt{3/2};\ 1/\sqrt{2};\ 0]$	$\sqrt{2}$	$\pi/6$	i_A-i_C	$-v_{dc}/6$
27	[0 1 1 1 1 0]	$[-\sqrt{3/2};\ -1/\sqrt{2};\ 0]$	$\sqrt{2}$	$-5\pi/6$	$-i_A+i_C$	$v_{dc}/6$
28	[0 1 1 1 0 1]	$[-\sqrt{3/2};\ 1/\sqrt{2};\ 0]$	$\sqrt{2}$	$5\pi/6$	$-i_A+i_B$	$v_{dc}/6$
29	[0 1 0 1 0 0]	$[-\sqrt{3/2};\ 1/\sqrt{2};\ 0]$	$\sqrt{2}$	$5\pi/6$	$-i_A+i_B$	$-v_{dc}/6$
30	[0 1 0 0 0 1]	$[0;\ \sqrt{2};\ 0]$	$\sqrt{2}$	$\pi/2$	i_B-i_C	$-v_{dc}/6$
31	[0 0 1 1 0 0]	$[-\sqrt{3/2};\ -1/\sqrt{2};\ 0]$	$\sqrt{2}$	$-5\pi/6$	$-i_A+i_C$	$-v_{dc}/6$
32	[0 0 1 0 1 0]	$[0;\ -\sqrt{2};\ 0]$	$\sqrt{2}$	$-\pi/2$	$-i_B+i_C$	$-v_{dc}/6$
33	[1 1 0 1 1 0]	$[0;\ 0;\ 0]$	0	0	0	$v_{dc}/6$
34	[1 0 1 1 0 1]	$[0;\ 0;\ 0]$	0	0	0	$v_{dc}/6$
35	[1 0 0 1 0 0]	$[0;\ 0;\ 0]$	0	0	0	$-v_{dc}/6$
36	[0 1 1 0 1 1]	$[0;\ 0;\ 0]$	0	0	0	$v_{dc}/6$
37	[0 1 0 0 1 0]	$[0;\ 0;\ 0]$	0	0	0	$-v_{dc}/6$
38	[0 0 1 0 0 1]	$[0;\ 0;\ 0]$	0	0	0	$-v_{dc}/6$
39	[1 1 1 1 1 1]	$[0;\ 0;\ 0]$	0	0	0	$v_{dc}/2$
40	[0 0 0 0 0 0]	$[0;\ 0;\ 0]$	0	0	0	$-v_{dc}/2$
41	[1 1 1 1 1 0]	$[-1/\sqrt{6};\ -1/\sqrt{2};\ 1/\sqrt{3}]$	$\sqrt{2/3}$	$-2\pi/3$	i_C	$v_{dc}/3$
42	[1 1 1 1 0 1]	$[-1/\sqrt{6};\ 1/\sqrt{2};\ 1/\sqrt{3}]$	$\sqrt{2/3}$	$2\pi/3$	i_B	$v_{dc}/3$
43	[1 1 1 1 0 0]	$[-\sqrt{2/3};\ 0;\ 2/\sqrt{3}]$	$\sqrt{2/3}$	π	i_B+i_C	$v_{dc}/6$
44	[1 1 1 0 1 1]	$[\sqrt{2/3};\ 0;\ 1/\sqrt{3}]$	$\sqrt{2/3}$	0	i_A	$v_{dc}/3$
45	[1 1 1 0 1 0]	$[1/\sqrt{6};\ -1/\sqrt{2};\ 2/\sqrt{3}]$	$\sqrt{2/3}$	$-\pi/3$	i_A+i_C	$v_{dc}/6$
46	[1 1 1 0 0 1]	$[1/\sqrt{6};\ 1/\sqrt{2};\ 2/\sqrt{3}]$	$\sqrt{2/3}$	$\pi/3$	i_A+i_B	$v_{dc}/6$
47	[1 1 0 1 1 1]	$[1/\sqrt{6};\ 1/\sqrt{2};\ -1/\sqrt{3}]$	$\sqrt{2/3}$	$\pi/3$	$-i_C$	$v_{dc}/3$
48	[1 1 0 0 0 0]	$[1/\sqrt{6};\ 1/\sqrt{2};\ 2/\sqrt{3}]$	$\sqrt{2/3}$	$\pi/3$	i_A+i_B	$-v_{dc}/6$
49	[1 0 1 1 1 1]	$[1/\sqrt{6};\ -1/\sqrt{2};\ -1/\sqrt{3}]$	$\sqrt{2/3}$	$-\pi/3$	$-i_B$	$v_{dc}/3$
50	[1 0 1 0 0 0]	$[1/\sqrt{6};\ -1/\sqrt{2};\ 2/\sqrt{3}]$	$\sqrt{2/3}$	$-\pi/3$	i_A+i_C	$-v_{dc}/6$
51	[1 0 0 1 1 1]	$[\sqrt{2/3};\ 0;\ -2/\sqrt{3}]$	$\sqrt{2/3}$	0	$-i_B-i_C$	$v_{dc}/6$
52	[1 0 0 0 0 0]	$[\sqrt{2/3};\ 0;\ 1/\sqrt{3}]$	$\sqrt{2/3}$	0	i_A	$-v_{dc}/3$
53	[0 1 1 1 1 1]	$[-\sqrt{2/3};\ 0;\ -1/\sqrt{3}]$	$\sqrt{2/3}$	π	$-i_A$	$v_{dc}/3$
54	[0 1 1 0 0 0]	$[-\sqrt{2/3};\ 0;\ 2/\sqrt{3}]$	$\sqrt{2/3}$	π	i_B+i_C	$-v_{dc}/6$
55	[0 1 0 1 1 1]	$[-1/\sqrt{6};\ 1/\sqrt{2};\ -2/\sqrt{3}]$	$\sqrt{2/3}$	$2\pi/3$	$-i_A-i_C$	$v_{dc}/6$
56	[0 1 0 0 0 0]	$[-1/\sqrt{6};\ 1/\sqrt{2};\ 1/\sqrt{3}]$	$\sqrt{2/3}$	$2\pi/3$	i_B	$-v_{dc}/3$
57	[0 0 1 1 1 1]	$[-1/\sqrt{6};\ -1/\sqrt{2};\ -2/\sqrt{3}]$	$\sqrt{2/3}$	$-2\pi/3$	$-i_A-i_B$	$v_{dc}/6$
58	[0 0 1 0 0 0]	$[-1/\sqrt{6};\ -1/\sqrt{2};\ 1/\sqrt{3}]$	$\sqrt{2/3}$	$-2\pi/3$	i_C	$-v_{dc}/3$
59	[0 0 0 1 1 0]	$[-1/\sqrt{6};\ -1/\sqrt{2};\ -2/\sqrt{3}]$	$\sqrt{2/3}$	$-2\pi/3$	$-i_A-i_B$	$-v_{dc}/6$
60	[0 0 0 1 0 1]	$[-1/\sqrt{6};\ 1/\sqrt{2};\ -2/\sqrt{3}]$	$\sqrt{2/3}$	$2\pi/3$	$-i_A-i_C$	$-v_{dc}/6$
61	[0 0 0 1 0 0]	$[-\sqrt{2/3};\ 0;\ -1/\sqrt{3}]$	$\sqrt{2/3}$	π	$-i_A$	$-v_{dc}/3$
62	[0 0 0 0 1 1]	$[\sqrt{2/3};\ 0;\ -2/\sqrt{3}]$	$\sqrt{2/3}$	0	$-i_B-i_C$	$-v_{dc}/6$
63	[0 0 0 0 1 0]	$[1/\sqrt{6};\ -1/\sqrt{2};\ -1/\sqrt{3}]$	$\sqrt{2/3}$	$-\pi/3$	$-i_B$	$-v_{dc}/3$
64	[0 0 0 0 0 1]	$[1/\sqrt{6};\ 1/\sqrt{2};\ -1/\sqrt{3}]$	$\sqrt{2/3}$	$\pi/3$	$-i_C$	$-v_{dc}/3$

2.3.1 – DVSI output voltage modulation without ZSC

The SVM without ZSC strategy considers only the vectors that do not generate zero-sequence voltage across the load. Some authors consider the zero-sequence component of the output voltage ($\mathbf{v}_{\mathbf{out}\,\gamma}$) as CMV across load phases as referred in [83]. This component is responsible for creating ZSCs in the machine, but not the currents flowing through the bearings [19][80][94]. It may be important to remember that in this document, the definition of CMV in an OEW machine is given by (2.1), while the zero-sequence component of the output voltage is the resulting γ component obtained by the Concordia and Park transformations.

The graphical representation of the output voltage vectors without zero-sequence voltage, in the $\alpha\beta$ plane, is shown in Fig. 2.11. Note that the reference vector may be in one of six output voltage sectors, being synthetized by the two adjacent vectors and by the null vector requiring the least number of commutations.

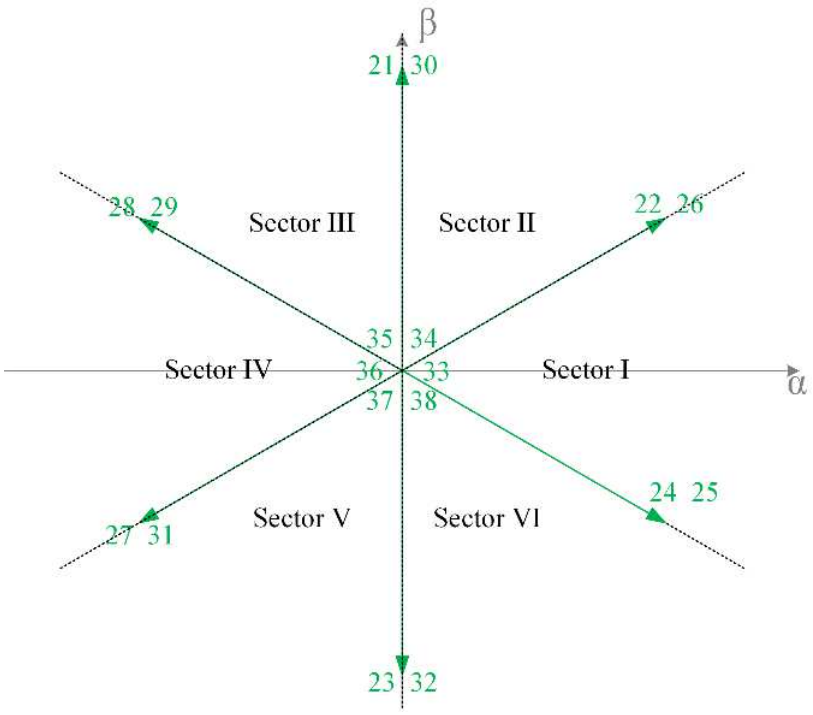
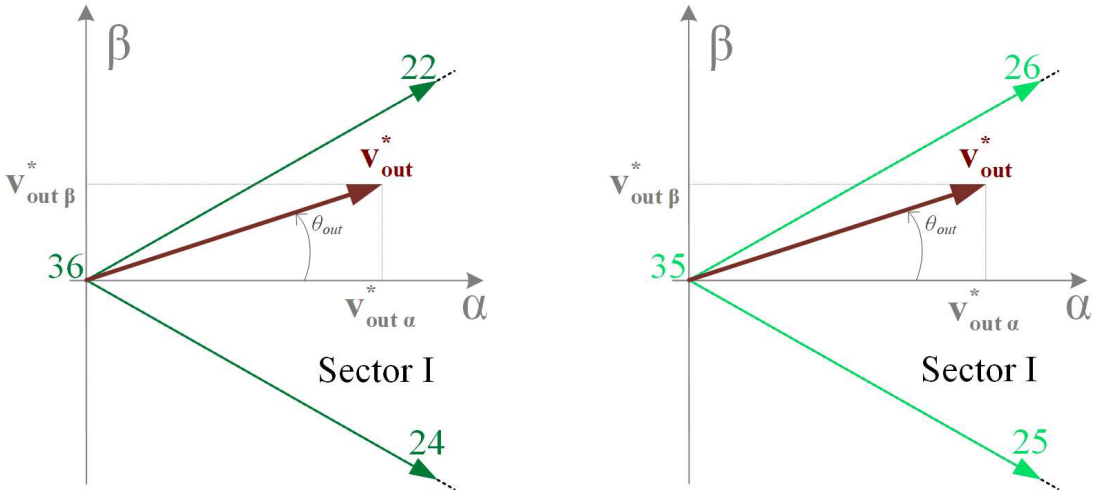


Fig. 2.11. DVSI output voltage vectors with null contribution to ZSC.

Consider an output voltage reference vector, $\mathbf{v}_{\mathbf{out}}^{*}$, in sector I with an angle θ_{out} as shown in Fig. 2.12. It has 4 adjacent vectors: 22, 24, 25 and 26. Note that vector 22 is identical to vector 26 in terms of output voltage, while vector 24 is identical to vector 25, being their only difference the number of DVSI upper switches turned ON (N_{sw}). To reduce the number of required

commutations within a switching period, these vectors are generally divided into two sets according to the N_{sw} of each switching state. The SVM strategy is then based in either of these two sets. Note that the null vectors are different for both sets. Let us call the switching states with $N_{sw} = 4$ as set I and the switching states with $N_{sw} = 2$ as set II.



(a) (b)

Fig. 2.12. Modulation of an output voltage reference vector located in Sector I. (a) with set I vectors. (b) with set II vectors.

Considering the scenario presented in Fig. 2.12(a), the output voltage reference is modulated by the active vectors 22 and 24 and by the null vector 36, whose analytical expressions are obtainable from Table 2.5, given by (2.37).

$$\begin{cases} \mathbf{v_{22}} = V_{dc}\left(\sqrt{3/2}\,\boldsymbol{\alpha} + 1/\sqrt{2}\,\boldsymbol{\beta}\right) \\ \mathbf{v_{24}} = V_{dc}\left(\sqrt{3/2}\,\boldsymbol{\alpha} - 1/\sqrt{2}\,\boldsymbol{\beta}\right) \\ \mathbf{v_{36}} = 0 \end{cases} \tag{2.37}$$

The resulting output voltage vector is synthetized by the weighted average of the adjacent switching states as given by (2.38), being δ^I_{22}, δ^I_{24} and δ^I_{36} the corresponding duty-cycles regarding the switching period where each of the switching states is applied. Note that the sum of these duty - cycles must correspond to the entire switching period ($\delta^I_{22}+\delta^I_{24}+\delta^I_{36} = 1$) and that the resulting output voltage vector has null zero-sequence voltage component.

$$\begin{aligned} \mathbf{v_{out}} &= \delta^I_{22}\mathbf{v_{22}} + \delta^I_{24}\mathbf{v_{24}} + \delta^I_{36}\mathbf{v_{36}} \\ &= V_{dc}\left[\frac{\sqrt{3}}{\sqrt{2}}\left(\delta^I_{22} + \delta^I_{24}\right)\boldsymbol{\alpha} + \frac{1}{\sqrt{2}}\left(\delta^I_{22} - \delta^I_{24}\right)\boldsymbol{\beta}\right] \end{aligned} \tag{2.38}$$

The duty-cycles that lead to the output voltage reference vector are obtained by solving the system of equations given by (2.39).

$$\begin{cases} \mathbf{v}_{\mathbf{out}\,\alpha}^{*} = \dfrac{\sqrt{3}\,V_{dc}}{\sqrt{2}}\left(\delta_{22}^{I}+\delta_{24}^{I}\right) \\ \mathbf{v}_{\mathbf{out}\,\beta}^{*} = \dfrac{V_{dc}}{\sqrt{2}}\left(\delta_{22}^{I}-\delta_{24}^{I}\right) \\ \delta_{22}^{I}+\delta_{24}^{I}+\delta_{36}^{I}=1 \end{cases} \Rightarrow \begin{cases} \delta_{24}^{I} = \dfrac{1}{\sqrt{6}}\dfrac{\mathbf{v}_{\mathbf{out}\,\alpha}^{*}}{V_{dc}} - \dfrac{1}{\sqrt{2}}\dfrac{\mathbf{v}_{\mathbf{out}\,\beta}^{*}}{V_{dc}} \\ \delta_{22}^{I} = \dfrac{1}{\sqrt{6}}\dfrac{\mathbf{v}_{\mathbf{out}\,\alpha}^{*}}{V_{dc}} + \dfrac{1}{\sqrt{2}}\dfrac{\mathbf{v}_{\mathbf{out}\,\beta}^{*}}{V_{dc}} \\ \delta_{36}^{I} = 1 - \dfrac{\sqrt{2}}{\sqrt{3}}\dfrac{\mathbf{v}_{\mathbf{out}\,\alpha}^{*}}{V_{dc}} \end{cases} \tag{2.39}$$

The formulation presented in (2.39) is only valid for an output reference vector located in sector I.

$$\left\|\mathbf{v}_{\mathbf{out}\,\alpha\beta}^{*}\right\| = \sqrt{\left(\mathbf{v}_{\mathbf{out}\,\alpha}^{*}\right)^{2}+\left(\mathbf{v}_{\mathbf{out}\,\beta}^{*}\right)^{2}} \tag{2.40}$$

Defining the amplitude of the output voltage vector in the $\alpha\beta$ plane as $\left\|\mathbf{v}_{\mathbf{out}\,\alpha\beta}^{*}\right\|$, given by (2.40) , a generalization of the duty-cycles for any sector may be obtained by selecting a reference angle, φ_{ref}^{I} . The duty-cycles are then computed through (2.41), where the indexes 'κ', 'λ' denote the adjacent active vectors of the output voltage reference vector and the index 'o' denote the null vector that requires the least amount of commutations. The corresponding switching states and reference angle for both sets of vectors indicated in Table 2.6, with θ_{out} defined by the angle between the output voltage reference vector and the α axis, as shown in Fig. 2.12.

$$\begin{cases} \delta_{\kappa}^{I} = \dfrac{\left\|\mathbf{v}_{\mathbf{out}\,\alpha\beta}^{*}\right\|}{V_{dc}}\left(\dfrac{\cos\left(\varphi_{ref}^{I}\right)}{\sqrt{6}} - \dfrac{\sin\left(\varphi_{ref}^{I}\right)}{\sqrt{2}}\right) \\ \delta_{\lambda}^{I} = \dfrac{\left\|\mathbf{v}_{\mathbf{out}\,\alpha\beta}^{*}\right\|}{V_{dc}}\left(\dfrac{\cos\left(\varphi_{ref}^{I}\right)}{\sqrt{6}} + \dfrac{\sin\left(\varphi_{ref}^{I}\right)}{\sqrt{2}}\right) \\ \delta_{o}^{I} = 1 - \dfrac{\sqrt{2}}{\sqrt{3}}\dfrac{\left\|\mathbf{v}_{\mathbf{out}\,\alpha\beta}^{*}\right\|}{V_{dc}}\cos\left(\varphi_{ref}^{I}\right) \end{cases} \tag{2.41}$$

Table 2.6: Generalization of duty-cycles for output voltage modulation without ZSCs.

Sector	Set 1 ($N_{sw}=4$)				Set 2 ($N_{sw}=2$)			
	Vector κ	Vector λ	Vector o	φ_{ref}^{I}	Vector κ	Vector λ	Vector o	φ_{ref}^{I}
I	24	22	36	θ_{at}	25	26	35	θ_{at}
II	22	21	33	$\theta_{out}-\pi/3$	26	30	38	$\theta_{out}-\pi/3$
III	21	28	34	$\theta_{out}-2\pi/3$	30	29	37	$\theta_{out}-2\pi/3$
IV	28	27	36	$\theta_{out}-\pi$	29	31	35	$\theta_{out}-\pi$
V	27	23	33	$\theta_{out}-4\pi/3$	31	32	38	$\theta_{out}-4\pi/3$
VI	23	24	34	$\theta_{out}-5\pi/3$	32	25	37	$\theta_{out}-5\pi/3$

2.3.2 – DVSI output voltage modulation without V_{cm0}

To minimizing CMV, the authors of [80] proposed a SVM strategy that only considers the DVSI Group I switching states featuring null contribution to CMV (red and blue vectors), presented in Fig. 2.13. Note that the $\alpha\beta$ plane is once again divided in six sectors, being the sector limits shifted by 30 degrees in respect to the previously presented modulation method.

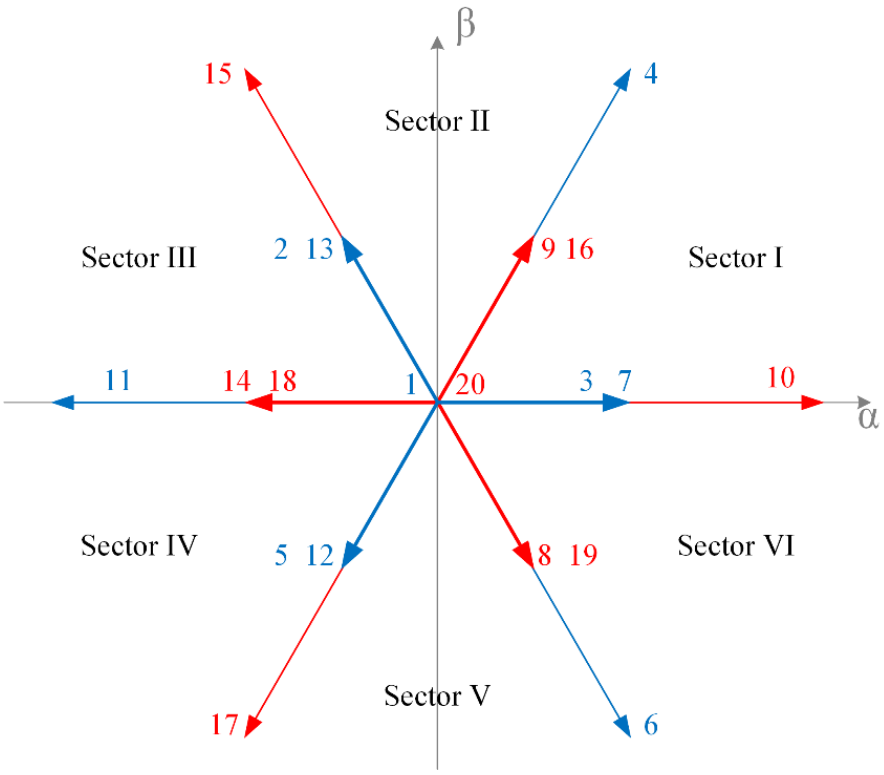


Fig. 2.13. DVSI output voltage vectors with null contribution to V_{cm0}.

As vectors in the first group feature non-null instantaneous zero-sequence voltage ($\mathbf{v_{out\,\gamma}} \neq 0$) the elimination of ZSCs must be accomplished through modulation in every switching period. Each output voltage vector can be modulated by the two adjacent active vectors and the two zero vectors. Since the two zero vectors have opposite contributions to zero-sequence voltage, they may be weighted in a way that guarantees null average zero-sequence voltage every switching period.

Let us consider the output voltage reference vector located in sector I, shown in Fig. 2.14.

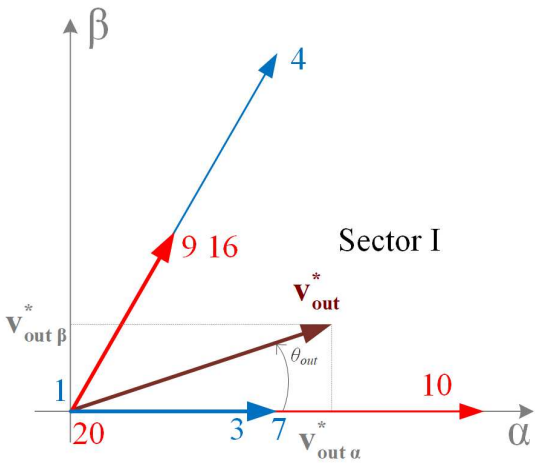


Fig. 2.14. Modulation of an output voltage reference vector located in Sector I with Group I switching states.

The adjacent active switching states are vectors 10 and 4 (high amplitude vectors) and vectors 3, 7, 9 and 16 (small amplitude vectors). Contrary to the usage of switching states in the input stage with lower dc-link voltage to reduce the switching losses of the output stage, the usage of small amplitude vectors on the output stage does not offer significant advantage due to most of the output voltage THD being consequence of the supplied zero-sequence component. For this reason, only the high amplitude vectors are considered for this modulation strategy. For a sector I output voltage vectors, the SVM strategy will consider switching states 1, 4, 10 and 20, given by (2.42).

$$\begin{cases} \mathbf{v_{10}} = V_{dc}\left(2\sqrt{2/3}\,\boldsymbol{\alpha} - \sqrt{1/3}\,\boldsymbol{\gamma}\right) \\ \mathbf{v_{4}} = V_{dc}\left(\sqrt{2/3}\,\boldsymbol{\alpha} + \sqrt{2}\,\boldsymbol{\beta} + \sqrt{1/3}\,\boldsymbol{\gamma}\right) \\ \mathbf{v_{1}} = V_{dc}\left(\sqrt{3}\,\boldsymbol{\gamma}\right) \\ \mathbf{v_{20}} = V_{dc}\left(-\sqrt{3}\,\boldsymbol{\gamma}\right) \end{cases} \tag{2.42}$$

The resulting output voltage vector is obtained through a weighted average of the considered switching states, as given by (2.43).

$$\begin{aligned}\mathbf{v}_{\mathbf{out}} &= \delta_{10}^{I}\mathbf{v}_{\mathbf{10}} + \delta_{4}^{I}\mathbf{v}_{\mathbf{4}} + \delta_{1}^{I}\mathbf{v}_{\mathbf{1}} + \delta_{20}^{I}\mathbf{v}_{\mathbf{20}} \\ &= V_{dc}\left[\frac{\sqrt{2}}{\sqrt{3}}\left(2\delta_{10}^{I}+\delta_{4}^{I}\right)\boldsymbol{\alpha} + \sqrt{2}\left(\delta_{4}^{I}\right)\boldsymbol{\beta} + \sqrt{1/3}\left(-\delta_{10}^{I}+\delta_{4}^{I}+3\delta_{1}^{I}-3\delta_{20}^{I}\right)\boldsymbol{\gamma}\right]\end{aligned} \tag{2.43}$$

The duty-cycles that lead to the output voltage reference vector are obtained by solving the system of equations given by (2.44).

$$\begin{cases}\mathbf{v}_{\mathbf{out}\,\alpha}^{*} = V_{dc}\dfrac{\sqrt{2}}{\sqrt{3}}\left(2\delta_{10}^{I}+\delta_{4}^{I}\right) \\ \mathbf{v}_{\mathbf{out}\,\beta}^{*} = V_{dc}\sqrt{2}\left(\delta_{4}^{I}\right) \\ \mathbf{v}_{\mathbf{out}\,\gamma}^{*} = V_{dc}\sqrt{1/3}\left(-\delta_{10}^{I}+\delta_{4}^{I}+3\delta_{1}^{I}-3\delta_{20}^{I}\right) \\ \delta_{10}^{I}+\delta_{4}^{I}+\delta_{1}^{I}+\delta_{20}^{I}=1\end{cases} \Rightarrow \begin{cases}\delta_{10}^{I} = \dfrac{\sqrt{3}}{2\sqrt{2}}\dfrac{\mathbf{v}_{\mathbf{out}\,\alpha}^{*}}{V_{dc}} - \dfrac{1}{2\sqrt{2}}\dfrac{\mathbf{v}_{\mathbf{out}\,\beta}^{*}}{V_{dc}} \\ \delta_{4}^{I} = \dfrac{1}{\sqrt{2}}\dfrac{\mathbf{v}_{\mathbf{out}\,\beta}^{*}}{V_{dc}} \\ \delta_{1}^{I} = -\dfrac{1}{2\sqrt{6}}\dfrac{\mathbf{v}_{\mathbf{out}\,\alpha}^{*}}{V_{dc}} - \dfrac{1}{2\sqrt{2}}\dfrac{\mathbf{v}_{\mathbf{out}\,\beta}^{*}}{V_{dc}} + \dfrac{1}{2\sqrt{3}}\dfrac{\mathbf{v}_{\mathbf{out}\,\gamma}^{*}}{V_{dc}} + \dfrac{1}{2} \\ \delta_{20}^{I} = -\dfrac{1}{\sqrt{6}}\dfrac{\mathbf{v}_{\mathbf{out}\,\alpha}^{*}}{V_{dc}} - \dfrac{1}{2\sqrt{3}}\dfrac{\mathbf{v}_{\mathbf{out}\,\gamma}^{*}}{V_{dc}} + \dfrac{1}{2}\end{cases} \tag{2.44}$$

For generalization of the duty-cycles to the remaining sectors, it is important to take a closer look at Fig. 2.13, where it is seen that the zero-sequence contribution of the active vectors may be symmetric depending on the output voltage vector reference being in an odd or even numbered sector. The generalization of the duty-cycles for the six sectors is given by (2.45), with the corresponding switching states and reference angle indicated in Table 2.7. Recall that $\left\|\mathbf{v}_{\mathbf{out}\,\alpha\beta}^{*}\right\|$ is the amplitude of the output reference vector in the $\alpha\beta$ plane, (2.40).

Due to the distinct zero-sequence voltage contribution of the active vectors according to the location of the output reference vector in an odd or even zone, the null vectors (vectors o_1 and o_2) also change depending on the output sector being odd or even.

The formulation given by (2.45), allows the modulation of an output voltage reference vector with adjustable zero-sequence voltage component. This is relevant when the electric machine to be supplied is a PMSM, where adjustable zero-sequence voltage is important to cancel the third harmonic of the electromotive force [94]. For induction machines and SynRMs, the zero-sequence loop voltage source is only determined by the zero-sequence voltage component of the DVSI. Thus, to maintain null ZSC in induction machines and SynRMs it is sufficient get rid of DVSI modulated zero-sequence voltages.

$$\begin{cases} \delta_{\kappa}^{I} = \dfrac{\left\|\mathbf{v}_{\mathbf{o}\,\alpha\beta}^{*}\right\|}{V_{dc}}\left(\dfrac{\sqrt{3}\cos\left(\varphi_{ref}^{I}\right)}{2\sqrt{2}} - \dfrac{\sin\left(\varphi_{ref}^{I}\right)}{2\sqrt{2}}\right) \\ \delta_{\lambda}^{I} = \dfrac{\left\|\mathbf{v}_{\mathbf{o}\,\alpha\beta}^{*}\right\|}{V_{dc}}\dfrac{\sin\left(\varphi_{ref}^{I}\right)}{\sqrt{2}} \\ \delta_{o1}^{I} = \dfrac{\left\|\mathbf{v}_{\mathbf{o}\,\alpha\beta}^{*}\right\|}{V_{dc}}\left(-\dfrac{\cos\left(\varphi_{ref}^{I}\right)}{2\sqrt{6}} - \dfrac{\sin\left(\varphi_{ref}^{I}\right)}{2\sqrt{2}}\right) + \dfrac{1}{2\sqrt{3}}\dfrac{\mathbf{v}_{\mathbf{out}\,\gamma}^{*}}{V_{dc}} + \dfrac{1}{2} \\ \delta_{o2}^{I} = \dfrac{\left\|\mathbf{v}_{\mathbf{o}\,\alpha\beta}^{*}\right\|}{V_{dc}}\left(-\dfrac{\cos\left(\varphi_{ref}^{I}\right)}{\sqrt{6}}\right) - \dfrac{1}{2\sqrt{3}}\dfrac{\mathbf{v}_{\mathbf{out}\,\gamma}^{*}}{V_{dc}} + \dfrac{1}{2} \end{cases} \tag{2.45}$$

Table 2.7: Generalization of the duty-cycles for output voltage modulation without V_{cm0}.

Sector	**Vector** κ	**Vector** λ	**Vector** $o1$	**Vector** $o2$	φ_{ref}^{I}
I	10	4	1	20	θ_{out}
II	4	15	20	1	$\theta_{out} - \pi/3$
III	15	11	1	20	$\theta_{out} - 2\pi/3$
IV	11	17	20	1	$\theta_{out} - \pi$
V	17	6	1	20	$\theta_{out} - 4\pi/3$
VI	6	10	20	1	$\theta_{out} - 5\pi/3$

To conclude the output voltage modulation section, it is important to mention that the active voltage vectors featured in both modulation strategies presented above, hold different magnitudes in the $\alpha\beta$ plane. Intuitively one would imagine that this would result in different converter voltage gains, but since the elimination of the average zero-sequence voltage component must be added to the modulation when using DVSI Group I vectors, the resulting maximum output voltage vector magnitude is identical in both modulation methods. Thus, in both strategies, the maximum output voltage waveform root mean square value that is possible to be modulated is given by (2.46).

$$v_{out\,rms} = \frac{V_{dc}}{\sqrt{2}} \tag{2.46}$$

2.4 – Association of the CSR and DVSI

In sections 2.2 and 2.3, both input and output stages were considered on their own. Considering that the switching frequency is high enough so that the CSR input voltages and DVSI output currents remain nearly constant through the switching period, it is possible to combine the modulation of the CSR and the DVSI. The dc-link voltage to be considered in the DVSI modulation should be the average dc-link voltage that results from the input stage modulation through (2.25). The association of both stages is then achieved combining their individual duty - cycles, by multiplying the duty-cycles of each individual stage.

As the DVSI modulation with vectors from Group I uses two zero vectors to reach null zero-sequence voltage average value, while the modulation using vectors from Group II only requires one zero vector, the resulting combined duty-cycles differ in both cases. The resulting duty-cycles for DVSI Group I modulation are given by (2.47), while the duty-cycles for DVSI Group II switching states are given by (2.48).

$$\begin{cases} \delta_{\rho\kappa} = \delta_{\rho}^{R}\delta_{\kappa}^{I} \\ \delta_{\rho\lambda} = \delta_{\rho}^{R}\delta_{\lambda}^{I} \\ \delta_{\rho o1} = \delta_{\rho}^{R}\delta_{o1}^{I} \\ \delta_{\rho o2} = \delta_{\rho}^{R}\delta_{o2}^{I} \\ \delta_{\sigma\kappa} = \delta_{\sigma}^{R}\delta_{\kappa}^{I} \\ \delta_{\sigma\lambda} = \delta_{\sigma}^{R}\delta_{\lambda}^{I} \\ \delta_{\sigma o1} = \delta_{\sigma}^{R}\delta_{o1}^{I} \\ \delta_{\sigma o2} = \delta_{\sigma}^{R}\delta_{o2}^{I} \end{cases} \tag{2.47}$$

$$\begin{cases} \delta_{\rho\kappa} = \delta_{\rho}^{R}\delta_{\kappa}^{I} \\ \delta_{\rho\lambda} = \delta_{\rho}^{R}\delta_{\lambda}^{I} \\ \delta_{\rho o} = \delta_{\rho}^{R}\delta_{o}^{I} \\ \delta_{\sigma\kappa} = \delta_{\sigma}^{R}\delta_{\kappa}^{I} \\ \delta_{\sigma\lambda} = \delta_{\sigma}^{R}\delta_{\lambda}^{I} \\ \delta_{\sigma o} = \delta_{\sigma}^{R}\delta_{o}^{I} \end{cases} \tag{2.48}$$

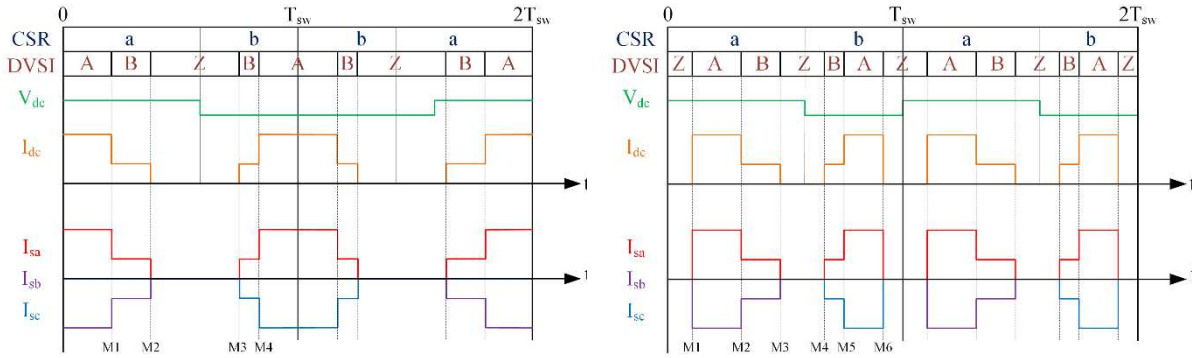
The methods presented above indicate which vectors should be applied during a respective duty-cycle. There is more than one way of structuring the pattern for them to be applied throughout each switching period. Depending on the priorities of the design, some switching

patterns may improve the quality of the input currents at the cost of increasing the switching losses or the other way around.

As an example, consider both switching patterns presented in Fig. 2.15 for an arbitrary scenario where two full switching cycles are represented. The organization of the switching pattern from Fig. 2.15(a) results in four (M1-M4) changes of DVSI switching state per switching period, while the pattern from Fig. 2.15(b) results in six (M1-M6). Thus, the DVSI switching losses for the switching pattern of Fig. 2.15(b) would be approximately 50% higher than the case of Fig. 2.15(a). On the other hand, observing the input current waveforms from both cases, it is concluded that the effective frequency seen by the CSR input filter is doubled by the second switching pattern, which would improve the input currents THDs or allow a reduced input filter size, or even a decrease in the switching frequency to a point where the switching losses would be comparable to the first scenario. For these reasons, the second switching pattern structure is chosen to be applied from this point onwards.

The detailed structure of a switching period featuring DVSI vectors from Group I has been proposed by authors of [88], shown in Fig. 2.16, while for DVSI vectors from Group II it is shown in Fig. 2.17.

Simulation results for the SVM strategies discussed in this chapter are presented in the next section, where the techniques are compared in terms of input and output waveforms THD and in terms of CMV supplied to the load.



(a) (b)

Fig. 2.15. Two different patterns in which the switching period can be arranged. (a) Pattern that minimizes DVSI switching losses at the cost of higher input current THDs. (b) Pattern with improved input currents THDs at the cost of higher DVSI switching losses.

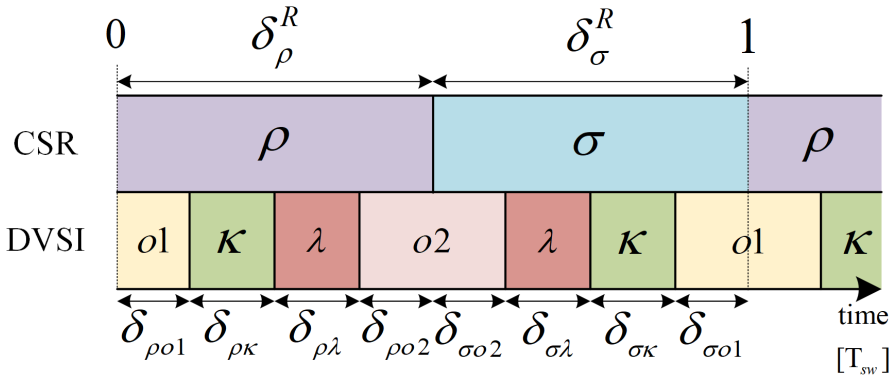


Fig. 2.16. Switching period structure for SVM strategy with DVSI Group I vectors.

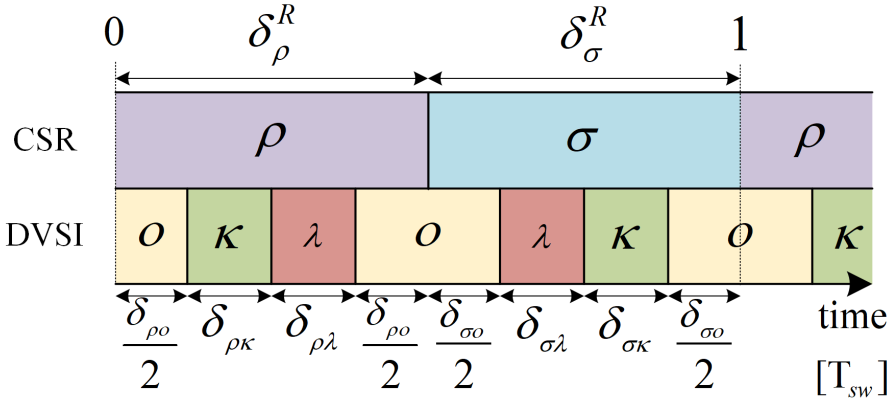


Fig. 2.17. Switching period structure for SVM strategy with DVSI Group II vectors.

2.5 – Analysis of OEW IMC SVM Methods

The modulation methods discussed in the previous sections have been implemented in a Model-Based simulation, using MATLAB®/Simulink software, supplying a fixed three-phase OEW RL series load (R_{load} and L_{load}). The switching devices were considered to be ideal (not requiring deadtimes or other special commutation logic).

For comparison purposes, the output frequency is maintained fixed, while the output voltage reference root mean square value is varied. Comparisons between the SVM strategies with reduced dc-link voltage and maximum dc-link voltage are presented in subsection 2.5.1, while a comparison between SVM strategies with output stage Groups I and II switching states is carried afterwards, in subsection 2.5.2.

The simulation model parameters are indicated in Table 2.8, where f_{sw} is the SVM switching frequency, f_o is the modulated output voltage waveform frequency, f_i is the input grid frequency,

$V_{ph\ rms}$ is the grid phase to neutral root mean square voltage and L_{cc} is the grid short circuit inductance. The filter components placement was indicated in Fig. 2.1.

Table 2.8: Simulation model parameters.

Simulation	T_s	200 [ns]
SVM	f_{sw}	50 [kHz]
	f_o	60 [Hz]
grid	f_i	50 [Hz]
	$V_{ph\ rms}$	230 [V]
	L_{cc}	50 [μH]
Filter	C_f	2 [μF]
	L_f	2 [mH]
	R_f	40 [Ω]
Load	R_{load}	100 [Ω]
	L_{load}	20 [mH]

2.5.1 – Reduced dc-link voltage strategy vs Maximum dc-link voltage strategy

As introduced in section 2.2, the converter operation under low output voltage requirements may use two different CSR modulation techniques. For higher output voltage requirements, only the modulation strategy with maximum dc-link voltage is viable. Concerning the output stage, the maximum output voltage without overmodulation, is given by (2.46) for both DVSI modulation techniques discussed in section 2.2. Considering the data provided in Table 2.8, the maximum possible root mean square value of output phase voltage for the CSR modulation strategy with reduced dc-link voltage is approximately 199V ($\sqrt{3}V_{ph\ rms}/2$), while for the maximum dc-link voltage strategy it is 345V ($3V_{ph\ rms}/2$). The maximum possible root mean square value of output phase voltage is obtained as given by (2.46). The average dc-link voltage of the maximum dc-link voltage strategy is given by (2.26), while for the reduced dc-link voltage strategy is given by (2.32).

This subsection is focused on the comparison of the two input stage modulation techniques. Therefore, the output stage modulation method remains unchanged, the strategy that features the DVSI switching states with null zero-sequence voltage components (Group II of DVSI vectors, Set II). Waveforms for two operating conditions are presented for $\Phi_i = 0$, the first with an output voltage reference of 100V in Fig. 2.18, and a second with 199V in Fig. 2.19. These

scenarios correspond to an approximated output power of 300W in Fig. 2.18 and 1200W in Fig. 2.19.

Note that by setting $\Phi_i = 0$, the grid current is not in phase with the IMC input voltage vector, this is clear from both Fig. 2.18(a),(d) and Fig. 2.19(a),(d). This is more accentuated when the output power is lower and happens due to the input filter capacitive characteristic at 50Hz, which must be taken into consideration when adjusting the operating power factor.

It is possible to observe that the dc-link peak current is similar for both CSR modulation strategies, while its average value is increased in the reduced dc-link voltage strategy. This was expected since the output power should be the same for both modulation methods while the average dc-link voltage has distinct values.

Taking a close look to Fig. 2.18(a) and Fig. 2.19(a), it is also noticeable that for the reduced dc-link voltage strategy the IMC input voltages present some distortion with increased output power. This results in additional distortion to the input currents in the transition between input voltage zones and current sectors. The input and output currents THDs for both modulation strategies are presented in Fig. 2.20 in their operating range. The reduced dc-link voltage strategy allows a slight improvement on the output currents while significantly deteriorating the input currents. Still, on both SVM strategies, the input currents THDs are kept below 3.5%.

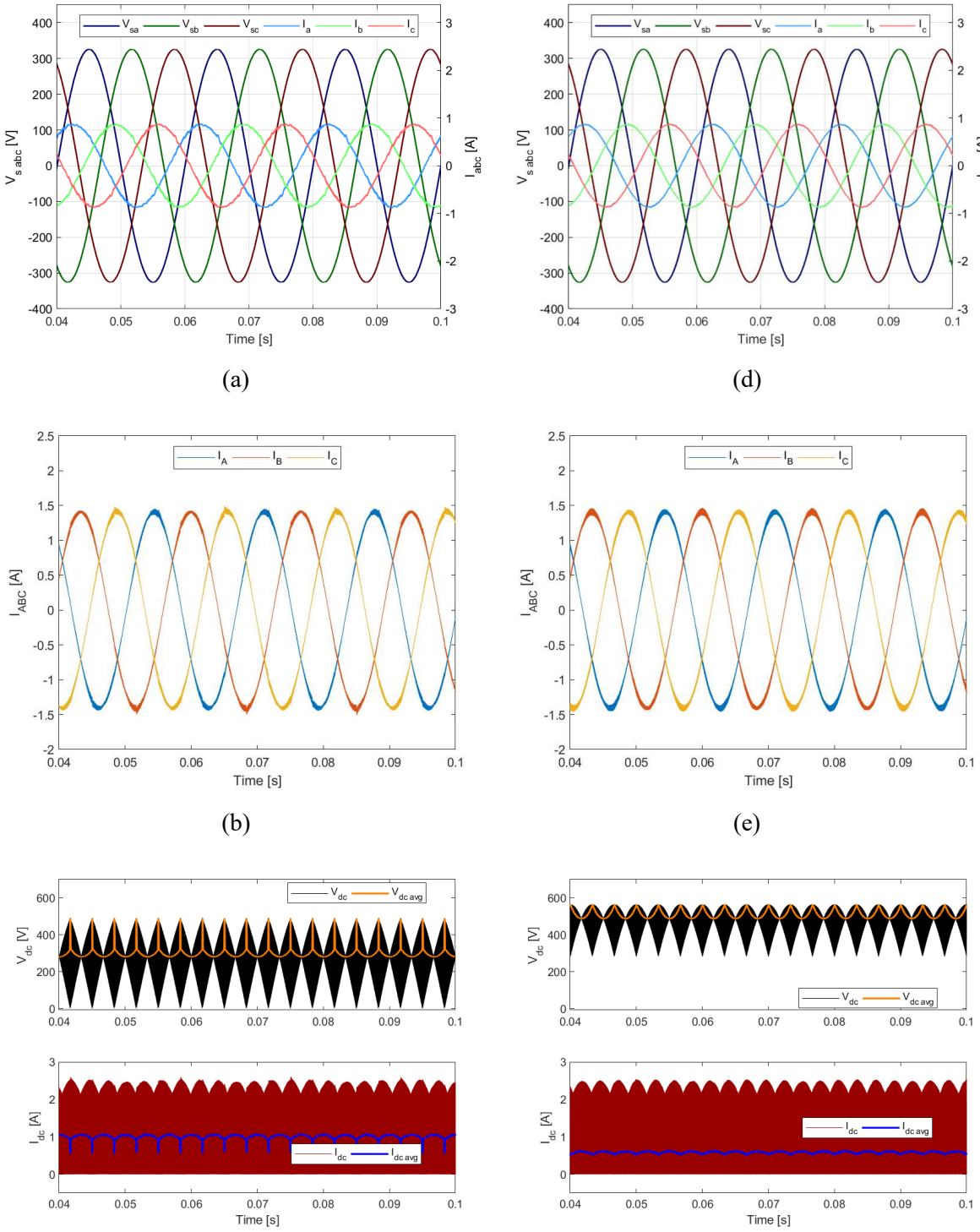


Fig. 2.18. IMC simulation results for two CSR modulation techniques for 100V of output phase voltage. Reduced dc-link voltage strategy: (a) input currents and voltages, (b) output currents, (c) dc-link voltage and current. Maximum dc-link voltage strategy: (d) input currents and voltages, (e) output currents, (f) dc-link voltage and current.

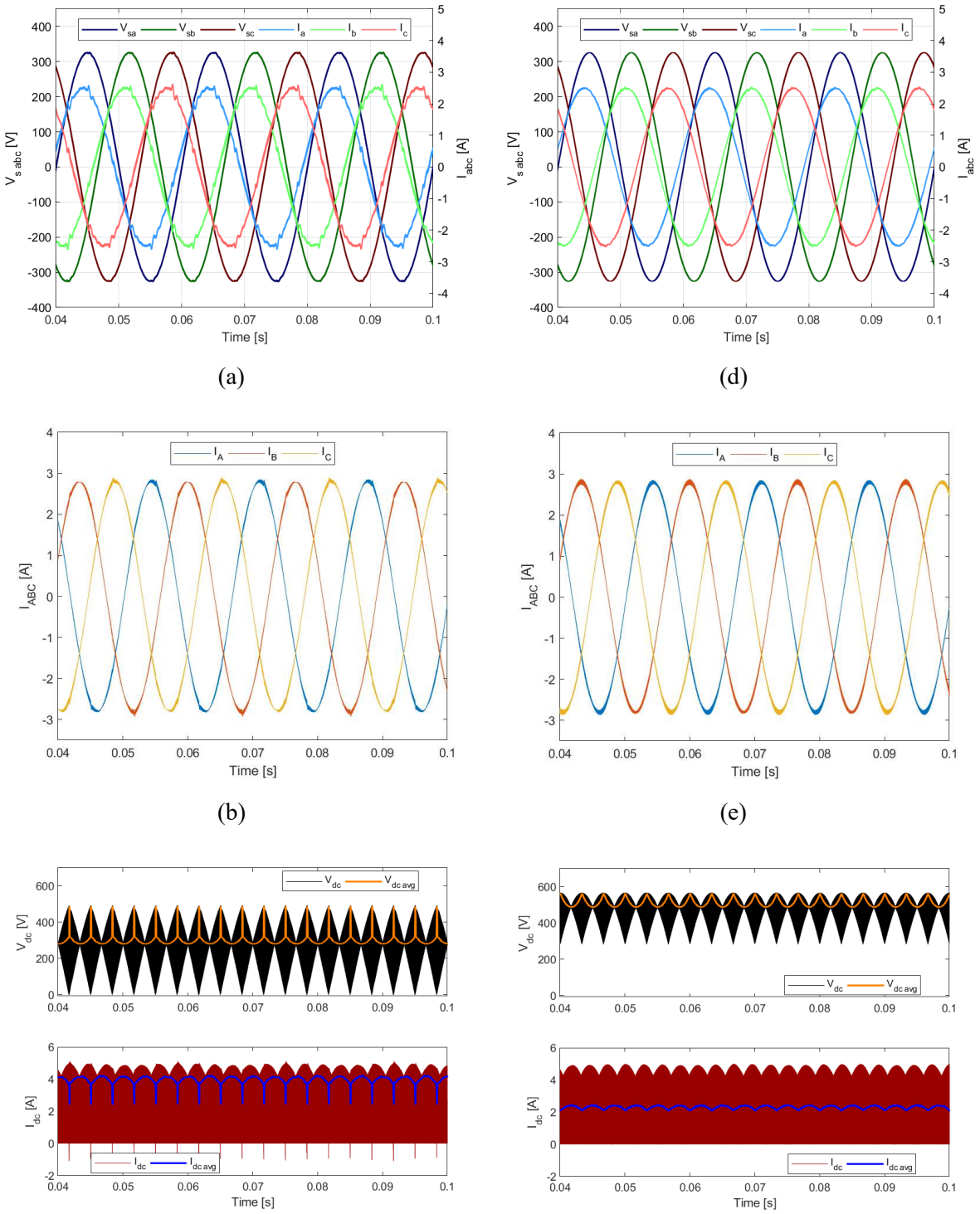
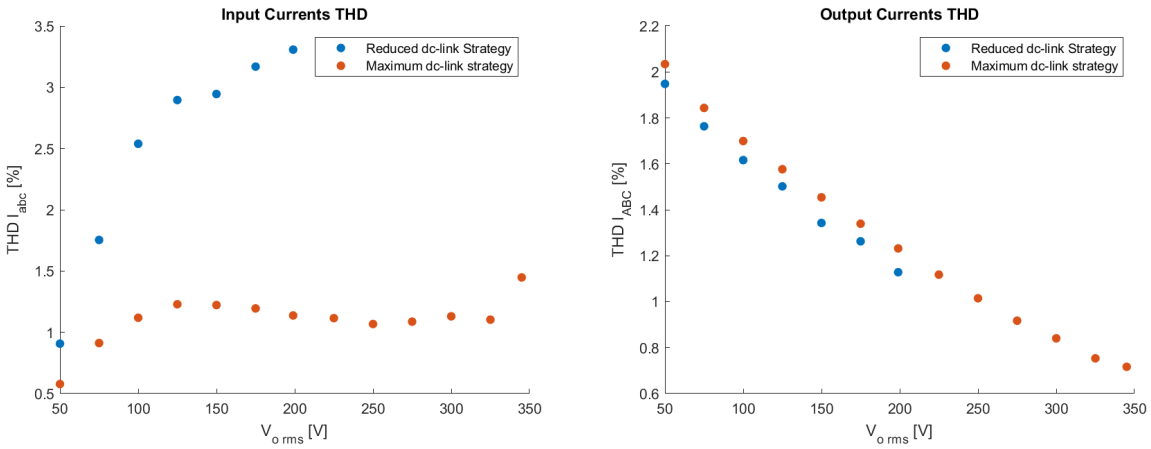


Fig. 2.19. IMC simulation results for two CSR modulation techniques for 199V of output phase voltage. Reduced dc-link voltage strategy: (a) input currents and voltages, (b) output currents, (c) dc-link voltage and current. Maximum dc-link voltage strategy: (d) input currents and voltages, (e) output currents, (f) dc-link voltage and current.



(a) (b)

Fig. 2.20. IMC with DVSI current THDs for reduced dc-link voltage strategy and maximum dc-link voltage strategy. (a) Input currents THDs. (b) Output currents THDs.

2.5.2 – DVSI Group I vectors vs DVSI Group II vectors

This subsection is focused on the comparison of the two DVSI modulation strategies presented in section 2.3. To allow comparison for the full output voltage range, the selected input stage modulation technique is the maximum dc-link voltage strategy, meaning that the maximum theoretical output phase voltage under linear modulation conditions is 345V (setting $\Phi_i=0$) when connected to a grid with the characteristics given in Table 2.8.

The two output stage modulation techniques differ on the considered switching states. The modulation strategy using DVSI Group I vectors (switching states 1 to 20) was introduced in [88] with the purpose of minimizing the CMV supplied to variable speed drives. On the other hand, the modulation strategy that uses DVSI Group II vectors (switching states 21 to 38) allows the IMC to eliminate the instantaneous zero-sequence voltage component supplied to the load. As previously discussed, even though the Group I vectors have higher amplitude in the $\alpha\beta$ plane, due to requiring zero sequence voltage compensation the converter gain under linear modulation operation is identical for both strategies.

Simulation results of two scenarios for both modulation strategies supplying a RL OEW load are presented, with the simulation parameters provided in Table 2.8, one with null input current-to-voltage displacement angle ($v_{out\,rms}$=298 V, Φ_i=0 rad) in Fig. 2.21 and a second scenario with inductive characteristic ($v_{out\,rms}$=298 V, Φ_i=π/6 rad) in Fig. 2.22.

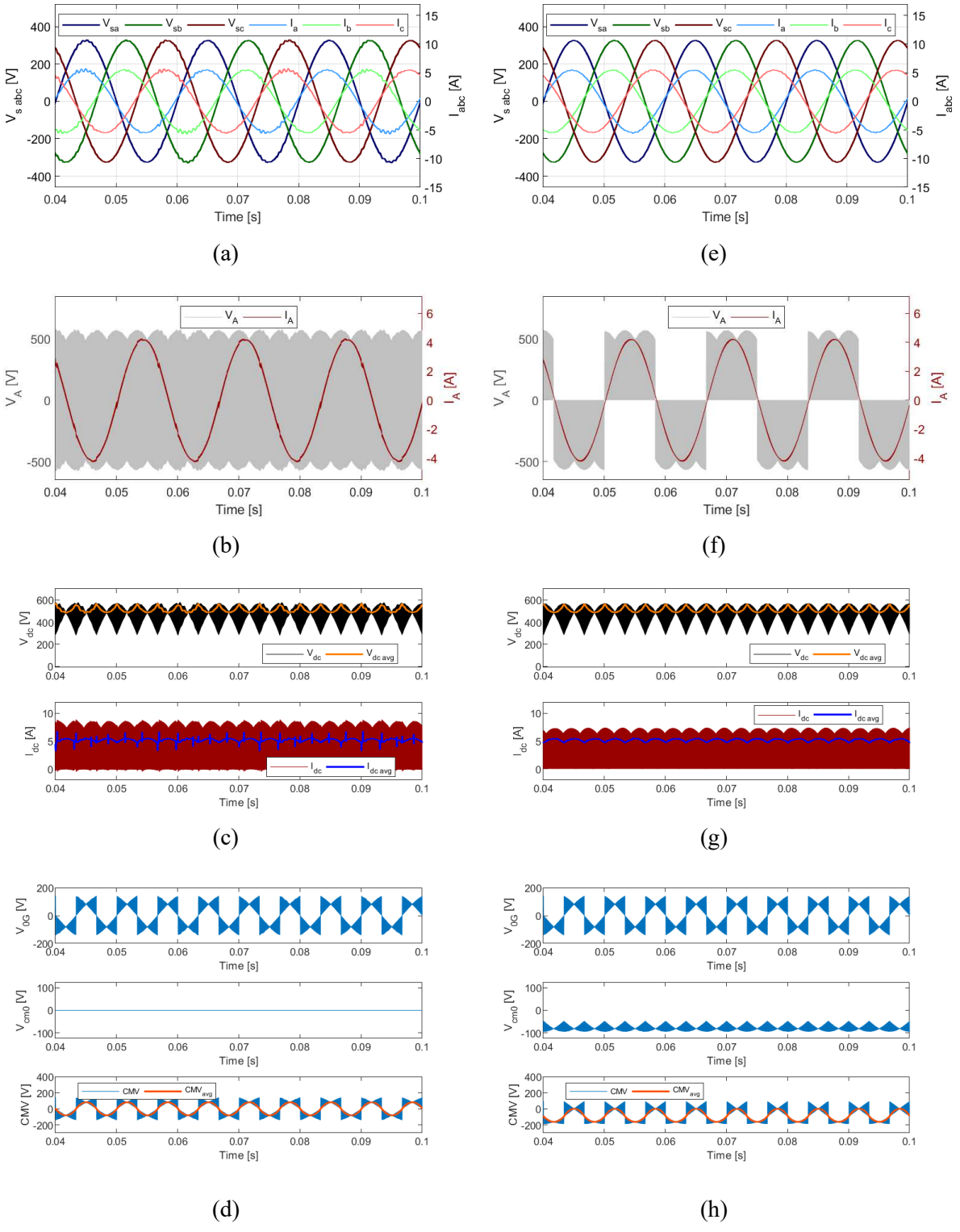


Fig. 2.21. IMC simulation results for two DVSI modulation techniques presented in section 2.2 for 298V of output phase voltage and $\Phi_i=0$. DVSI Group I vectors strategy: (a) input currents and voltages, (b) output current and voltage of phase A, (c) dc-link voltage and current, (d) CMV and its components. DVSI Group II vectors strategy: (e) input currents and voltages, (f) output current and voltage of phase A, (g) dc-link voltage and current, (h) CMV and its components.

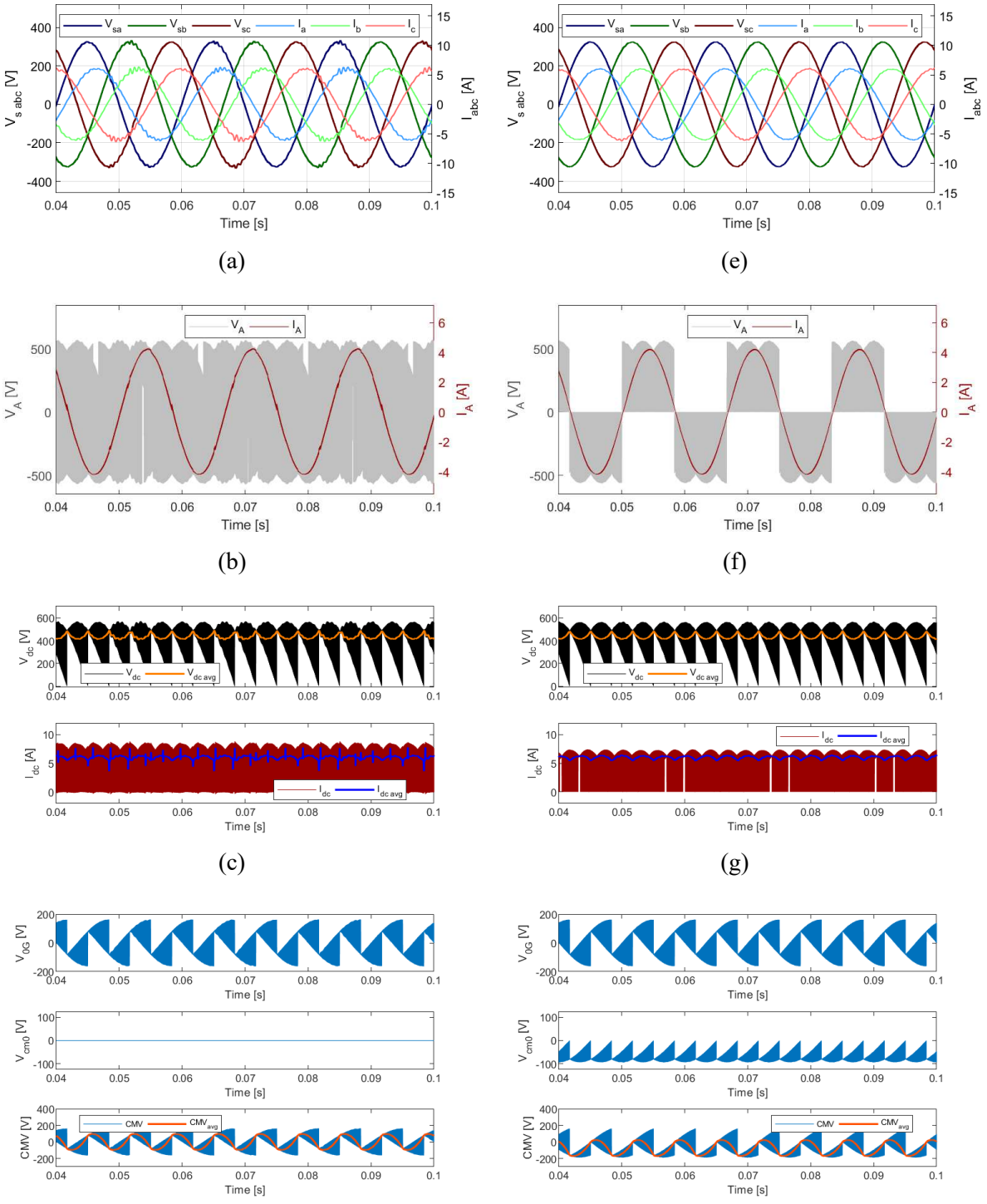


Fig. 2.22. IMC simulation results for two DVSI modulation techniques presented in section 2.2 for 298V of output phase voltage and $\Phi_i=\pi/6$. DVSI Group I vectors strategy: (a) input currents and voltages, (b) output current and voltage of phase A, (c) dc-link voltage and current, (d) CMV and its components. DVSI Group II vectors strategy: (e) input currents and voltages, (f) output current and voltage of phase A, (g) dc-link voltage and current, (h) CMV and its components.

It is seen in Fig. 2.21.(b) and Fig. 2.22.(b) that the modulation strategy with DVSI Group I vectors results in either the positive or negative dc-link voltage applied to each phase of the load (two levels). On the other hand, the Group II vectors allow for positive, negative or zero voltage (3 levels) as shown in Fig. 2.21.(f) and Fig. 2.22.(f). This results in output currents with higher harmonic content for the strategy that makes use of the Group I vectors.

On the CMV supplied to the OEW RL load, because the input stage modulation is the same for both strategies, its contribution (V_{0G}) is identical in both cases. The difference appears in the contribution of the output stage, V_{cm0}, which is null with DVSI Group I vectors, while pulsed depending on the soft dc-link voltage for DVSI Group II vectors. Note that the results presented in both Fig. 2.21(h) and Fig. 2.22(h) use the set II of DVSI Group II vectors, which according to (2.8), Table 2.5 and Table 2.6 results in negative V_{cm0}. The resulting global CMV is the sum of these two components.

To quantify the impact of the modulation methods on the CMV, both its instantaneous and average values during one switching period (CMV_{avg}) are plotted in subfigures (d) and (h) of both Fig. 2.21 and Fig. 2.22. It is possible to observe that both the instantaneous CMV peak value and its average value are significantly reduced with the DVSI Group I vectors modulation strategy.

The input quantities and output currents THDs for a significant operating range of reference output voltages and for three different characteristic scenarios of input current-to-voltage displacement angles are presented in Fig. 2.23.

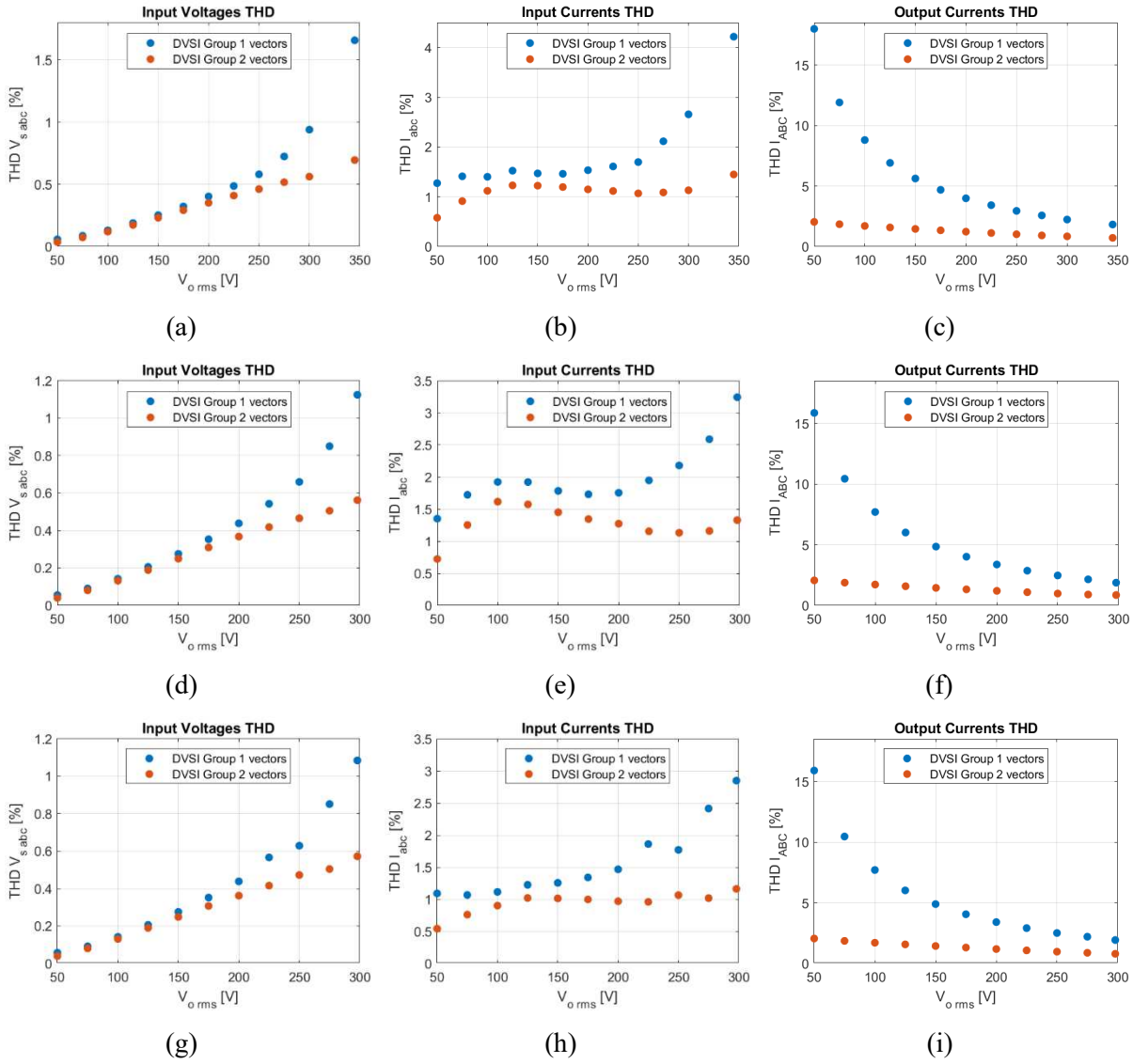


Fig. 2.23. IMC with DVSI THDs for output stage modulation with Group i vectors and Group II vectors: (a)-(c) Φ_i=0; (d)-(f) Φ_i=-π/6; (g)-(i) Φ_i=π/6.

Even though the THD of the input quantities are maintained low in both modulation techniques, the DVSI modulation strategy that uses Group I vectors presents approximately two times higher THD on both input quantities in higher output power ranges, subfigures (a),(b),(d),(e),(g) and (h) of Fig. 2.23. For lower power ranges, the input quantities THD are similar on both modulation strategies but the output currents THDs are significantly higher for group I vectors modulation strategy, subfigures (c), (f) and (i) of Fig. 2.23.

2.5.3 – Analysis of the Input Stage modulation techniques in the IMC Losses

In section 2.2, it was pointed out that the reduced dc-link voltage strategy allows the output stage to switch with lower dc-link voltages. This results in smaller DVSI switching losses but leads to higher active vector duty - cycles on the DVSI side, which increase the time where current is flowing through the CSR switches and consequently increase the CSR conduction losses. For this reason, it is interesting to analyse the losses of both IMC stages to quantify the effect of both modulation strategies to the global converter losses.

To perform the loss analysis, an average model of the converter was developed where the input filter is disregarded while assuming that every IMC semiconductor is identical and operating under the same thermal conditions, constant and equal junction temperature, leading to identical loss characteristics. The switching devices considered were GaN High Electron Mobility Transistors (HEMT).

On the output stage, at any given instant, each load current flows through two semiconductors, thus the conduction losses of this stage are given by (2.49), where R_{ds} is the drain to source resistance of the semiconductor.

$$P_{cond}^{DVSI} = 6R_{ds}i_{o\,rms}^{2} \tag{2.49}$$

The switching losses of the output stage depend on both the output current and dc-link voltage at the commutation instant. The adopted switching pattern, shown in Fig. 2.17 and detailed in Fig. 2.15(b), has 6 commutation events (M1 to M6) per switching period. In each of these events, two semiconductors switch ON and two switch OFF.

Remembering that the switching frequency is assumed to be high enough so that both the CSR input voltages and DVSI output currents remain nearly constant during the switching period, let us consider the situation where the output voltage reference vector is placed in output sector I, while using Group II and Set II DVSI switching states. Thus, through Table 2.6, the used vectors are 35 (vector *o*), 25 (vector κ) and 26 (vector λ). Considering the linearized switching loss energy model presented in [95] and adopting the conventional IMC losses calculation in [96], the switching energy lost due to the turn ON and turn OFF of a given semiconductor under specific instantaneous operating conditions (E_{sw} at voltage v and current i) is considered proportional to the manufacturer catalogue loss data at reference operating condition (E_{sw}^{R} at voltage V^R and current I^R), as given by (2.50).

$$E_{sw} = E_{sw}^{R} \frac{v\, i}{V^{R} I^{R}} \tag{2.50}$$

Take for example M1, the transition of switching state 35 to 25. From Table 2.5 it is seen that S_{A2u} and S_{B2d} turn OFF and S_{A2d} and S_{B2u} turn ON while the dc-link voltage is given by the CSR vector ρ. The energy lost due to the six switching events is given by (2.51)

$$\begin{cases} E_{sw}^{M1} = \dfrac{E_{sw}^{R}}{V^{R} I^{R}} v_{dc}^{\rho} \left(\left| i_A \right| + \left| i_B \right| \right) \\ E_{sw}^{M2} = \dfrac{E_{sw}^{R}}{V^{R} I^{R}} v_{dc}^{\rho} \left(\left| i_B \right| + \left| i_C \right| \right) \\ E_{sw}^{M3} = \dfrac{E_{sw}^{R}}{V^{R} I^{R}} v_{dc}^{\rho} \left(\left| i_A \right| + \left| i_C \right| \right) \\ E_{sw}^{M4} = \dfrac{E_{sw}^{R}}{V^{R} I^{R}} v_{dc}^{\sigma} \left(\left| i_A \right| + \left| i_C \right| \right) \\ E_{sw}^{M5} = \dfrac{E_{sw}^{R}}{V^{R} I^{R}} v_{dc}^{\sigma} \left(\left| i_B \right| + \left| i_C \right| \right) \\ E_{sw}^{M6} = \dfrac{E_{sw}^{R}}{V^{R} I^{R}} v_{dc}^{\sigma} \left(\left| i_A \right| + \left| i_B \right| \right) \end{cases} \tag{2.51}$$

The switching energy lost during a full switching period is the sum of switching energies of all commutation events M1-M6.

$$E_{sw}^{T_{sw}} = \sum_{k=1}^{6} E_{sw}^{Mk} = 2 \frac{E_{sw}^{R}}{V^{R} I^{R}} \left(v_{dc}^{a} + v_{dc}^{b} \right) \left(\left| i_A \right| + \left| i_B \right| + \left| i_C \right| \right) \tag{2.52}$$

The DVSI switching power losses are then obtained by (2.53).

$$P_{sw} = f_{sw} E_{sw}^{T_{sw}} = 2 f_{sw} \frac{E_{sw}^{R}}{V^{R} I^{R}} \left(v_{dc}^{a} + v_{dc}^{b} \right) \left(\left| i_A \right| + \left| i_B \right| + \left| i_C \right| \right) \tag{2.53}$$

Moving to the input stage, recalling that only Group II DVSI vectors are used, the commutation occurs with zero dc-link current, thus the switching losses can be disregarded. For the conduction losses, one bidirectional switch is connected to the upper dc-link bus while the other switch is connected to the bottom dc-link bus. This means that at any given instant, there are 4 semiconductors in series with the dc-link current (two per bidirectional switch). Thus, the conduction losses of the input stage can be computed by (2.54).

$$P_{cond}^{CSR} = 4 R_{ds} I_{dc\,rms}^{2} \tag{2.54}$$

The root mean square value of the dc-link current is obtained through (2.55), where δ_κ and δ_λ are the duty-cycles of the output stage active vectors, while i_κ and i_λ are the corresponding dc-link currents of those same switching states.

$$I_{dc\,rms} = \sqrt{\delta_\kappa i_\kappa^2 + \delta_\lambda i_\lambda^2} \tag{2.55}$$

The loss analysis was performed for an IMC with DVSI composed of GaN HEMTs from the manufacturer GaN Systems with reference GS66508T, considering a fixed junction temperature of 100ºC. The HEMT parameters are given in Table 2.9. The analysis is performed for a varying output reference voltage from 25V to 199V. The grid characteristics are 400V phase to phase at 50Hz, with the SVM switching frequency set to 50kHz, output frequency of 50Hz and null input displacement angle. The load resistance was adjusted for a high load scenario (R_{load} set to 25Ω) and a lower load scenario (R_{load} set to 100Ω).

Table 2.9: GaN HEMT GS66508T parameters at 100ºC.

R_{ds}	85[mΩ]
E_{sw}^R	66[μJ]
V^R	400[V]
I^R	15[A]

The average model simulation results are presented in Fig. 2.24, for a low load case scenario in (a)-(d), and for a higher load scenario in (e)-(h) parts. Note that the output stage conduction losses are identical for both modulation methods as expected from (2.49).

On the switching losses, by observation of Fig. 2.24(b) and Fig. 2.24(f) it is concluded that the reduced dc-link voltage strategy present lower switching losses than the modulation method with maximum dc-link voltage, as expected. Note that the switching losses evolve linearly with the increase of output voltage. This happens because the RL load current increases linearly with the output voltage.

On the input stage side, it is observed in Fig. 2.24(c) and Fig. 2.24(g) that the CSR conduction losses grow with the square of the output voltage, which is a consequence of (2.54) and (2.55) due to the RL load characteristic. Note that the reduced dc-link voltage presents higher CSR conduction losses.

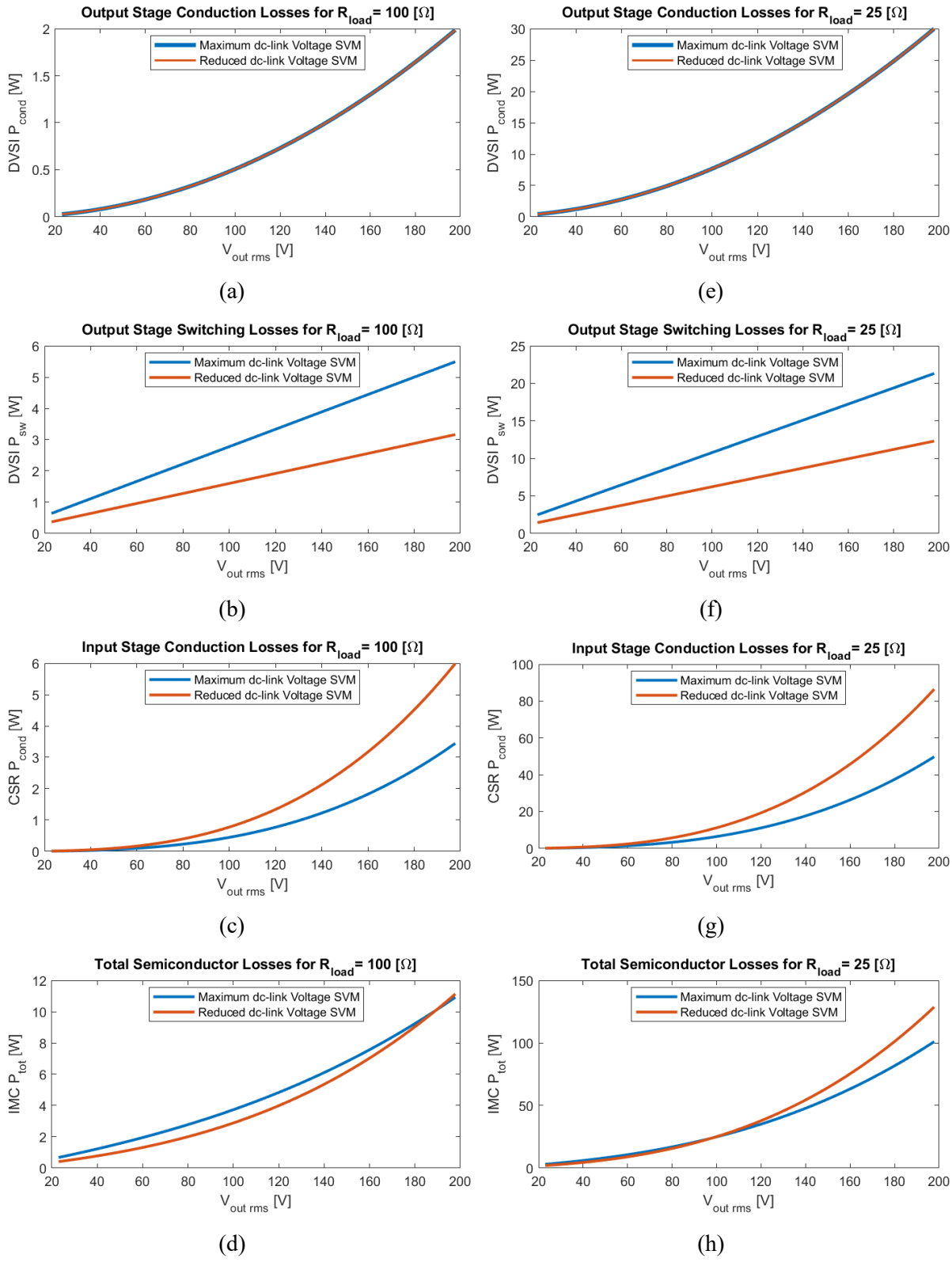


Fig. 2.24. IMC loss analysis for both CSR modulation strategies in a low load scenario (a)-(d), and in a high load scenario (e)-(h).

Since the DVSI switching losses and the CSR conduction losses exhibit opposite behaviours for both CSR modulation methods, and by being greatly dependent on the output power of the converter, it is not possible to guarantee that any of the modulation methods will outperform the other for a given operating range in terms of minimizing the semiconductor losses without knowing the exact load characteristics, especially when dealing with electric machines that have different mechanical loads and speed ranges. This is observable in Fig. 2.24(d) and Fig. 2.24(h) where for the lower load scenario the reduced dc-link voltage strategy presents lower losses than the maximum dc-link strategy until an output voltage around 180V and in the higher load scenario this only happens up to approximately 100V.

Still, this study shows that for lower output power levels the reduced dc-link voltage strategy is more likely to decrease the IMC losses and that for higher power levels the same happens with the maximum dc-link voltage modulation method. Note that this analysis only makes sense for output voltages bellow 199V. For higher output voltages only the maximum dc-link voltage strategy can supply the load.

CHAPTER 3

SYNCHRONOUS RELUCTANCE MACHINE

The SynRM concept is well known, but only recently this type of electrical machine has emerged as a viable alternative to well established machines. When directly fed from the grid, this machine has no self-starting capability and possesses an extremely low power factor. On the other hand, when supplied by an electronic power converter under closed loop control, such problems can be easily overcome while unlocking attractive characteristics such as high efficiency and robustness at low cost [49]. The reason for the recent boom of interest in the SynRMs is due to the increasing number of variable speed drives and its applications where high efficiency, robustness and low cost are key requirements [97].

The SynRM working principle is based on the reluctance torque originated by the stator windings "seeing" a varying magnetic reluctance in respect to the rotor position. This is achieved by purposely introducing flux barriers in the rotor creating an anisotropic rotor structure, visible in Fig. 3.1. This results in both, a higher and a lower magnetic reluctance path for the magnetic flux produced by the stator currents to flow. If the lower magnetic reluctance path (the *d* axis) is not aligned with the field created by the stator, a reluctance torque will appear to force the alignment. Thus, the reluctance torque is a consequence of the flux trying to flow through the lowest magnetic reluctance path. If the stator field is kept rotating at a synchronous speed, ω_e, the reluctance torque originated by the rotor anisotropy will make it follow the stator field.

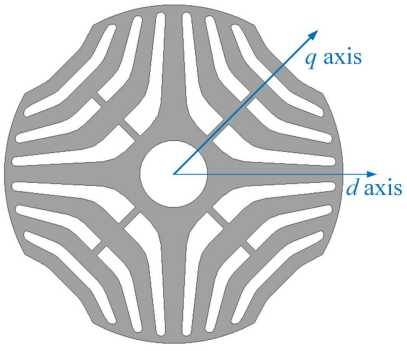


Fig. 3.1. Anisotropic rotor structure of a 4 pole SynRM.

Thus, the SynRM does not require permanent magnets nor currents flowing through its rotor to produce torque, resulting in a cheaper rotor than both PMSMs and induction machines (IMs) while featuring identical stators. At the same time, due to the absence of rotor currents, the SynRM rotor losses are lower than in IMs, allowing SynRM cold rotors to achieve better efficiencies and a size reduction when compared with an equivalently rated IM [45][47].

Although not being able to achieve the efficiency and power density levels of PMSMs, the SynRM is way less sensitive to its operating thermal and electrical conditions given that there is no risk of permanent magnets demagnetization [46], while offering extremely high overload capability [98] and unlimited speed-range under field-weakening operation (the speed limit of SynRMs only depends on the drive mechanical parameters) [46].

3.1 – SynRM Mathematical Model

The equation that models the mechanical dynamics of an electrical machine shaft is given by (3.1), where ω_m is the rotor angular speed, T_e is the electromagnetic torque, T_{load} is the load torque, J is the shaft constant of inertia and k_D is the viscous friction coefficient. Note that the stator field synchronous speed relates to the rotor mechanical angular speed as $\omega_e = p\,\omega_m$, where p is the SynRM number of pole pairs.

$$\frac{d\omega_m}{dt} = \frac{1}{J}\left(T_e - T_{load} - k_D\omega_m\right) \tag{3.1}$$

Regarding the dynamics of electrical quantities, due to the rotor anisotropy the stator winding self and mutual inductances are functions of the rotor mechanical position, θ_m. To avoid dealing with rotor position varying parameters, SynRM is commonly modelled in a *dqz* reference frame synchronized with the rotor angular electric position, θ_e ($\theta_e = p\,\theta_m$).

In a power invariant rotor synchronized *dqz* reference frame, the electrical dynamics of an OEW SynRM can be modelled by (3.2), where v_d, v_q, and v_z are the terminal voltages along the *d*, *q* and *z* axis; i_d, i_q, and i_z are the stator currents along the *d*, *q* and *z* axis; ψ_d, ψ_q, and ψ_z are the stator flux linkages along the *d*, *q* and *z* axis; and R_s is the winding resistance.

$$\begin{cases} v_d = R_s i_d + \dfrac{d\psi_d}{dt} - \omega_e \psi_q \\ v_q = R_s i_q + \dfrac{d\psi_q}{dt} + \omega_e \psi_d \\ v_z = R_s i_z + \dfrac{d\psi_z}{dt} \end{cases} \tag{3.2}$$

The electromagnetic torque developed by the SynRM is a function of both the direct and quadrature axis fluxes and currents, as given by (3.3). Note that neither the zero-sequence axis flux nor current contribute to the developed torque, on the other hand they generate copper losses and contribute to the core saturation. Thus, it is beneficial to keep ZSC as close to zero as possible. For this reason, the analysis presented in this chapter for the operation trajectories and parameter identification considers that the selected controllers and modulation methods can keep ZSC null, allowing the use of literature works that focus only on *dq axis*.

$$T_e = p\left(\psi_d i_q - \psi_q i_d\right) \tag{3.3}$$

Since there are no ideal magnetic materials, the relation between the magnetic flux and the currents is never completely linear. Particularly, the SynRMs very high overload capability may result in a highly saturated magnetic characteristic [98]. Moreover, the flux linkage on either of the *dqz* frame axis does not depend exclusively on its self-axis current, they are affected by the other axis currents in a phenomenon known as cross-saturation [97].

Thus, the inclusion of magnetic saturation effects in the SynRM mathematical model is mandatory to obtain an accurate prediction of its operation [99]. On the other hand, the results presented in [98] and [100], namely the characteristics of torque versus current magnitude and the optimal current trajectory, composed of current pairs (i_d, i_q) resulting in the maximum torque per ampere (MTPA) trajectory, suggest that up to around 250% of the rated SynRM current, there is practically no difference in these characteristics whether the cross-saturation phenomenon is taken into consideration or not. That being said, for studying SynRM drives that don't operate in heavy overload scenarios, neglecting the cross-saturation phenomenon should still reproduce adequate results while avoiding complex self-commissioning methods that require power electronic converters and digital signal processing units with already tunned controllers as the ones discussed in [101].

There is extensive literature in modelling SynRMs considering magnetic saturation. Some authors propose the usage of flux linkages as state variables as presented in works [100][102],

while others chose to use currents as state variables [97][103][104]. In both cases, the non-linear magnetic characteristics are commonly stored in look up tables (LUTs) to minimize the computational burden. In this thesis, the approach with currents as state variables is utilized as it is better suited for FOC by allowing direct control over the currents.

Considering that the ZSC is kept approximately null and by disregarding cross-saturation, the flux linkages in the *dqz* frame can be rewritten by (3.4), where the inductance L_d is a function of i_d and the inductance L_q is a function of i_q. The zero-sequence flux linkage is given by the product of the ZSC, i_z, by the leakage inductance, L_{lk}, that is considered constant. Note that although the objective is to eliminate the ZSC to reduce copper losses and minimize the impact on the magnetic saturation of the direct and quadrature axis, its dynamics must be included in the model.

$$\begin{cases} \psi_d = L_d\left(i_d\right) i_d \\ \psi_q = L_q\left(i_q\right) i_q \\ \psi_z = L_{lk} i_z \end{cases} \tag{3.4}$$

At this point, it is important to define the concepts of apparent and incremental inductances, illustrated in Fig. 3.2. The apparent inductance is the absolute inductance of the machine, defined as the slope of a straight line from the origin to the actual operating point, as given by (3.5) for a general '*x*' axis, maintaining accordance with (3.4). On the other hand, the incremental inductance is given by the partial derivative of the flux in respect to the current, given by (3.6) for a general '*x*' axis. These concepts are a consequence of static and dynamic permeabilities of ferromagnetic materials [105]. Since the state variables of our model are the currents, the definition of incremental inductance is useful to compute the derivative of the flux with respect to time, as given by (3.7).

$$L_x^{app} = L_x = \frac{\psi_x}{i_x} \tag{3.5}$$

$$L_x^{inc} = \frac{\partial \psi_x}{\partial i_x} \tag{3.6}$$

$$\frac{d\psi_x}{dt} = \frac{\partial \psi_x}{\partial i_x}\frac{di_x}{dt} = L_x^{inc}\frac{di_x}{dt} \tag{3.7}$$

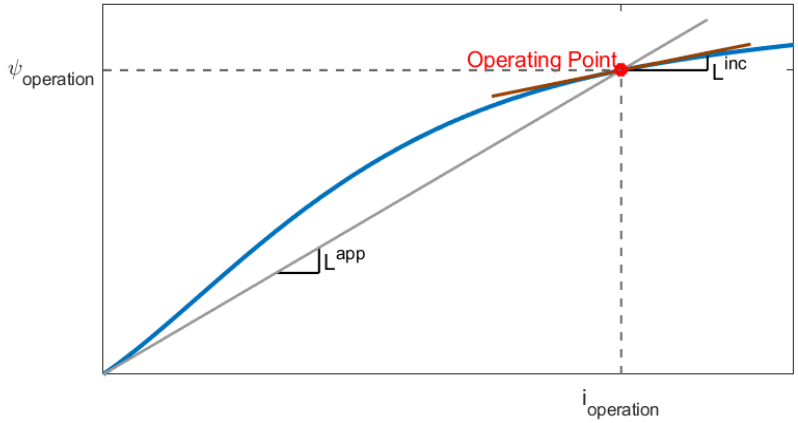


Fig. 3.2. Illustration of apparent and incremental inductances concepts in non-linear ferromagnetic materials.

The electrical dynamics of a SynRM considering non-linear magnetic characteristic while disregarding cross-saturation is given by (3.8). The electromagnetic torque is given by (3.9).

$$\begin{cases} v_d = R_s i_d + L_d^{inc}\left(i_d\right)\dfrac{di_d}{dt} - \omega_e L_q\left(i_q\right) i_q \\ v_q = R_s i_q + L_q^{inc}\left(i_q\right)\dfrac{di_q}{dt} + \omega_e L_d\left(i_d\right) i_d \\ v_z = R_s i_z + L_{lk}\dfrac{di_z}{dt} \end{cases} \tag{3.8}$$

$$T_e = p\left(L_d\left(i_d\right) - L_q\left(i_q\right)\right) i_d i_q \tag{3.9}$$

Observing (3.9), it can be concluded that the electromagnetic torque developed by the SynRM depends on the product of both direct and quadrature axis currents by the difference between the non-linear direct and quadrature inductances. This means that there are countless combinations of i_d and i_q that produce a desired torque. This is extensively documented in [45] and on one hand adds complexity to the control of SynRMs, but at the same time allows the machine to develop the desired output torque while providing extra degrees of freedom to enhance certain operating characteristics.

Thus, it is possible to produce the same torque with different values of current magnitude, which means that there is one combination of i_d and i_q that leads to minimum copper losses while still producing the required torque.

3.2 – SynRM Operating Trajectories

The trajectory composed by the combinations of i_d and i_q that minimize the stator current magnitude for the output torque range of the electric machine is designated as MTPA trajectory. Most works found in literature disregard the fact that SynRM copper losses bellow base speed are much bigger than core losses, MTPA being the most popular operating trajectory for SynRMs, operating bellow the machine base speed due to its high efficiency. This operating region where the SynRM speed is bellow base speed and constant rated torque is achievable is usually known as constant torque zone and results in the first operating region of SynRMs.

At this point, it is convenient to introduce the definition of the current angle, α_i, given by (3.10) and represented in the vector diagram of Fig. 3.3.

$$\alpha_i = \tan^{-1}\left(\frac{i_q}{i_d}\right) \tag{3.10}$$

If the magnetic saturation is disregarded, from (3.9) it is clear that the MTPA trajectory is obtained by using $i_d = i_q$, which would result in a current angle of 45º. When saturation is considered, this is not true anymore due to the dependency of L_d and L_q on the machine currents. The magnetic saturation of the d axis inductance must be compensated by decreasing i_d and increasing i_q, resulting in a current angle bigger than 45º [45].

Under steady state operation, neglecting stator resistance, the SynRM voltage equations may be approximated by (3.11). Note that if the speed is high enough it will not be possible to operate in the MTPA trajectory because the required supply voltage will exceed the rated value. This is what happens above SynRM base speed, where field-weakening strategies must be adopted to allow operation above the base speed range.

$$\begin{cases} v_d \approx -\omega_e L_q\left(i_q\right) i_q \\ v_q \approx \omega_e L_d\left(i_d\right) i_d \\ v_z \approx 0 \end{cases} \tag{3.11}$$

It is now important to introduce the definition of load angle, δ, given by (3.12) and corresponding to the angular displacement between the d axis and the stator flux vector as shown in Fig. 3.3. The load angle is considered positive when the SynRM is developing positive output torque (Motor operation) and negative when the developed output torque is negative (Generator operation).

$$\delta = \tan^{-1}\left(\frac{L_q i_q}{L_d i_d}\right) \tag{3.12}$$

Under field weakening operation, both the SynRM supply voltages and currents are at their rated values. To increase the SynRM speed, the load angle should be increased (in magnitude, since its signal depends on the operation mode). This situation is usually known as the second operation region of SynRM or the constant power region, where the maximum developed torque is decreased inversely to the increase of speed to maintain the rated power. The load angle may continue to be increased until it reaches its stability limit of 45º. From that operation point, it is not possible to maintain the SynRM current at its nominal value, and the developed torque starts decreasing quadratically with the increase of speed. This situation where the load angle is fixed at its stability limit is known as the third operating region of SynRMs.

It is now important to understand how the load angle is set. Note that the increase in the current angle, α_i, while the stator current magnitude remains constant and ZSC are kept null, results in the increase of i_q and the decrease of i_d. Analysing (3.12), considering a positive electromagnetic torque, one may observe that the increase in the relation i_q / i_d leads to the increase of the load angle, δ. Thus, the increase in the load angle may be accomplished with the increase of the current angle. The stability limit is achieved when the relation i_q / i_d is equal to the saliency ratio, ξ, as shown in (3.13). Setting the tangent of the current angle equal to the saliency ratio is known as the Maximum Torque per Volt (MTPV) trajectory. This is the most popular trajectory to operate the SynRM in the third operating region.

$$MTPV \rightarrow \ \delta = 45^{\circ} \Rightarrow \tan(\delta) = 1 \Rightarrow \frac{L_q i_q}{L_d i_d} = 1 \Rightarrow \frac{i_q}{i_d} = \frac{L_d}{L_q} = \xi \tag{3.13}$$

Lastly, a mention is given to another popular trajectory in SynRM operation, that is the Maximum Torque per kilo Volt-Ampere (MTPkVA) or Maximum Power Factor (MPF) trajectory. This trajectory maximizes the SynRM power factor for a given stator current and is obtained by forcing the relation i_q / i_d to be equal to the square root of the saliency ratio, as given by (3.14).

$$MPF \rightarrow \ \alpha_i = \tan^{-1}\left(\sqrt{\frac{L_d}{L_q}}\right) \Rightarrow \frac{i_q}{i_d} = \sqrt{\frac{L_d}{L_q}} = \sqrt{\xi} \tag{3.14}$$

These are just some of the most popular SynRM operating trajectories. There are others such as the Constant d-axis current, Maximum Efficiency which diverges from the MTPA as the iron losses are considered, Maximum Rate of change of Torque, etc [45].

One of the objectives of this thesis is to propose a new controller that can follow a given operating trajectory. Thus, this thesis does not enter too much into detail in the elaboration of SynRM operation trajectories and will focus on the control of the machine bellow drive base speed following a MTPA trajectory stored in a LUT.

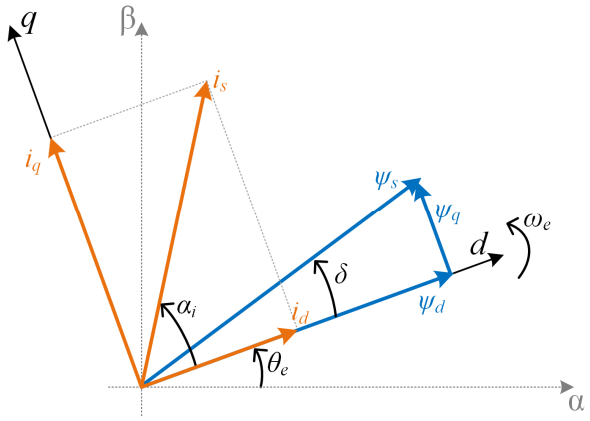


Fig. 3.3. Vector diagram of SynRM quantities in the *dqz* frame.

3.3 – SynRM Parameter Identification

The knowledge of the SynRM non-linear magnetic model is crucial for operation on a desired operating trajectory, having direct impact on the drive efficiency, developed torque quality, currents, and fluxes [101]. There is extensive literature on the identification of SynRM parameters. Some authors propose the extraction of magnetic flux maps through numerical methods such as FEA [106][107], this way it is possible to include some important magnetic effects such as saturation, cross-saturation, and slotting effect. The slotting effect is due to the shape of the stator teeth and is observed by a small variation of the *dq* axis flux in relation to the rotor position, being disregarded when a rotor synchronized *dqz* frame transformation is utilized for modelling the SynRM. This effect has been proven to have little impact in the SynRM modelling and control and is constantly disregarded in most research works [99]. The parameter identification of electric machines through numerical methods has the inconvenience of being applicable only by the motor designer, since other users do not have enough data to build an accurate numerical or finite element model of the machine [108]. This has led researchers to develop self-commissioning procedures for SynRMs. These characterization procedures can be classified as constant speed identification methods and standstill identification methods. The first class requires a dedicated setup with a prime mover, to

guarantee fixed speed operation, with dedicated instrumentation. On the other hand, standstill identification methods are of simpler application due to supplying the SynRM with different signals, recording the machine response and then postprocess the recorded data to obtain the machine characteristics.

In [108], a standstill with free-shaft method is proposed where controlled current is injected in the SynRM *d* and *q* axis, while the supply voltage subtracted by the voltage drop at the winding resistor is integrated to obtain a measurement of the magnetic flux. The drive currents are controlled using a model predictive controller where the inductances are roughly estimated online through a flux observer to reduce torque ripples and vibrations. The SynRM is supplied by a VSI, allowing independent control of *d* and *q* axis currents, allowing the inclusion of cross-saturation effects in the SynRM characterization. The authors of [100] propose a new self-commissioning method that applies positive and constant voltage in one axis of the machine until its current reaches a selected maximum magnitude value. Then it switches the polarity of the voltage until the current reaches the symmetric limit, and the polarity of the voltage is switched again and so on. This is performed for both axes separately to obtain the self-axis saturation characteristics. Then a third part of the procedure is proposed to consider the cross-saturation effects. As explained in section 3.1, the cross-saturation phenomena gains relevance in heavy overload conditions, which is not the focus of this work.

The self-commissioning procedure proposed in this thesis requires position measurement using an encoder, such as in the previous works but just makes use of a single-phase autotransformer to allow regulation of the applied voltage to the SynRM, not requiring the rotor to be blocked. On the other hand, it does not offer the possibility of extracting cross-saturation effects, meaning that it is not indicated for machines that operate under severe overload conditions. The procedure is the following:

i. Using a bench power supply with current limitation, apply low DC-voltage to the phase ‘A’ winding. This will align the SynRM rotor *d* axis with that winding. After aligned, reduce the dc-voltage to zero and then disconnect the power supply without misaligning the rotor.

ii. Connect the single-phase autotransformer as indicated in Fig. 3.4. Start increasing the AC-voltage until i_A reaches a previous stablished limit (in this work this value was selected to be around 150% of the SynRM rated current). Use a scope to store the 4 waveforms indicated in purple on the schematic of Fig. 3.4 (V_{in}, V_{An}, i_A and i_B). Slowly reduce the voltage to zero and disconnect the autotransformer.

iii. Align the SynRM rotor *q* axis with the phase 'A' winding (rotate the rotor by θ_e=90º).

iv. Reconnect the autotransformer as shown in Fig. 3.4 and repeat step ii.

v. Measure the three windings resistance using an ohmmeter and average it.

vi. Post-process the stored data as indicated in flowchart of Fig. 3.5.

This characterization procedure was applied to a 3kW SynRM from ABB, whose catalogue characteristics are given in Table 3.1. The *d* axis waveforms are presented in Fig. 3.6, while the *q* axis waveforms are shown in Fig. 3.7.

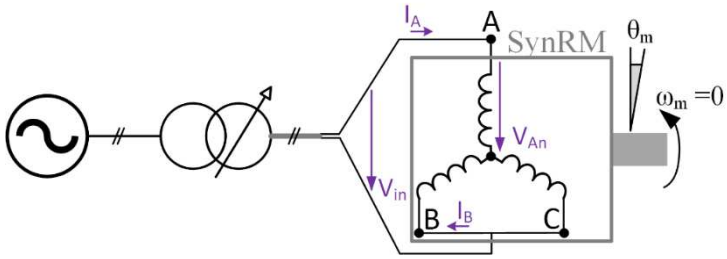


Fig. 3.4. SynRM Characterization schematic.

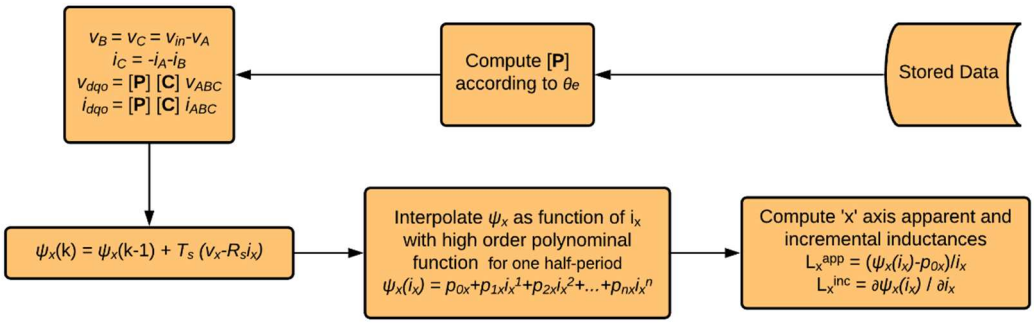


Fig. 3.5. Post-processing flowchart of SynRM characterization procedure for a general '*x*' axis.

Table 3.1: ABB 3kW SynRM catalogue characteristics.

Product Code	3GAL102523
Nominal speed	1500 rpm
Nominal torque	19.1 Nm
Nominal voltage $_{\text{L-L rms}}$	380 V
Nominal current $_{\text{rms}}$	7.1 A
Nominal efficiency	85.5 %
Nominal Power Factor	0.75

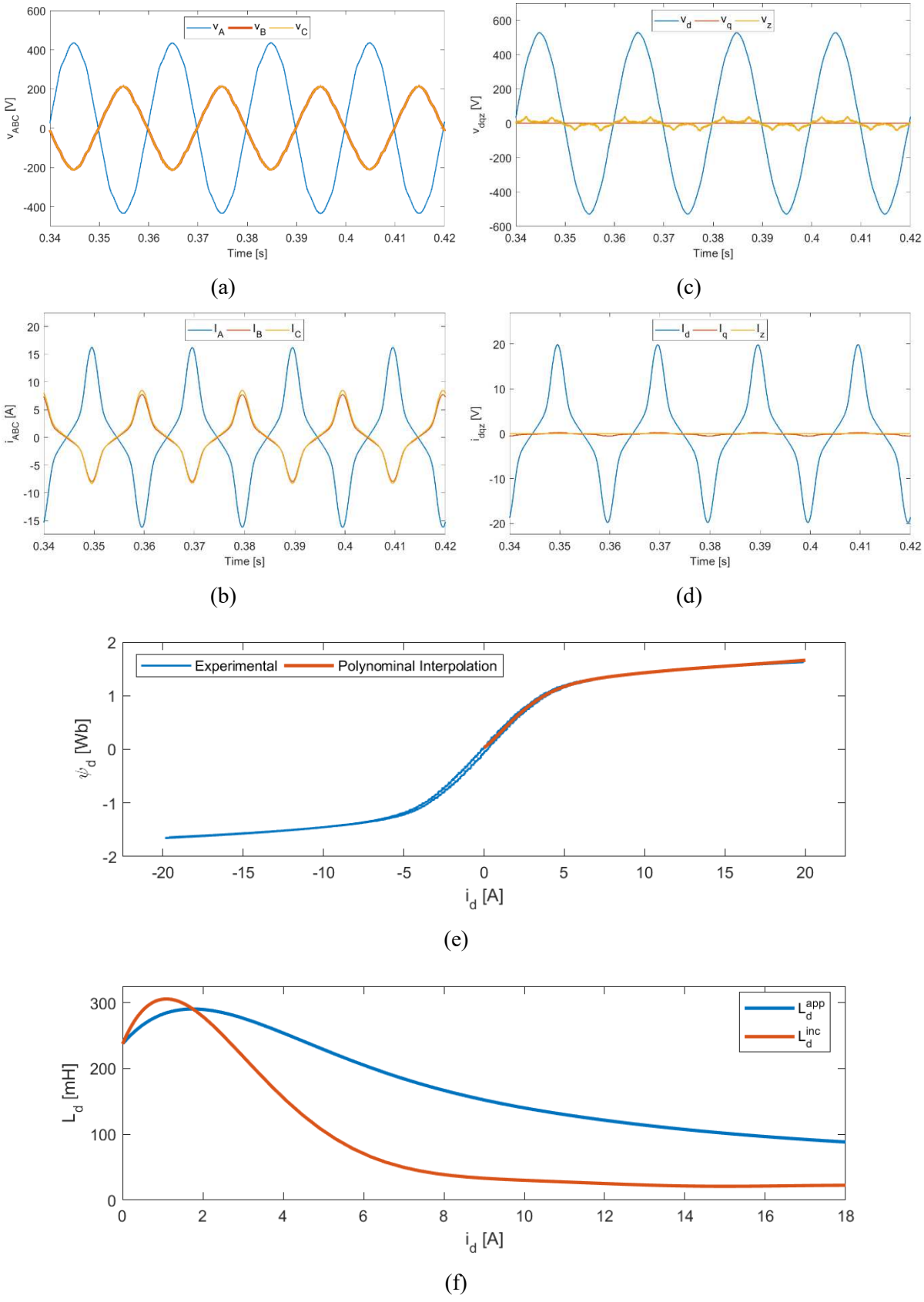


Fig. 3.6. *d*-axis experimental waveforms ($\theta_e=2\theta_m=0$). (a) v_{ABC} ; (b) i_{ABC} ; (c) v_{dqz} ; (d) i_{dqz} ; (e) $\psi_d=f(i_d)$; (f) *d* axis apparent and incremental inductances as function of i_d.

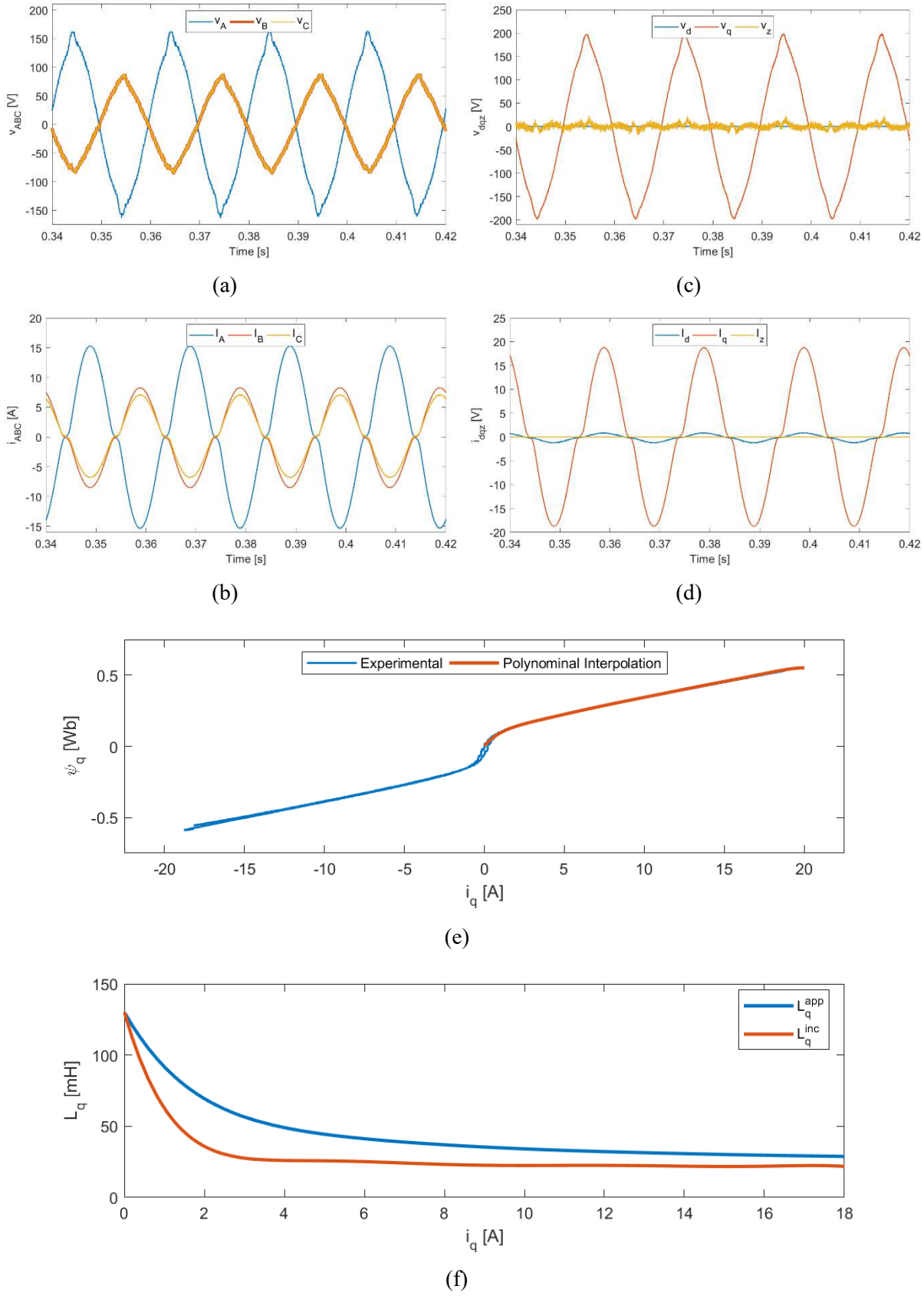
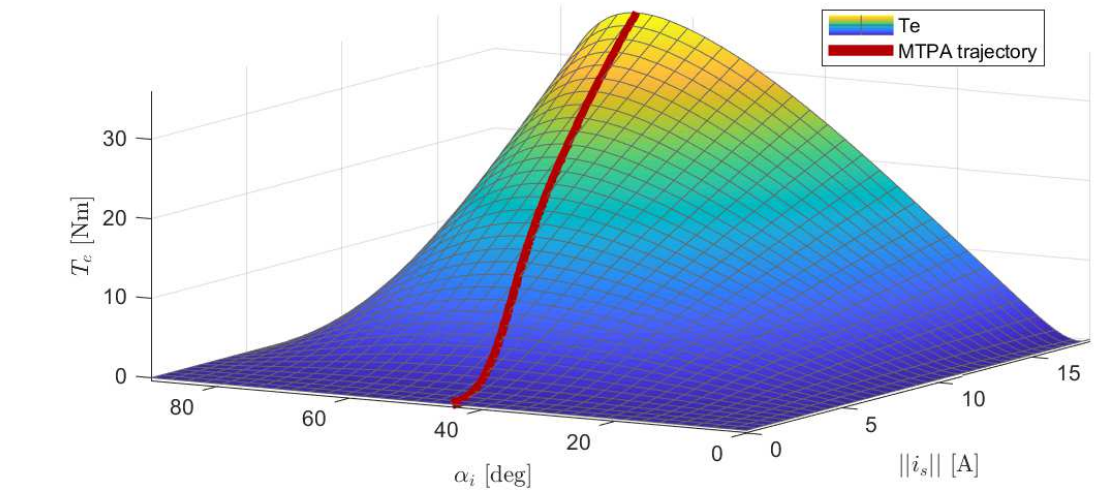


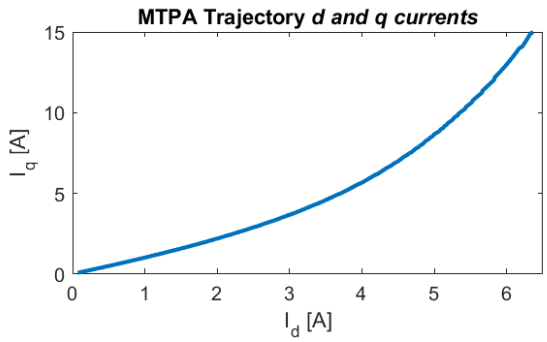
Fig. 3.7. q-axis experimental waveforms ($\theta_e=2\theta_m=\pi/2$). (a) v_{ABC} ; (b) i_{ABC} ; (c) v_{dqz} ; (d) i_{dqz} ; (e) $\psi_q=f(i_q)$; (f) q axis apparent and incremental inductances as function of i_q.

The analytical interpolation of the *d* and *q* flux curves was performed with good results in [108] by recurring to high order polynomial functions. The same approach is followed in this thesis, with both the *d* and *q* flux curves being interpolated by a nth order polynomial function as given by (3.15) for a general '*x*' axis. For the SynRM considered in this work, 9th order functions were selected whose coefficients are presented in Table 3.2. It is then possible to compute the SynRM torque as a function of the stator current magnitude, $\|i_s\| = \sqrt{i_d^2 + i_q^2}$ (assuming ZSC are kept null), and current angle. This allows the extraction of the MTPA trajectory as shown in Fig. 3.8.(a), composed by the pairs of i_d and i_q presented in Fig. 3.8.(b), resulting in the Torque per Ampere characteristic shown in Fig. 3.8.(c).

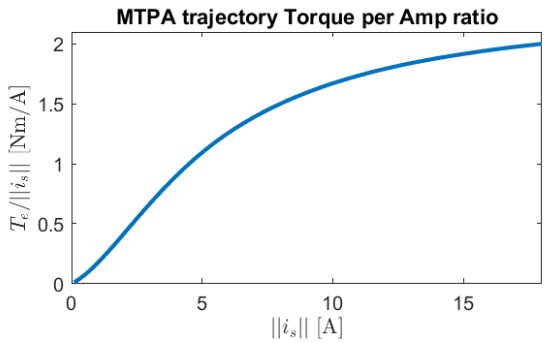
$$\psi_x(i_x) = p_0 i_x^0 + p_1 i_x^1 + p_2 i_x^2 + \ldots + p_n i_x^n \tag{3.15}$$



(a)



(b)



(c)

Fig. 3.8. Extracted MTPA trajectory for the ABB 3kW SynRM. (a) Electromagnetic torque as function of stator current magnitude and current angle. (b) MTPA pairs of i_d and i_q. (c) MTPA developed Torque per Ampere characteristic.

From Fig. 3.8.(a) and Fig. 3.8.(b), it is possible to conclude that the MTPA trajectory starts at a current angle of 45º, but as magnetic saturation gets more accentuated, the current angle is increased. This result, was expected as stated in the previous subsection, showing the importance of including magnetic saturation in the modelling and control of SynRMs [49][100][104][109].

Table 3.2: *d* and *q* axis flux polynomial interpolation coefficients.

	p_0	p_1	p_2	p_3	p_4	p_5	p_6	p_7	p_8	p_9
ψ_d	2.710E-02	2.373E-01	7.222E-02	-3.166E-02	5.172E-03	-4.657E-04	2.494E-05	-7.869E-07	1.338E-08	-9.302E-11
ψ_q	2.897E-03	1.301E-01	-4.936E-02	1.279E-02	-1.976E-03	1.878E-04	-1.098E-05	3.798E-07	-6.975E-09	5.031E-11

3.4 – SynRM Control strategies

Electrical machines control strategies may be classified as scalar and as vector control techniques. The scalar methods are the simplest and commonly found in industrial VSDs, being the V/f method the most popular among them. Scalar control methods are developed considering the steady state model of the machine, acting on the amplitude of the controlled quantities and its frequency. This allows a low-cost and low-complexity implementation but results in poor dynamic performance, where the tracking of the reference speed is not guaranteed [47].

Vector control techniques are based on a motor model valid for transient conditions, considering not only the amplitude of the controlled quantities but also its phase, allowing independent control of flux and torque. This way vector control techniques offer a boost in the performance of VSDs. For SynRM, the most popular vector control techniques are the FOC and the Direct Torque Control (DTC).

In FOC methods, the SynRM stator currents are split into their flux and torque producing components, i_d and i_q respectively [46], being their reference values obtained through one operating trajectory as indicated in section 3.2. A common SynRM speed control algorithm structure based on FOC is presented in Fig. 3.9. It commonly features a proportional integral linear (PI) controller to generate a reference of required torque based on the error in SynRM speed, followed by the transformation of this reference torque into *d* and *q* reference currents based on the selected operating trajectory. The reference currents are controlled using two PIs,

one for each axis current by generating a reference *d* and *q* axis voltage that is modulated to the SynRM through SVM. For OEW SynRMs, the FOC may be applied exactly in the same way, if the modulated zero-sequence voltage applied to the machine is kept null.

The main advantages of FOC are its high steady-state performance, precise current control, and fixed switching frequency operation [47]. On its drawbacks, FOC is characterized by a relatively high computational burden and limited dynamic behaviour due to the slow response of the linear controllers coupled to the modulator.

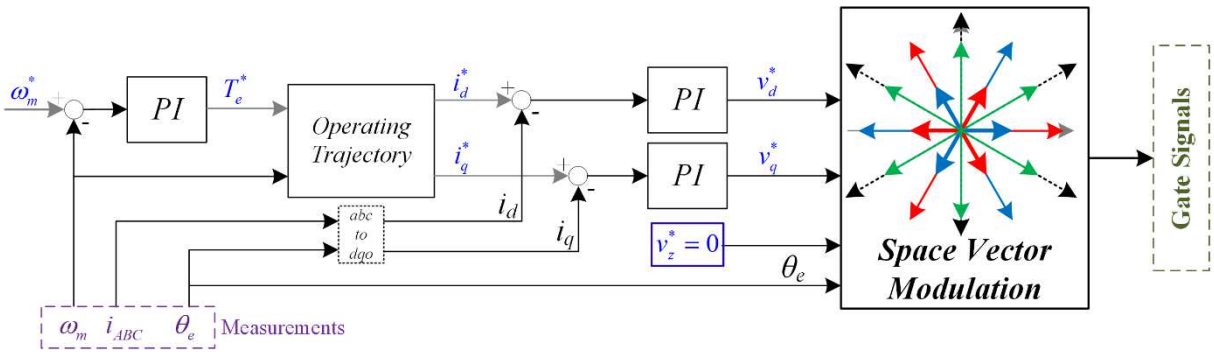


Fig. 3.9. FOC based speed control structure of SynRM.

While in FOC the flux and torque are regulated by its corresponding current producing components, in DTC the flux and torque quantities are directly regulated in a stationary *αβ* reference frame. For this, an estimator of flux is implemented by (3.16), and the torque estimation is performed using (3.17). Note that the flux observer allows an estimation of the flux phase, which allows inherent sensorless operation capability.

$$\begin{cases} \hat{\psi}_\alpha = \int \left(v_\alpha - R_s i_\alpha \right) dt \\ \hat{\psi}_\beta = \int \left(v_\beta - R_s i_\beta \right) dt \end{cases} \Rightarrow \begin{cases} \left\| \hat{\psi}_s \right\| = \sqrt{\hat{\psi}_\alpha^2 + \hat{\psi}_\beta^2} \\ \hat{\theta}_{\psi_s} = \tan^{-1}\left(\dfrac{\hat{\psi}_\beta}{\hat{\psi}_\alpha} \right) \end{cases} \tag{3.16}$$

$$\hat{T}_e = p\left(\hat{\psi}_\alpha i_\beta - \hat{\psi}_\beta i_\alpha \right) \tag{3.17}$$

The regulation of torque and flux is performed using hysteresis controllers that state if the controlled quantities must be increased or decreased. This is accomplished by acting on the converter switching states that allow direct and independent control of both quantities. For an OEW SynRM supplied by a DVSI, one possible DTC switching table is presented in Fig. 3.10.(a) with the stationary *αβ* reference frame sectors shown in Fig. 3.10.(b) [110]. The

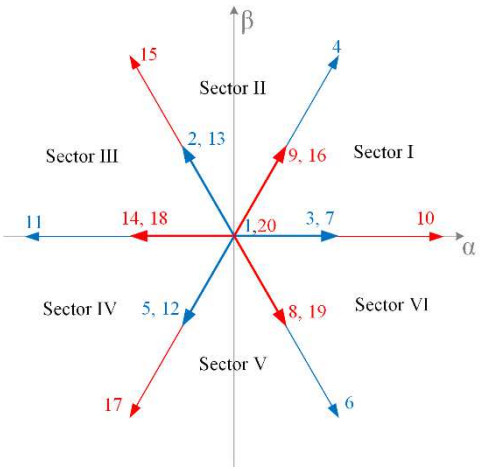
switching states numeration of Fig. 3.10 is in accordance with the numeration presented in section 2.2 of this document.

Note that for an OEW SynRM, the elimination of ZSC in FOC is performed by modulating null zero-sequence supply voltage. For DTC, the elimination of ZSC requires an extra hysteresis controller to accomplish this task. A speed control algorithm structure based on DTC for OEW SynRM is presented in Fig. 3.11.

The main advantages of DTC are its extremely fast torque response while maintaining little sensitivity to machine parameter variations, and its simplicity due to the absence of modulators and current controllers. This is not entirely true on OEW arrangements due to requiring control of ZSC. Still, if ZSC is kept close to zero, its impact on the SynRM dynamic behaviour should be minimal. On its drawbacks, DTC is characterized by originating high torque and flux ripples, switching at variable frequency, currents with relatively high THD and poor performance at low speed which may jeopardize the speed tracking of the drive and the quality of torque and flux [47].

i_z	$\lVert\hat{\psi}_s\rVert$	$\hat{T}_e$	$\hat{\theta}_{\psi_s}$ Sector I	II	III	IV	V	VI
↗	↗	↗	4	2	11	5	6	3
		↘	6	3	4	2	11	5
	↘	↗	2	11	5	6	3	4
		↘	5	6	3	4	2	11
↘	↗	↗	9	15	14	17	8	10
		↘	8	10	9	15	14	17
	↘	↗	15	14	17	8	10	9
		↘	17	8	10	9	15	14

(a)



(b)

Fig. 3.10. OEW SynRM DTC. (a) DTC switching table. (b) stationary reference frame sectorization. Courtesy of [110].

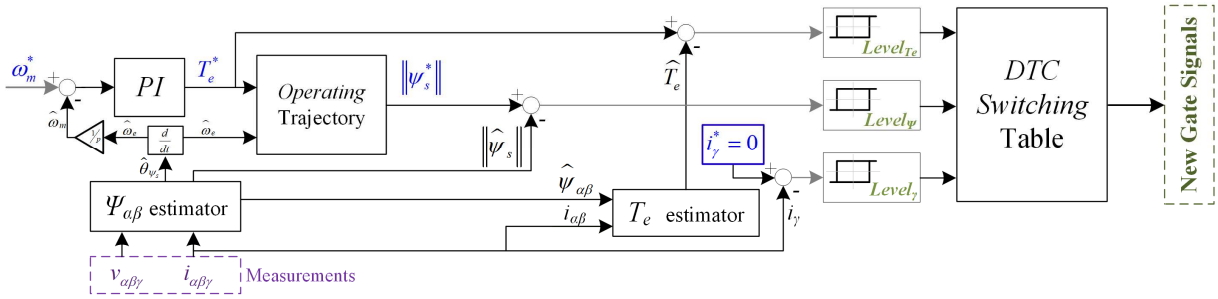


Fig. 3.11. DTC based speed control structure of OEW SynRM.

A mention is given to model predictive controllers (MPC) that are becoming popular among researchers by allowing simple and high-performance control of SynRMs [47]. MPCs allow the control of multiple objectives while considering several constraints by using a suitable cost function. In most MPCs, this cost function is computed for all possible switching states at every sampling period, being the switching state that minimizes the cost function the optimal switching state to be applied during the next sampling period, while the computation of the cost function is repeated. Although presenting a simple solution for control of SynRMs with very promising results in the literature [46][104][111], MPC require very high computational burden due to the computation of the cost function for every switching state in every sampling instant. This may be practical for traditional VSIs that only feature 8 switching states, but for the converter topology used in this thesis it would require the computation of the cost function for 576 switching states (64 from the output stage and 9 from the input stage). Even if some switching states could be disregarded depending on some constraints in each sampling period, it would result in a giant computational burden, considered not feasible in a practical manner.

CHAPTER 4

OEW SYNRM DRIVE BASED ON IMC WITH CMV REDUCTION

In this chapter, the main contributions of this thesis are presented with simulation results. These can be divided in two major parts:

- Adaptive SynRM speed FOC based on a backstepping non-linear control technique;
- Novel SVM method for the IMC with DVSI output featuring CMV reduction.

On the SynRM speed controller, a novel non-linear adaptive control approach based on Lyapunov control theory featuring backstepping is proposed in section 4.1, along with estimation techniques for both mechanical and electrical quantities.

Then, in section 4.2, emphasis is given to the development of a novel SVM technique that allows a reduction of the CMV at the machine terminals while improving the input and output waveforms quality.

The whole system, composed by the SynRM supplied by the OEW IMC, is implemented in simulation in section 4.3. In subsection 4.3.1 emphasis is given to the comparison of the VSD performance with a typical FOC structure based in PI controllers and the proposed modified FOC structure recurring to non-linear control theory. Subsection 4.3.2 is devoted to demonstrating that the novel SVM technique proposed in this work is capable of both reducing the CMV while improving the input and output waveforms quality when compared to the state-of-the-art SVM technique for CMV reduction covered in chapter 2.

4.1 – Adaptive non-linear Backstepping Speed controller for SynRM

The SynRM working principle, operation and its most common control strategies have been introduced in chapter 3 with significant detail. Although it is known that every type of electric machine is affected by the magnetic saturation, because SynRM torque production depends on the difference between the direct and quadrature axis inductances, being the quadrature axis characterized by possessing flux barriers and small iron bridges that allow magnetic flux to

flow, SynRMs operate with much greater saturation levels than most types of electrical machines. FOC is SynRMs most common and with better steady state performance control strategy. Traditionally, this technique features three different and independent PI controllers, one for each controlled quantity (mechanical angular velocity and direct and quadrature currents).

This section is devoted to the proposal of a modified SynRM speed FOC scheme whose objective is to achieve an improved dynamic response, while maintaining the very good steady state response of traditional FOC schemes. For this, a non-linear backstepping controller approach is proposed. The backstepping approach breaks the full system control problem into a sequence of lower order subsystems control problems and recursively use some states as "virtual controls" to obtain the intermediate control laws using Lyapunov functions to achieve stability [112].

The idea is to find the optimal voltage reference to be modulated through the IMC with DVSI, utilizing a novel SVM strategy to be proposed in section 4.2, that allows a SynRM speed control with excellent steady state response, improved dynamic response and reduced CMV.

Let us start considering the speed dynamics (from section 3.1) of the SynRM and defining the speed error, e_ω, by (4.1) and its integral e_I by (4.2). We can choose a Lyapunov function, V_0, based on these two quantities, given by (4.3). Note that by setting k_I as a positive constant, V_0 is a positive semi-definite function, guaranteeing $V_0 \geq 0$ at every instant.

$$e_\omega = \omega_{ref} - \omega \tag{4.1}$$

$$e_I = \int_0^t e_\omega dt \tag{4.2}$$

$$V_0 = k_I \frac{e_I^2}{2} + \frac{e_\omega^2}{2} \tag{4.3}$$

Since V_0 is a positive semi-definite function, if its time derivative is a negative semi-definite function, then according to the 2nd method of Lyapunov stability, the error e_ω will asymptotically converge to zero, resulting in the speed reference being followed ($\omega=\omega_{ref}$). The time derivative of V_0 is given by (4.4), where $d = \frac{T_{load}}{J}$ and $b = \frac{k_D}{J}$.

$$\frac{dV_0}{dt} = k_I e_I e_\omega + e_\omega \left(\frac{d\omega_{ref}}{dt} - \frac{d\omega}{dt} \right) = k_I e_I e_\omega + e_\omega \left(\frac{d\omega_{ref}}{dt} - \frac{T_e}{J} + d + b\omega \right) \tag{4.4}$$

To guarantee that $\frac{dV_0}{dt} \leq 0$, let us make $\frac{dV_0}{dt} = -k_\omega e_\omega^2$, where k_ω is a positive constant. It is now possible to compute the desired electromagnetic torque, T_e^*, that enforces this condition, as given by (4.5).

$$\begin{aligned} &\frac{dV_0}{dt} = -k_\omega e_\omega^2 \Leftrightarrow \\ &\Leftrightarrow k_1 e_1 e_\omega + e_\omega \left(\frac{d\omega_{ref}}{dt} - \frac{T_e^*}{J} + d + b\omega \right) = -k_\omega e_\omega^2 \Leftrightarrow \\ &\Rightarrow T_e^* = J \left(k_1 e_1 + k_\omega e_\omega + \frac{d\omega_{ref}}{dt} + d + b\omega \right) \end{aligned} \tag{4.5}$$

Note that the desired electromagnetic torque requires the knowledge of every machine parameter (J, b, d). Let us consider that the parameters J and b are possible to be measured in the laboratory, and invariant during operation. On the other hand, $d = \frac{T_{load}}{J}$, is greatly dependent on the operation conditions, meaning that d should be estimated. For this, a modification to the Lyapunov function proposed in (4.3) must be performed, with the new Lyapunov function, V_1, given by (4.6), where γ_d is the estimation gain that must be a positive constant, and $\tilde{d}$ is the error of d estimation given by (4.7). $\hat{d}$ is the observed value.

$$V_1 = k_1 \frac{e_1^2}{2} + \frac{e_\omega^2}{2} + \frac{\tilde{d}^2}{2\gamma_d} \tag{4.6}$$

$$\tilde{d} = d - \hat{d} \tag{4.7}$$

Accounting with the estimation of d, the reference torque is given by (4.8).

$$T_e^* = J \left(k_1 e_1 + k_\omega e_\omega + \frac{d\omega_{ref}}{dt} + \hat{d} + b\omega \right) \tag{4.8}$$

The time derivative of V_1 is given by (4.9). Again, to guarantee that V_1 is a negative semi-definite function, let us set $\frac{dV_1}{dt} = -k_\omega e_\omega^2$. This requires $e_\omega - \frac{\dot{\hat{d}}}{\gamma_d} = 0$, resulting in the adaptation law given by (4.10).

$$\begin{aligned}
\frac{dV_1}{dt} &= k_I e_I e_\omega + e_\omega\left(\frac{d\omega_{ref}}{dt} - \frac{T_e^*}{J} + d + b\omega\right) - \frac{\tilde{d}\,\dot{\hat{d}}}{\gamma_d} = \\
&= k_I e_I e_\omega + e_\omega\left(\frac{d\omega_{ref}}{dt} - \frac{J\left(k_I e_I + k_\omega e_\omega + \dfrac{d\omega_{ref}}{dt} + \hat{d} + b\omega\right)}{J} + d + b\omega\right) - \frac{\tilde{d}\,\dot{\hat{d}}}{\gamma_d} = \\
&= -k_\omega e_\omega^{\,2} + e_\omega \tilde{d} - \frac{\tilde{d}\,\dot{\hat{d}}}{\gamma_d} = \\
&= -k_\omega e_\omega^{\,2} + \tilde{d}\left(e_\omega - \frac{\dot{\hat{d}}}{\gamma_d}\right)
\end{aligned} \tag{4.9}$$

$$\dot{\hat{d}} = \gamma_d e_\omega \quad \Rightarrow \quad \hat{d} = \gamma_d \int_0^t e_\omega dt \tag{4.10}$$

Since the estimation of d is obtained through the integral of the velocity error and a positive and constant gain γ_d, it can be included in the integral action of the controller given by (4.2). The resulting electromagnetic torque reference, considering the estimation of d is given by (4.11).

$$\begin{aligned}
T_e^* &= J\left(k_I e_I + k_\omega e_\omega + \frac{d\omega_{ref}}{dt} + \hat{d} + b\omega\right) = \\
&= J\left(k_I \int_0^t e_\omega dt + k_\omega e_\omega + \frac{d\omega_{ref}}{dt} + \gamma_d \int_0^t e_\omega dt + b\omega\right) = \\
&= J\left(\left[k_I + \gamma_d\right]\int_0^t e_\omega dt + k_\omega e_\omega + \frac{d\omega_{ref}}{dt} + b\omega\right)
\end{aligned} \tag{4.11}$$

To select the controller gains k_ω, k_I and γ_d for an accurate speed tracking reference, one may write (4.8) in the Laplace domain and compare it with a second order system in its canonical form, as given in (4.12), where ζ is the damping ration. This yields a relation between the total integral gain, $k_{Id} = K_I + \gamma_d$, and the proportional gain, k_ω.

$$\begin{cases} E_\omega\left[\left(k_I + \gamma_d\right) + k_\omega s + s^2\right] = 0 \\ \omega_0^2 + 2\zeta\omega_0 s + s^2 = 0 \end{cases} \Rightarrow \begin{cases} k_\omega = 2\zeta\omega_0 \\ \left(k_I + \gamma_d\right) = \omega_0^2 \end{cases} \tag{4.12}$$

As shown in section 3.4, the SynRM torque generation is function of the direct and quadrature currents and inductances. To obtain the required reference torque, the SynRM direct and

quadrature currents must be controlled. Let us define the quadrature current error and its derivative by (4.13) and the direct current error and its derivative by (4.14).

$$e_q = i_q^* - i_q \Rightarrow \frac{de_q}{dt} = \frac{di_q^*}{dt} - \frac{di_q}{dt} \tag{4.13}$$

$$e_d = i_d^* - i_d \Rightarrow \frac{de_d}{dt} = \frac{di_d^*}{dt} - \frac{di_d}{dt} \tag{4.14}$$

Consider the positive semidefinite Lyapunov function V_2 given by (4.15). Let us define the error in the SynRM electromagnetic torque as $e_T = T_e^* - T_e \Rightarrow T_e = T_e^* - e_T$. Since $\frac{dV_1}{dt} = -k_\omega e_\omega^2$, the derivative of V_2 is computed through (4.16), where $\frac{di_q}{dt}$ is obtained based on the SynRM model given by (3.8).

$$V_2 = k_I \frac{e_I^2}{2} + \frac{e_\omega^2}{2} + \frac{e_q^2}{2} \tag{4.15}$$

$$\begin{aligned} \frac{dV_2}{dt} &= k_I e_I e_\omega + e_\omega \frac{de_\omega}{dt} + e_q \frac{de_q}{dt} = \\ &= k_I e_I e_\omega + e_\omega \left(\frac{d\omega_{ref}}{dt} - \frac{T_e}{J} + d + b\omega \right) + e_q \left(\frac{di_q^*}{dt} - \frac{v_q^* - R_s i_q - \omega_e L_d i_d}{L_q^{inc}} \right) = \\ &= -k_\omega e_\omega^2 + \frac{e_\omega e_T}{J} + e_q \left(\frac{di_q^*}{dt} - \frac{v_q^* - R_s i_q - \omega_e L_d i_d}{L_q^{inc}} \right) \end{aligned} \tag{4.16}$$

At this point, it is important to take a closer look at e_T, given by (4.17).

$$\begin{aligned} e_T &= T_e^* - T_e = p\left(L_d - L_q\right) i_d^* i_q^* - p\left(L_d - L_q\right) i_d i_q \\ &= p\left(L_d - L_q\right)\left(i_d^* i_q^* - i_d \left[i_q^* - e_q \right]\right) \\ &= p\left(L_d - L_q\right)\left(i_q^* e_d + e_q i_d\right) \end{aligned} \tag{4.17}$$

Assuming that the direct axis is stabilized, $e_d = 0 \Rightarrow e_T = p\left(L_d - L_q\right) e_q i_d$, one can make $\frac{dV_2}{dt} = -k_\omega e_\omega^2 - k_q e_q^2$, where k_q is a positive constant, guaranteeing $\frac{dV_2}{dt} \le 0$. It is possible to solve (4.16) to obtain the reference quadrature axis voltage v_q^*, given by (4.18).

$$v_q^* = L_q^{inc}\left(k_q e_q + \frac{p\left(L_d - L_q\right) i_d e_\omega}{J} + \frac{di_q^*}{dt} \right) + R_s i_q + \omega_e L_d i_d \tag{4.18}$$

The same logic may be applied to the SynRM direct axis, by defining the positive semidefinite Lyapunov function V_3 given by (4.19), whose derivative is given by (4.20), where $\frac{di_d}{dt}$ is obtained based on the SynRM model given by (3.8).

$$V_3 = k_1 \frac{e_1^2}{2} + \frac{e_\omega^2}{2} + \frac{e_q^2}{2} + \frac{e_d^2}{2} \tag{4.19}$$

$$\begin{aligned} \frac{dV_3}{dt} &= k_1 e_1 e_\omega + e_\omega \frac{de_\omega}{dt} + e_q \frac{de_q}{dt} + e_d \frac{de_d}{dt} \\ &= -k_\omega e_\omega^2 - k_q e_q^2 + e_d \left(\frac{di_d^*}{dt} - \frac{v_d^* - R_s i_d + \omega_e L_q i_q}{L_d^{inc}} \right) \end{aligned} \tag{4.20}$$

Making $\frac{dV_3}{dt} = -k_\omega e_\omega^2 - k_q e_q^2 - k_d e_d^2$, where k_d is a positive constant, guaranteeing $\frac{dV_3}{dt} \leq 0$. It is possible to solve (4.20) to obtain the reference direct axis voltage v_d^* , given by (4.21).

$$v_d^* = L_d^{inc}\left(k_d e_d + \frac{di_d^*}{dt} \right) + R_s i_d - \omega_e L_q i_q \tag{4.21}$$

Note that the computed reference voltages require the electrical parameters to be known. In case of the winding resistance, if the resistance measurement is performed at the regular operating temperature it may be acceptable to consider that it does not vary significantly, assuming it to be constant. In the case of direct and quadrature inductances this is not acceptable as discussed in chapter 3 due to the significant iron saturation in which the SynRM can operate. Thus, it is required to estimate the SynRM direct and quadrature inductances. This thesis proposes the use of the Recursive Least Squares (RLS) algorithm for online estimation of SynRM electrical parameters L_d and L_q, while the winding resistance is assumed to be constant.

The RLS algorithm estimates the system output at instant k, $\left[\hat{y}_{(k)}\right]$, using measured values, $\left[\varphi_{(k)}\right]$, and previously estimated system parameters, $\left[\hat{\theta}_{(k-1)}\right]$. For this, it is required that the system dynamics may be written linearly to the estimated system parameters matrix, as given by (4.22) . Then, the estimated output is compared with the real system measured output, $\left[y_{(k)}\right]$ as given by (4.23), allowing the computation of an estimation error matrix, $\left[\varepsilon_{(k)}\right]$.

$$\left[\hat{y}_{(k)}\right]=\left[\varphi_{(k)}\right]^{T}\left[\hat{\theta}_{(k-1)}\right] \tag{4.22}$$

$$\left[\varepsilon_{(k)}\right]=\left[y_{(k)}\right]-\left[\hat{y}_{(k)}\right] \tag{4.23}$$

The parameter matrix is updated, $\left[\hat{\theta}_{(k)}\right]$, based on the previous parameter estimation, $\left[\hat{\theta}_{(k-1)}\right]$, summed by a correction factor resulting from the gain matrix, $\left[L_{(k)}\right]$, multiplied by the estimation error, $\left[\varepsilon_{(k)}\right]$, as given by (4.24).

$$\left[\hat{\theta}_{(k)}\right]=\left[\hat{\theta}_{(k-1)}\right]+\left[L_{(k)}\right]\left[\varepsilon_{(k)}\right] \tag{4.24}$$

The gain matrix is obtained through (4.25), where $\left[P_{(k-1)}\right]$ is the covariance matrix of the previous instant, and λ is the forgetting factor. The updated covariance matrix is obtained through (4.26).

$$\left[L_{(k)}\right]=\frac{\left[P_{(k-1)}\right]\left[\varphi_{(k)}\right]}{\lambda[I]+\left[\varphi_{(k)}\right]^{T}\left[P_{(k-1)}\right]\left[\varphi_{(k)}\right]} \tag{4.25}$$

$$\left[P_{(k)}\right]=\left([I]-\left[L_{(k)}\right]\left[\varphi_{(k)}\right]^{T}\right)\left[P_{(k-1)}\right]\frac{1}{\lambda} \tag{4.26}$$

The forgetting factor introduces a way to exponentially forget old data, giving more importance to recent data. This factor is such that $0\leq\lambda\leq1$, taking more old data into account the closer to 1 it is, being typical values set to 0.95~0.99.

As introduced in chapter 3, due to iron magnetic saturation, the SynRM inductances can be classified as apparent and incremental inductances. The apparent inductances are responsible for the torque production and electromotive forces, while the incremental inductances are responsible for the electrical dynamics of currents. Taking a closer look at the SynRM mathematical model given by (3.8) and (3.9), one may conclude that the effect of incremental inductances is neglectable in steady state. Also, whenever there is a change in the currents, the inductances vary, requiring the RLS estimator to converge to the new inductance values. For these reasons, the RLS algorithm implemented only considers the existence of apparent inductances. The RLS algorithm applied to the SynRM is given through (4.27)-(4.29), where T_{rls} is the timestep of the RLS observer, $\Delta i_{d\,(k)}=i_{d\,(k)}-i_{d\,(k-1)}$ and $\Delta i_{q\,(k)}=i_{q\,(k)}-i_{q\,(k-1)}$.

$$\left[\hat{\theta}_{(k-1)}\right]=\begin{bmatrix}\hat{L}_{d\,(k-1)}\\ \hat{L}_{q\,(k-1)}\end{bmatrix} \tag{4.27}$$

$$\left[y_{(k)}\right]=T_{rls}\begin{bmatrix}v_{d\,(k)}-R_s i_{d\,(k)}\\ v_{q\,(k)}-R_s i_{q\,(k)}\end{bmatrix} \tag{4.28}$$

$$\left[\varphi_{(k)}\right]^T=\begin{bmatrix}\Delta i_{d\,(k)} & -T_{rls}\omega_{e\,(k)} i_{q\,(k)}\\ T_{rls}\omega_{e\,(k)} i_{d\,(k)} & \Delta i_{q\,(k)}\end{bmatrix} \tag{4.29}$$

The estimated inductances at instant *k* are given by (4.30), with the gain matrix being computed using (4.25).

$$\begin{bmatrix}\hat{L}_{d\,(k)}\\ \hat{L}_{q\,(k)}\end{bmatrix}=\begin{bmatrix}\hat{L}_{d\,(k-1)}\\ \hat{L}_{q\,(k-1)}\end{bmatrix}+\left[L_{(k)}\right]\left(T_{rls}\begin{bmatrix}v_{d\,(k)}-R_s i_{d\,(k)}\\ v_{q\,(k)}-R_s i_{q\,(k)}\end{bmatrix}-\begin{bmatrix}\Delta i_{d\,(k)} & -T_{rls}\omega_{e\,(k)} i_{q\,(k)}\\ T_{rls}\omega_{e\,(k)} i_{d\,(k)} & \Delta i_{q\,(k)}\end{bmatrix}\begin{bmatrix}\hat{L}_{d\,(k-1)}\\ \hat{L}_{q\,(k-1)}\end{bmatrix}\right) \tag{4.30}$$

The full structure of the proposed SynRM adaptive non-linear backstepping speed FOC is shown in Fig. 4.1. When compared to the traditional FOC structure of Fig. 3.9, it is observed that the three linear PI controllers that output the electromagnetic torque reference and *dqz* frame reference voltages are replaced by the virtual control signals that stabilize the Lyapunov functions (V_1, V_2 and V_3), computed through (4.11), (4.18) and (4.21) respectively.

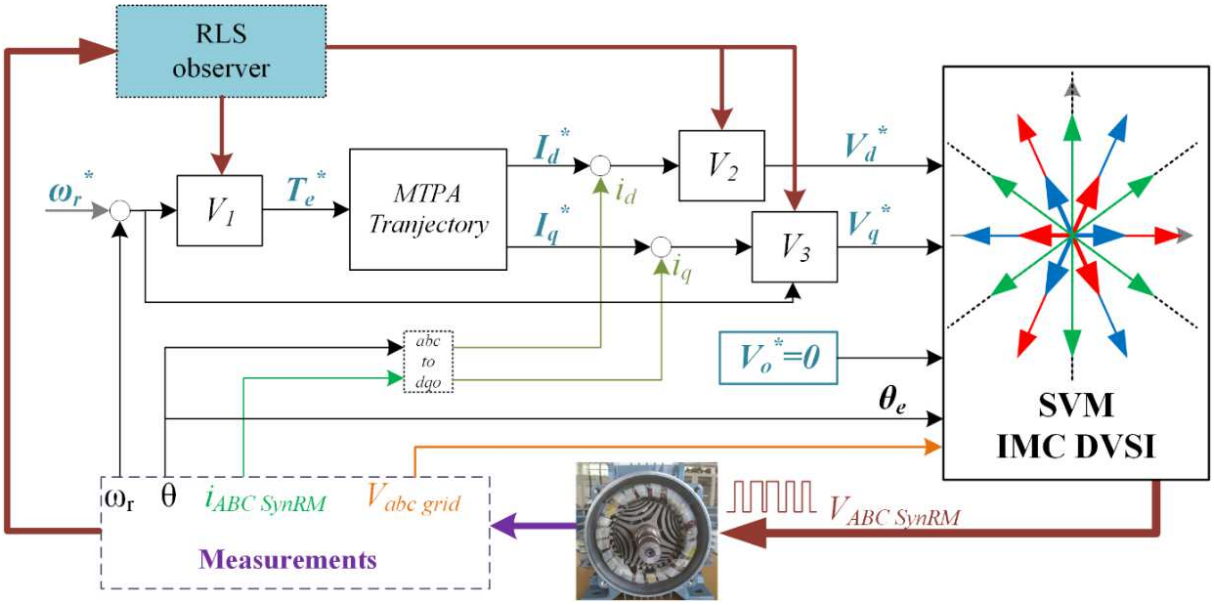


Fig. 4.1. Proposed adaptive non-linear backstepping speed FOC structure.

4.2 – Novel SVM strategy for CMV reduction

As concluded from the simulation results presented in chapter 2, in respect to the input stage modulation, the reduced dc-link strategy produces lower DVSI switching losses at the cost of increasing the CSR conduction losses while slightly deteriorating the input currents and voltages waveforms. The converter efficiency improvement introduced by the reduced dc-link strategy is valid until the point where the CSR conduction losses reach the DVSI switching losses, from this operating point onwards the most efficient input stage SVM technique is the maximum dc-link voltage strategy.

On the output stage, it was concluded that the SVM strategy that uses Group I DVSI switching states allows a reduction in the drive CMV by eliminating the contribution of the output stage, v_{cm0}. In that case, the CMV is only consequence of the input stage contribution, v_{0G}. On the other hand, the quality of both input and output stage waveforms is negatively affected when compared to the SVM strategy featuring Group II switching states, being the output currents the most affected quantities.

There is also an important note to be made relative to the CSR switching current. With DVSI Group I vectors, the input stage switching happens when the DVSI null vectors 1 and 20 are selected resulting in a soft dc-link current close to zero, if ZSC is close to zero ($i_{dc}=i_A+i_B+i_C$ or $i_{dc}=-(i_A+i_B+i_C)$). With the strategy featuring Group II vectors, the soft dc-link current is truly null ($i_{dc}=0$) because the load currents are freewheeled through the DVSI switches. Although the two SVM strategies should result in negligible CSR switching losses, the strategy featuring Group II vectors does not require any special multistep commutation logic for the bidirectional switches other than deadtimes, while the strategy featuring the Group I vectors does require an input voltage based multistep commutation logic.

It seems that the only true advantage of the output stage modulation using DVSI Group I vectors is the reduction of CMV. If there is a way of accomplishing CMV reduction with vectors from Group II, maybe some of the properties offered by the modulation technique presented in section 2.3.1 can be maintained while still decreasing CMV.

It has been pointed out in chapter 2 that the DVSI Group II switching states come as pairs, one with $N_{sw} = 4$ and the other with $N_{sw} = 2$. According to (2.8), this means that the switching states from Group II Set I ($N_{sw}=4$) result in $v_{cm0} > 0$, while switching states from Group II Set II

($N_{sw} = 2$) result in $v_{cm0} < 0$. By selecting $N_{sw} = 4$ or $N_{sw} = 2$, one gain control over the polarity of v_{cm0}. By choosing v_{cm0} polarity to be contrary to the polarity of v_{0G}, the peak value of CMV should be reduced, even when compared to the strategy featuring DVSI Group I vectors.

Note that the choice of v_{cm0} polarity does vary the switching state (Set I or Set II) applied to the machine, but it does not affect the $\alpha\beta\gamma$ components of the output voltage vector applied to the load. Thus, the computation of duty cycles for the CSR (δ_{ρ}^{R}, δ_{σ}^{R}) and DVSI (δ_{κ}^{I}, δ_{λ}^{I}, δ_{o}^{I}) presented in section 2.2 and subsection 2.3.1 are still valid for this new method. On the other hand, the switching period structure presented in Fig. 2.17 may require changes because the input stage active vectors (ρ and σ) polarity of v_{0G} may be different from each other (v_{0G}^{ρ} and v_{0G}^{σ}).

Let us start by analysing the easiest case, where both v_{0G}^{ρ} and v_{0G}^{σ} have the same polarity. In such scenario, if v_{0G}^{ρ} and v_{0G}^{σ} are positive the output stage modulation should use the DVSI Group II Set II ($N_{sw} = 2$) as presented in Fig. 4.2(a), whereas in the case v_{0G}^{ρ} and v_{0G}^{σ} are negative the output stage modulation should use the DVSI Group II Set I ($N_{sw} = 4$) as shown in Fig. 4.2(b).

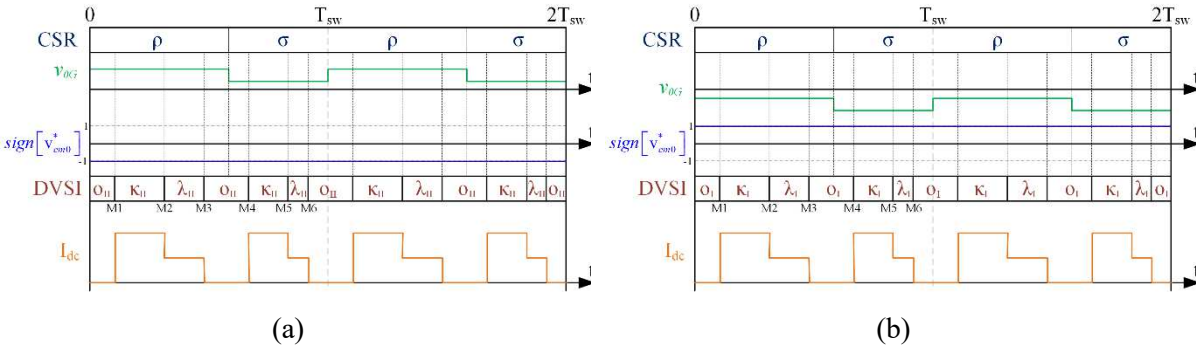
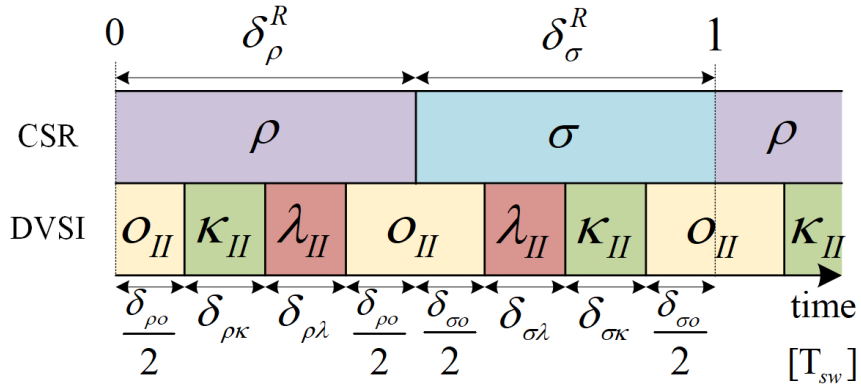


Fig. 4.2. Illustration of the proposed CMV reduction logic. (a) For both v_{0G}^{ρ} and v_{0G}^{σ} positive. (b) For both v_{0G}^{ρ} and v_{0G}^{σ} negative.

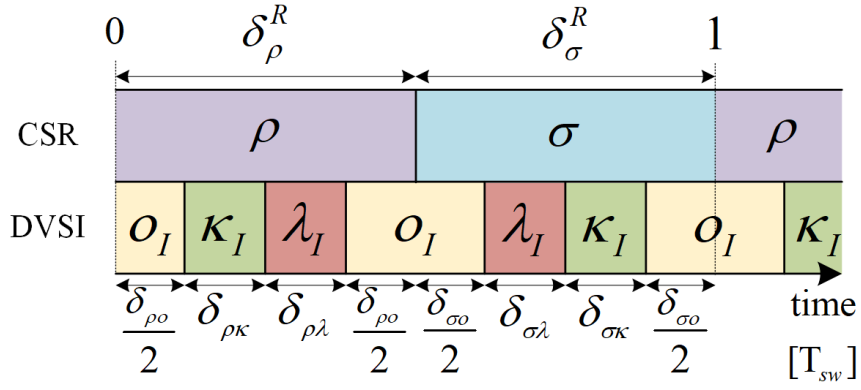
This scenario results in a switching period structure identical to the one of Fig. 2.17 with the vectors indicated in Table 2.6, being the only difference in the choice of the DVSI Group II Set according to the polarity of v_{0G}. The generalization of the situation where the polarity of v_{0G}^{ρ} and v_{0G}^{σ} is the same is detailed in Fig. 4.3.

Sector	Vector κ_I	Vector λ_I	Vector o_I	Vector κ_{II}	Vector λ_{II}	Vector o_{II}	φ^I_{ref}
I	24	22	36	25	26	35	θ_o
II	22	21	33	26	30	38	$\theta_o-\pi/3$
III	21	28	34	30	29	37	$\theta_o-2\pi/3$
IV	28	27	36	29	31	35	$\theta_o-\pi$
V	27	23	33	31	32	38	$\theta_o-4\pi/3$
VI	23	24	34	32	25	37	$\theta_o-5\pi/3$

(a)



(b)



(c)

Fig. 4.3. SVM strategy to reduce peak CMV for the situation where $sign(v^{\rho}_{0G}) = sign(v^{\sigma}_{0G})$. (a) Generalization of the switching states for the output vector sector. (b) Switching period structure for the case where $v_{0G}>0$. (c) Switching period structure for the case where $v_{0G}<0$.

However, if the polarities of v^{ρ}_{0G} and v^{σ}_{0G} are different, the choice of v_{cm0} polarity varies depending on their sign and requires swapping of v_{cm0} polarity upon the input stage switch between vector ρ and vector σ. Let us analyse the situation where $v^{\rho}_{0G}>0$ and $v^{\sigma}_{0G}<0$, presented in Fig. 4.4.(a). It is possible to observe that if the switching period structure is maintained equal

to the previously analysed case where $sign(v_{0G}^{\rho}) = sign(v_{0G}^{\sigma})$, this would require extra vector commutations (8 instead of 6). Also, one may see that the input stage switching happens at the same instant that the output stage switch between zero vectors. Although the dc-link current is null in both null vectors, the switching requires a deadtime which may result in a non-null dc-link current. This means that in some situations the input stage switching may not happen at zero current, requiring multistep commutation logic. The loss of the ability to switch the input stage without multistep commutation logic opens the door to the modification of the switching period structure of Fig. 4.4.(a) to the structure proposed in Fig. 4.4.(b). Where only 6 vector commutations are required on the output stage, restoring the number of commutations to the same as when v_{0G}^{ρ} and v_{0G}^{σ} have the same polarity.

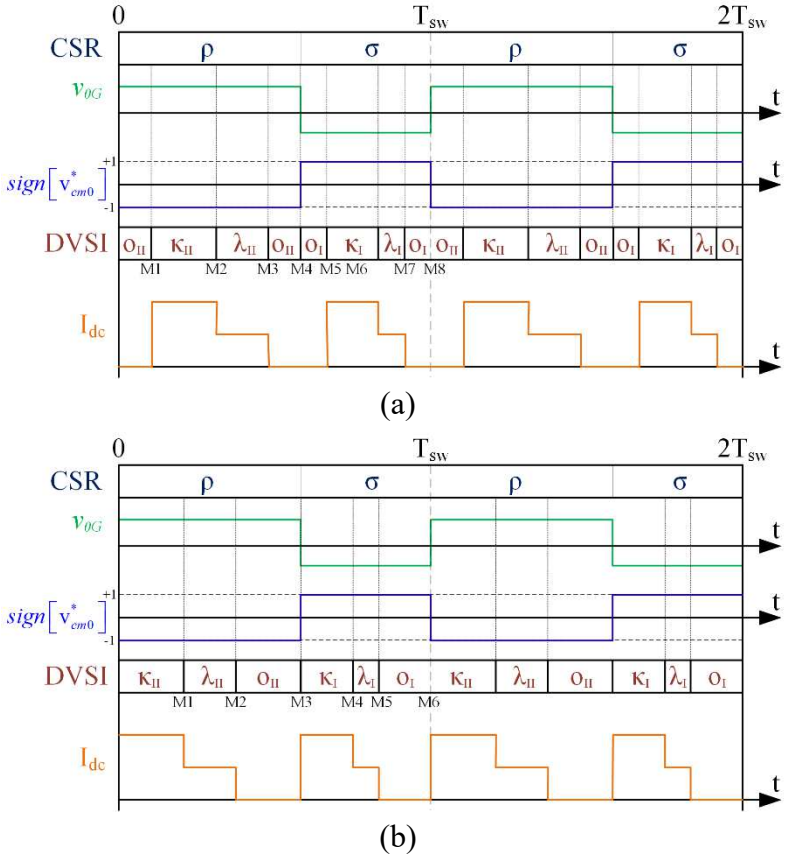
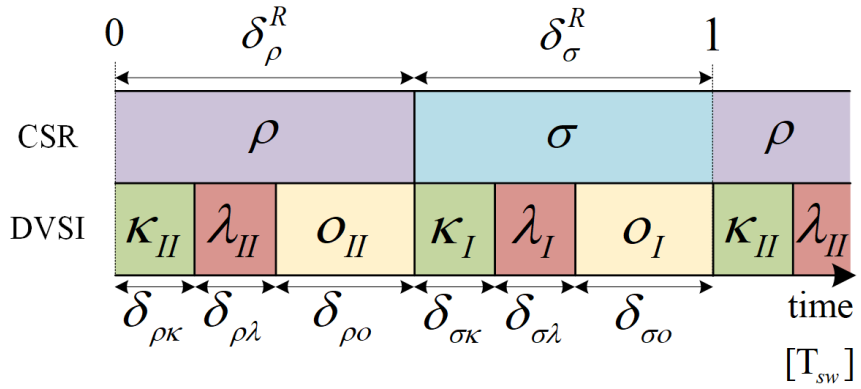


Fig. 4.4. Illustration of the proposed CMV reduction logic when $v_{0G}^{\rho} > 0$ and $v_{0G}^{\sigma} < 0$.
(a) Maintaining the previous switching period structure. (b) Modified switching period structure.

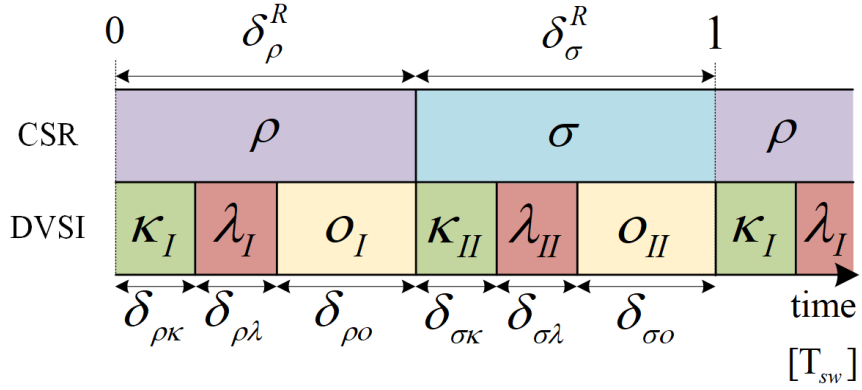
The generalization of the SVM method with reduced CMV for all output sectors when the polarities of v_{0G}^{ρ} and v_{0G}^{σ} are different is given in Fig. 4.5.(a), with the switching period structure for the case $v_{0G}^{\rho} > 0$ and $v_{0G}^{\sigma} < 0$ in Fig. 4.5.(b), and the case $v_{0G}^{\rho} < 0$ and $v_{0G}^{\sigma} > 0$ in Fig. 4.5.(c).

Sector	Vector κ_I	Vector λ_I	Vector o_I	Vector κ_{II}	Vector λ_{II}	Vector o_{II}	φ_{ref}^{I}
I	24	22	33	25	26	38	θ_o
II	22	21	34	26	30	37	$\theta_o-\pi/3$
III	21	28	36	30	29	35	$\theta_o-2\pi/3$
IV	28	27	33	29	31	38	$\theta_o-\pi$
V	27	23	34	31	32	37	$\theta_o-4\pi/3$
VI	23	24	36	32	25	35	$\theta_o-5\pi/3$

(a)



(b)



(c)

Fig. 4.5. SVM strategy to reduce peak CMV for the situation where $sign(v_{0G}^{\rho}) \neq sign(v_{0G}^{\sigma})$. (a) Generalization of the switching states for the output vector sector. (b) Switching period structure for the case when $v_{0G}^{\rho} > 0$ and $v_{0G}^{\sigma} < 0$. (c) Switching period structure for the case where $v_{0G}^{\rho} < 0$ and $v_{0G}^{\sigma} > 0$.

Comparing Fig. 4.3.(a) and Fig. 4.5.(a), it is possible to observe the null vectors used are not the same, this choice was performed to reduce the number of required commutations between

the active vectors with different signs of v_{cm0}. This is further detailed in Fig. 4.6, for an output voltage vector located in Sector I. One may observe that when the v_{0G} contributions of both ρ and σ vectors have the same polarity, Fig. 4.6.(a), only half of the DVSI arms switch while when $sign(v_{0G}^{\rho}) \neq sign(v_{0G}^{\sigma})$ all of the DVSI arms switch according to Fig. 4.6.(b). Still, the global amount of switching manoeuvrers is the same in both situations, which should maintain the switching losses approximately the same.

time → 0				d_ρ				T_{sw}				$T_{sw}+d_\rho$				$2T_{sw}$
CSR	ρ				σ				ρ				σ				
DVSI	36	24	22	36	36	22	24	36	36	24	22	36	36	22	24	36	
Arm A1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	
Arm B1	1	0	1	1	1	1	0	1	1	0	1	1	1	1	0	1	
Arm C1	1	1	0	1	1	0	1	1	1	1	0	1	1	0	1	1	
Arm A2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Arm B2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Arm C2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
N_{sw}	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	

(a)

time → 0				d_ρ				T_{sw}				$T_{sw}+d_\rho$				$2T_{sw}$
CSI	ρ				σ				ρ				σ				
DVSI	24	22	33	25	26	38	24	22	33	25	26	38					
Arm A1	1	1	1	1	1	0	1	1	1	1	1	0					
Arm B1	0	1	1	0	0	0	0	1	1	0	0	0					
Arm C1	1	0	0	0	0	1	1	0	0	0	0	1					
Arm A2	0	0	1	0	0	0	0	0	1	0	0	0					
Arm B2	1	1	1	1	0	0	1	1	1	1	0	0					
Arm C2	1	1	0	0	1	1	1	1	0	0	1	1					
N_{sw}	4	4	4	2	2	2	4	4	4	2	2	2					

(b)

Fig. 4.6. Output stage Arm signals for the proposed SVM method for an output voltage vector in the Sector I. Note that Arm 'x' equal to '1' means that the upper switch is ON and the bottom switch if OFF, while '0' means that the upper switch is OFF while the bottom switch if ON. (a) For the situation with $sign(v_{0G}^{\rho}) = sign(v_{0G}^{\sigma})$ and $v_{0G}<0$. (b) For the situation with $sign(v_{0G}^{\rho}) \neq sign(v_{0G}^{\sigma})$, being $v_{0G}^{\rho} < 0$ and $v_{0G}^{\sigma} > 0$.

4.3 – Simulation Results

This section is devoted to providing simulation results for the two novel approaches proposed in this chapter. Firstly, in subsection 4.3.1 a comparison between the SynRM traditional FOC and the FOC technique proposed in section 4.1 is performed using the novel SVM technique introduced in the previous section. Then, subsection 4.3.2 focus in analysing the CMV supplied to the SynRM and the converter input and output currents THDs with the proposed SVM approach in section 4.2 compared to the typical CMV reduction SVM technique proposed in [80], detailed in chapter 2.

The scenarios under study have been implemented in a Model-Based simulation, using MATLAB®/Simulink, where the OEW IMC supplies the SynRM characterized in chapter 3. A diagram of the proposed system is presented in Fig. 4.7, whose simulation model parameters are given in Table 4.1.

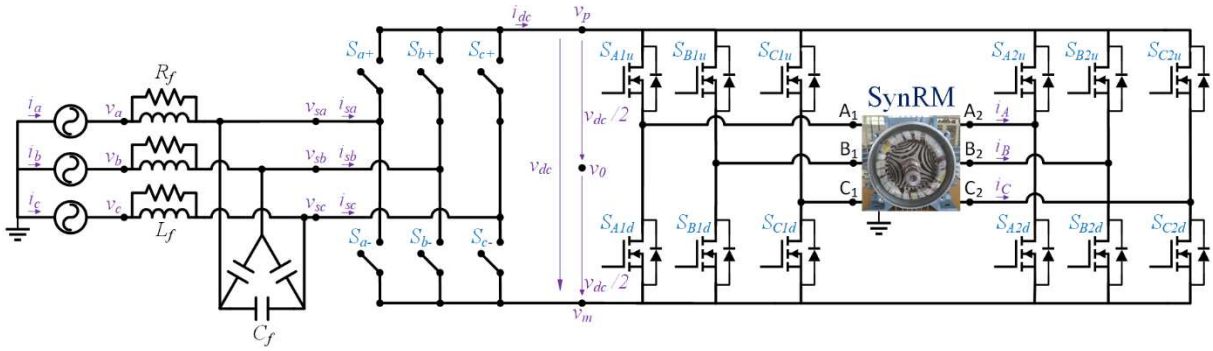


Fig. 4.7. Diagram of the proposed system: OEW SynRM drive based on IMC.

Table 4.1. Proposed Drive simulation model parameters.

Simulation	T_s	400 [ns]
SVM	f_{sw}	50 [kHz]
Grid	f_i	50 [Hz]
	$V_{ph\ rms}$	230 [V]
	L_{cc}	50 [µH]
Filter	C_f	2 [µF]
	L_f	2 [mH]
	R_f	10 [Ω]
Mechanical Parameters	J	0.015 [kg.m^2]
	k_D	0.0042 [Nm.s]
Proposed Controller	k_ω	500
	k_I	62500
	k_q	10000
	k_d	4000
RLS	T_{rls}	200 [µs]
	λ	0.98

4.3.1 – Proposed FOC for SynRM vs Traditional FOC

To assess the performance of the proposed FOC and to compare it with the typical FOC, three different operation scenarios are introduced. In the 1st scenario, the objective is to assess the steady state behaviour, while the 2nd and 3rd scenarios have been introduced to evaluate the proposed FOC performance in transient behaviour.

The corresponding operation details of each scenario are as follow:

1) Steady state operation for two different load scenarios: 5Nm and 19Nm mechanical load torques, while the SynRM is rotating at nominal speed (1500rpm).
2) The simulation starts with the machine at standstill. At t=0.1s the speed reference is ramped up to the SynRM nominal speed, then at t=0.5s the speed reference is ramped down to nominal speed in the reverse direction. The mechanical load torque (T_{load}) is maintained null in this scenario.
3) The simulation starts with the SynRM at the nominal speed and null mechanical load torque. At t=0.6s a step of 15Nm (approximately 80% of the nominal torque) is given in the mechanical load torque, then at t=0.9s another step is given to the load torque from 15Nm to -15Nm, and then again at t=1.2s the load torque is stepped from -15Nm to 15Nm.

Because a comparison between two FOC techniques is pretended, it is relevant to specify the gains of the traditional FOC, given in Table 4.2, but also how these gains were computed, which is detailed in Appendix A. Also, it is worth mentioning that the SVM strategy used throughout the three scenarios provided in this subsection is the technique proposed in section 4.2, with the maximum dc-link voltage option.

Table 4.2. Linear controllers gains of the simulated traditional FOC.

Speed PI	k_p	3.75
	k_i	469.5
***q* axis PI**	k_p	542
	k_i	7083
***d* axis PI**	k_p	999
	k_i	7083

1st scenario – Drive at Steady State

The steady state behaviour of both FOCs is now compared. Two different mechanical load conditions are evaluated while the SynRM is rotating at the nominal speed. The selected load torques were 5Nm (approximately 25% of the nominal torque) and 19Nm (nominal torque).

The 1st scenario simulation results featuring the proposed FOC technique are presented in Fig. 4.8, considering the two mechanical load cases, 5Nm in subfigures (a)-(d) and 19Nm in subfigures (e)-(h).

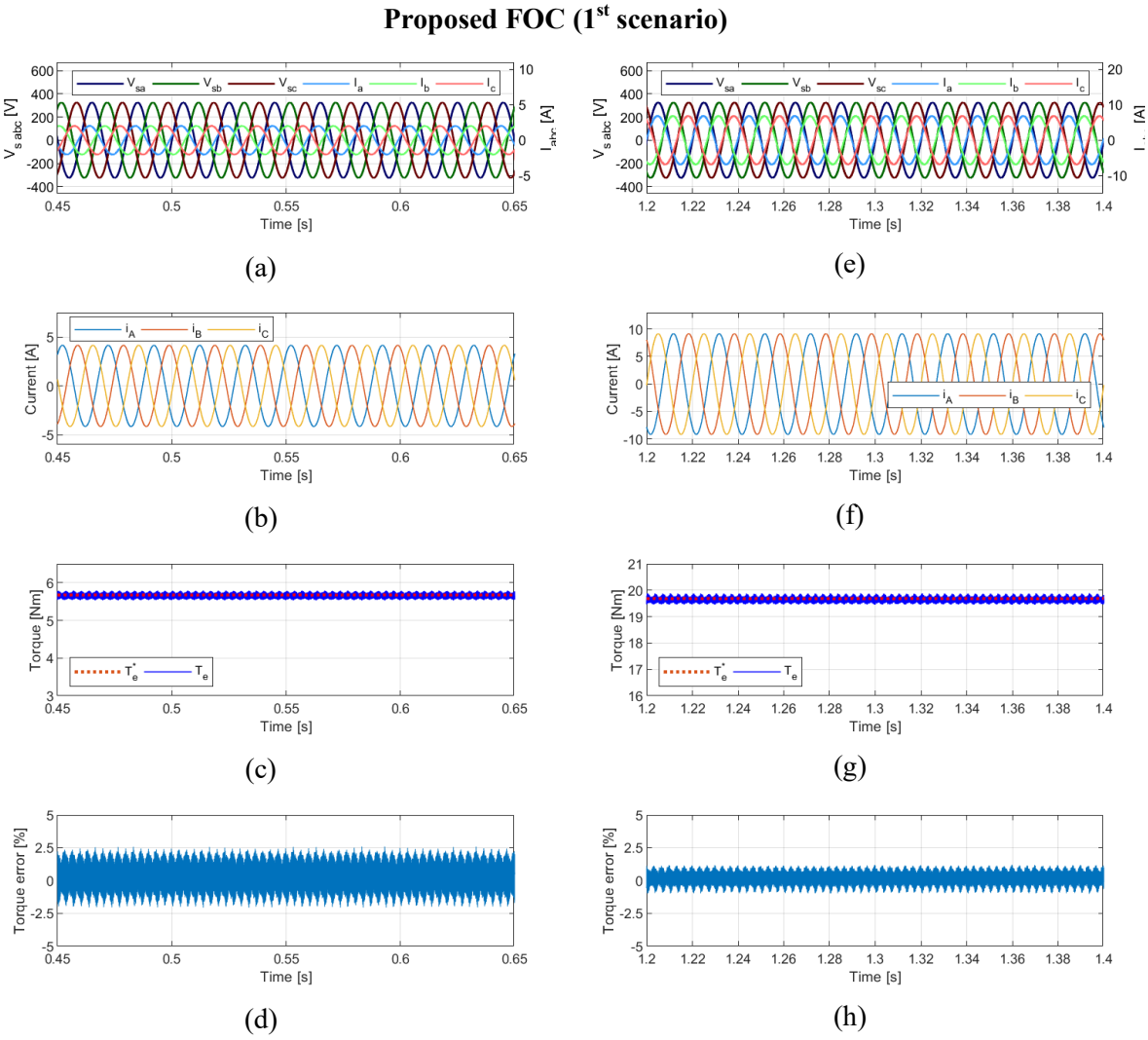


Fig. 4.8. 1st scenario simulation results of the proposed adaptive non-linear backstepping speed FOC in steady state with SynRM rotating at 1500rpm. T_{load}= 5Nm: (a) IMC input voltages and grid currents, (b) SynRM stator currents, (c) SynRM electromagnetic torque, (d) SynRM torque error in percentage. T_{load}= 19Nm: (e) IMC input voltages and currents, (f) SynRM stator currents, (g) SynRM electromagnetic torque, (h) SynRM torque error in percentage.

Whereas the simulation results featuring the typical FOC are presented in Fig. 4.9. By observing the simulation results obtained with both FOC methods, one can say that the drive steady state behaviour is undistinguishable. From the grid currents and IMC input voltages to the SynRM currents and its developed torque, the results are extremely similar. Also, both IMC input quantities as well as the SynRM currents show very little harmonic content, while the developed electromagnetic torque is smooth, even at the lower mechanical load scenario where the torque ripple represents around 2.5% of the reference torque. Thus, it is a very good indicator that the proposed FOC technique maintains the excellent steady state performance of traditional FOCs.

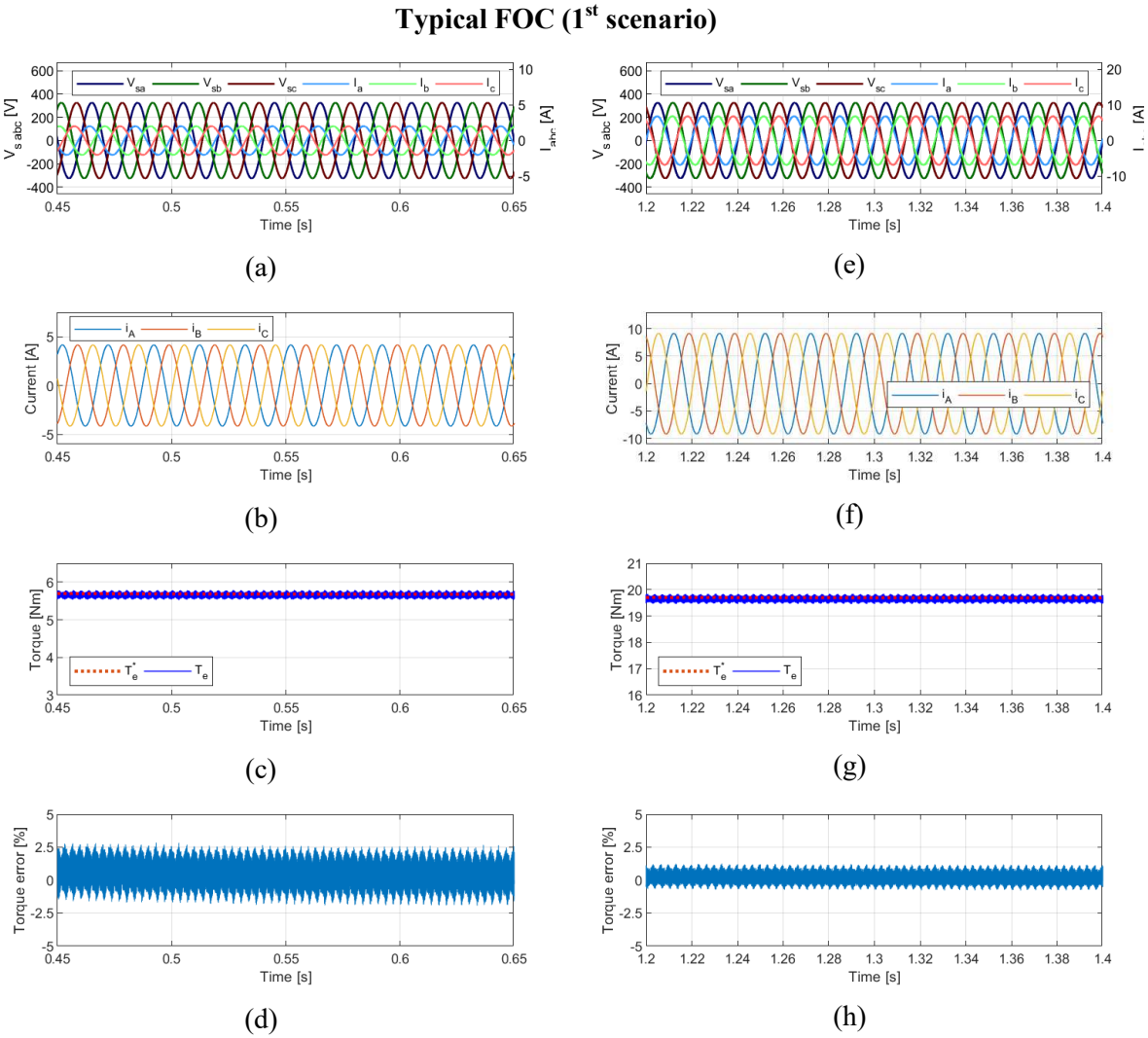


Fig. 4.9. 1st scenario simulation results of the typical FOC structure, using linear controllers in steady state with SynRM rotating at 1500rpm. T_{load}= 5Nm: (a) IMC input voltages and grid currents, (b) SynRM stator currents, (c) SynRM electromagnetic torque, (d) SynRM torque error in percentage. T_{load}= 19Nm: (e) IMC input voltages and currents, (f) SynRM stator currents, (g) SynRM electromagnetic torque, (h) SynRM torque error in percentage.

2nd scenario – Drive acceleration and deceleration

The drive capability to rapidly accelerate to the nominal speed and then decelerate and accelerate again to the nominal speed in the reverse direction, with no mechanical load, is evaluated in this operation scenario.

The drive performance with the proposed FOC strategy is presented in Fig. 4.10, showing the speed tracking performance in Fig. 4.10.(a), the electromagnetic torque and its reference in Fig. 4.10.(b), the SynRM currents in the *dqz* frame in Fig. 4.10.(c) and in the *abc* frame in Fig. 4.10.(d) and the RLS *d* axis and *q* axis inductance estimations in Fig. 4.10.(e). From these results, one may conclude the speed reference is accurately tracked, as are the references of torque and SynRM currents, which in addition present low ripple in the controlled quantities. It is also possible to observe that the RLS inductance estimations eventually converge to the true SynRM inductance values if the speed is not too low, showing limitations when the SynRM speed is extremely low, near the instant when the machine rotation direction is reversed. The inductance estimation capability is regained after the machine starts accelerating in the reverse direction. It is still important to mention that even during the instants where the inductance estimation is not completely accurate, the SynRM developed torque and currents tracked impeccably the reference quantities.

The results obtained using the traditional FOC technique for this scenario are presented in Fig. 4.11, where it is possible to observe that although the speed reference is followed, the SynRM speed shows a slight overshoot after the reference velocity stops varying. In terms of the SynRM developed torque and currents, the reference quantities are accurately tracked with low ripple in the controlled quantities.

By comparing the results obtained for this scenario with the two FOC techniques under study, it is possible to conclude that the proposed technique follows more accurately the speed reference imposed, as clearly shown in Fig. 4.12 where the velocity error, e_ω, is shown simultaneously for the two FOC approaches. Thus, for this scenario the proposed FOC outperforms the traditional PI based FOC.

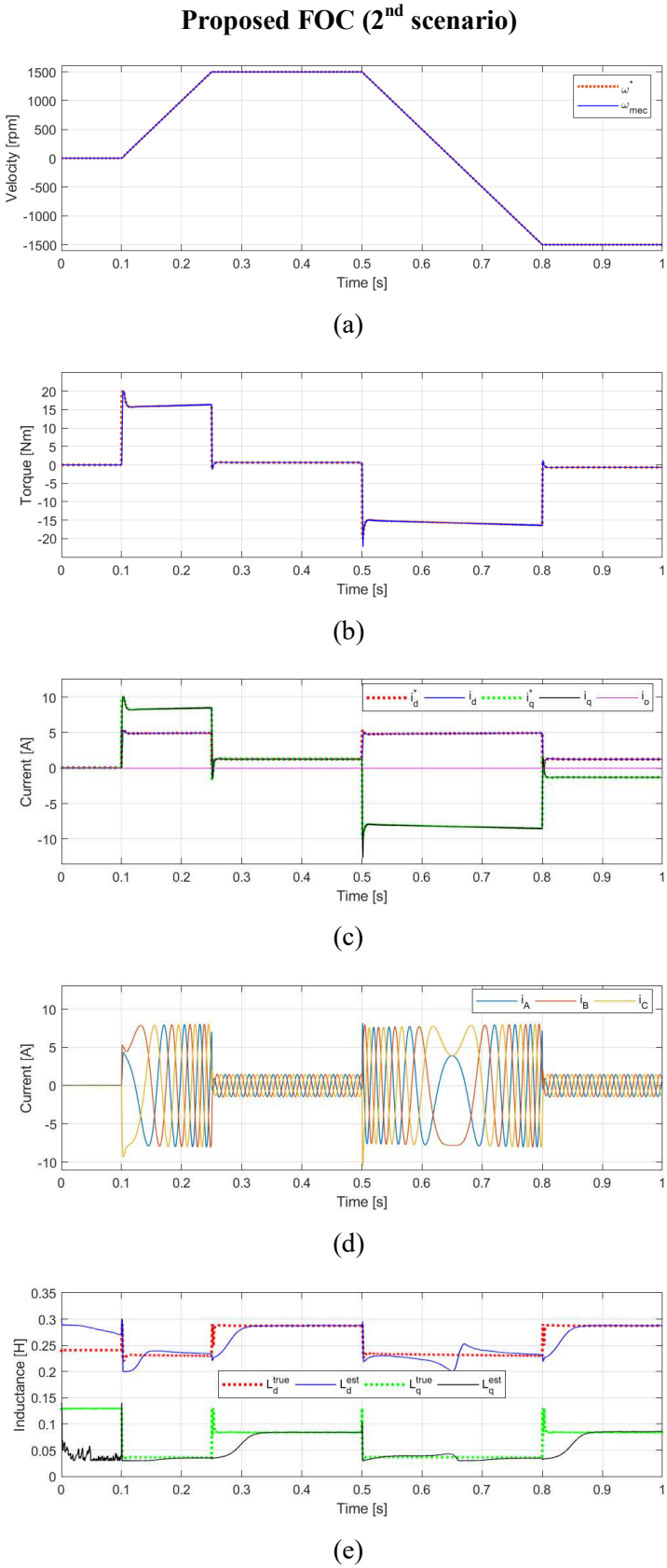


Fig. 4.10. 2nd scenario simulation results of the proposed adaptive non-linear backstepping speed FOC. (a) SynRM speed. (b) SynRM Torque. (c) SynRM currents in the *dqz* reference frame. (d) SynRM stator currents. (e) SynRM inductances and RLS estimations.

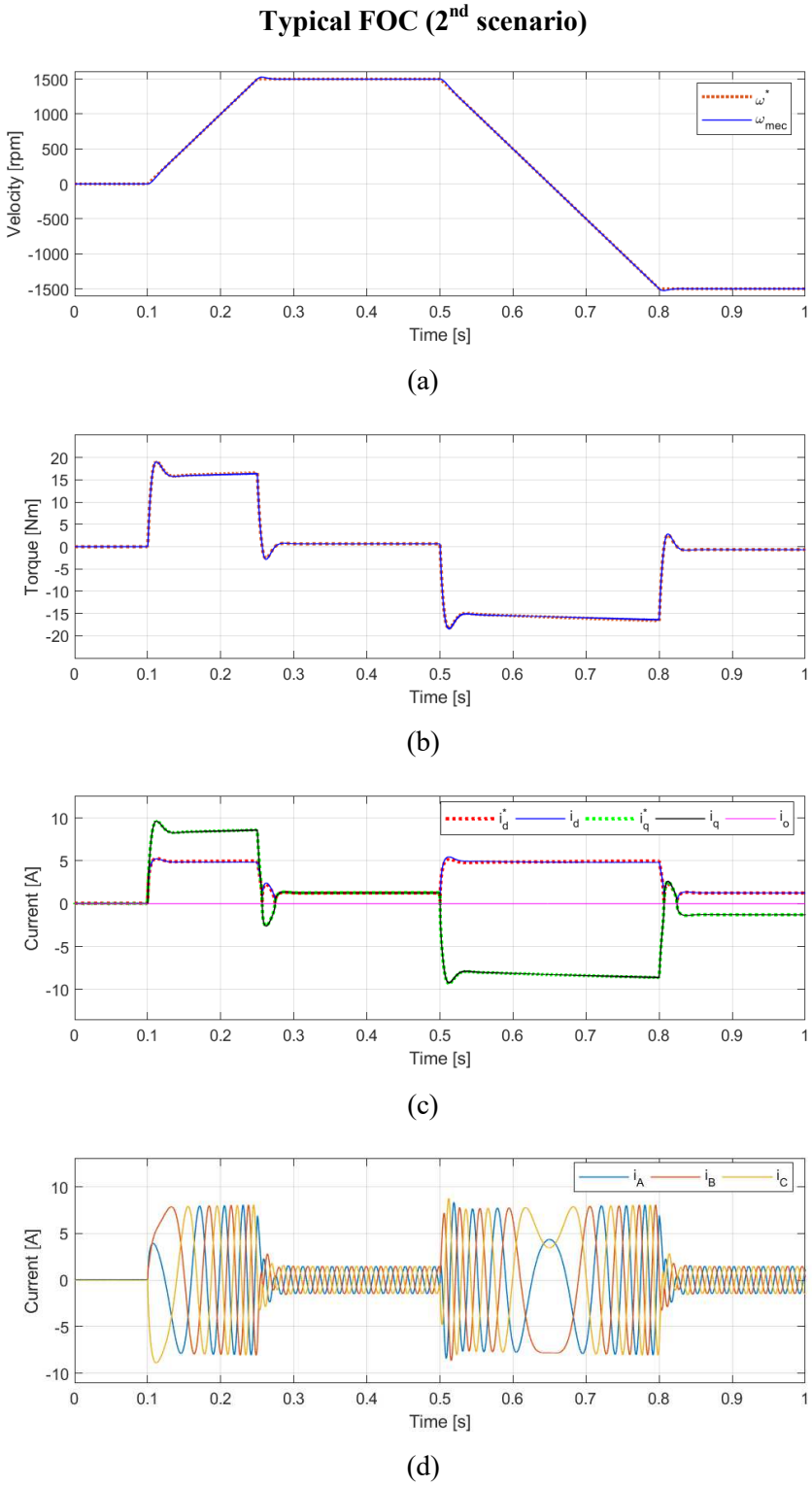


Fig. 4.11. 2nd scenario simulation results of the typical FOC structure, using linear controllers. (a) SynRM speed. (b) SynRM Torque. (c) SynRM currents in the *dqz* reference frame. (d) SynRM stator currents.

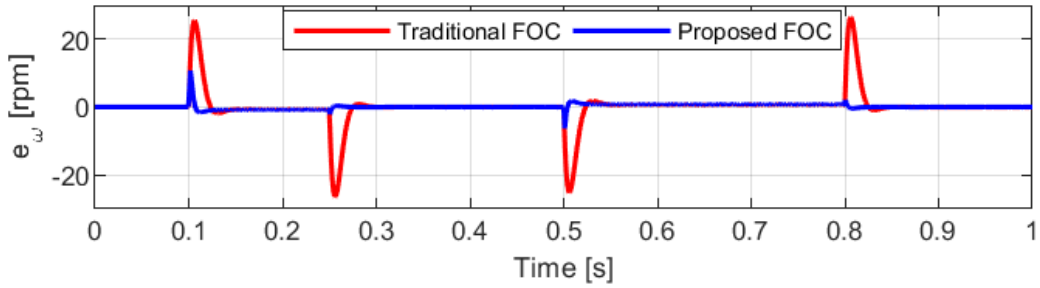


Fig. 4.12. 2nd scenario error in velocity for the two FOC approaches under study.

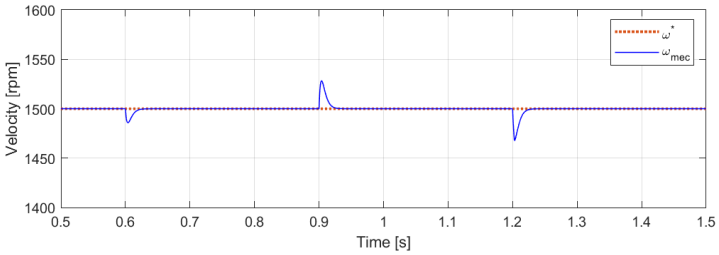
3rd scenario – Mechanical Load/Source torque step

In the 3rd scenario, the capability of handling significant and abrupt load torque variations while maintaining a fixed reference speed is analysed for the two FOC approaches under study.

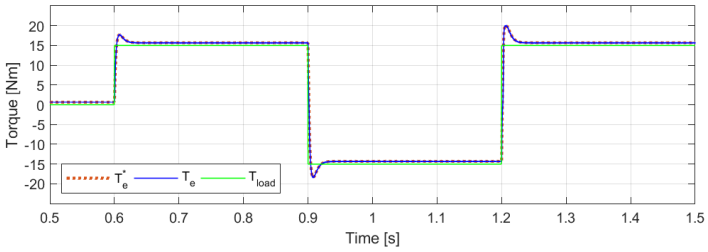
The simulation results of the proposed FOC for this scenario are presented in Fig. 4.13, where in Fig. 4.13.(a) the speed tracking performance is shown, then in Fig. 4.13.(b) the electromagnetic torque reference and its actual value is presented a long with the mechanical load torque. The SynRM currents in the *dqz* frame are given in Fig. 4.13.(c) and in the *abc* frame in Fig. 4.13.(d). Lastly, the RLS *d* and *q* axis inductances estimations are given in Fig. 4.13.(e). It is possible to observe that in the moment of the load torque step, the machine speed deviates from the reference speed as expected, but the drive can return to the reference speed by adjusting the developed electromagnetic torque. Also, just as in the previous scenario, the machine torque and currents present very little ripple, while the inductance estimations show improved performance when compared with the previous scenario because the SynRM is not operating in a low-speed region.

The performance of the traditional FOC technique for this scenario is provided in Fig. 4.14. Just as happened with the proposed controller, the SynRM velocity deviates from the reference value after the load torque steps, later returning to the reference value. The developed electromagnetic torque and currents follow the reference quantities with low ripple.

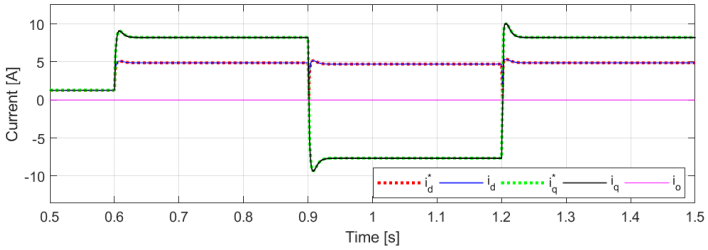
Proposed FOC (3rd scenario)



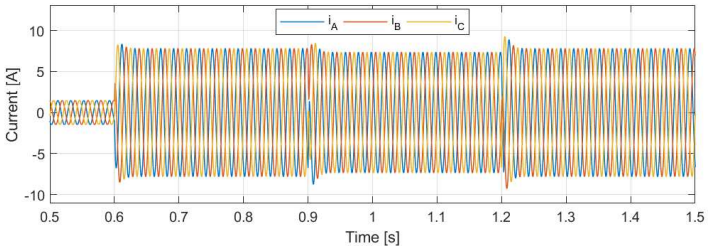
(a)



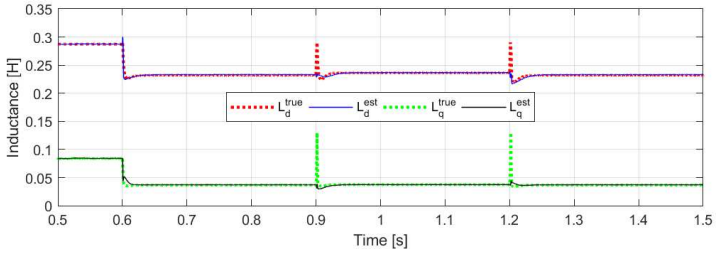
(b)



(c)



(d)



(e)

Fig. 4.13. 3rd scenario simulation results with the proposed adaptive non-linear backstepping speed FOC. (a) SynRM speed. (b) SynRM Torque. (c) SynRM currents in the *dqz* reference frame. (d) SynRM stator currents. (e) SynRM inductances and RLS estimations.

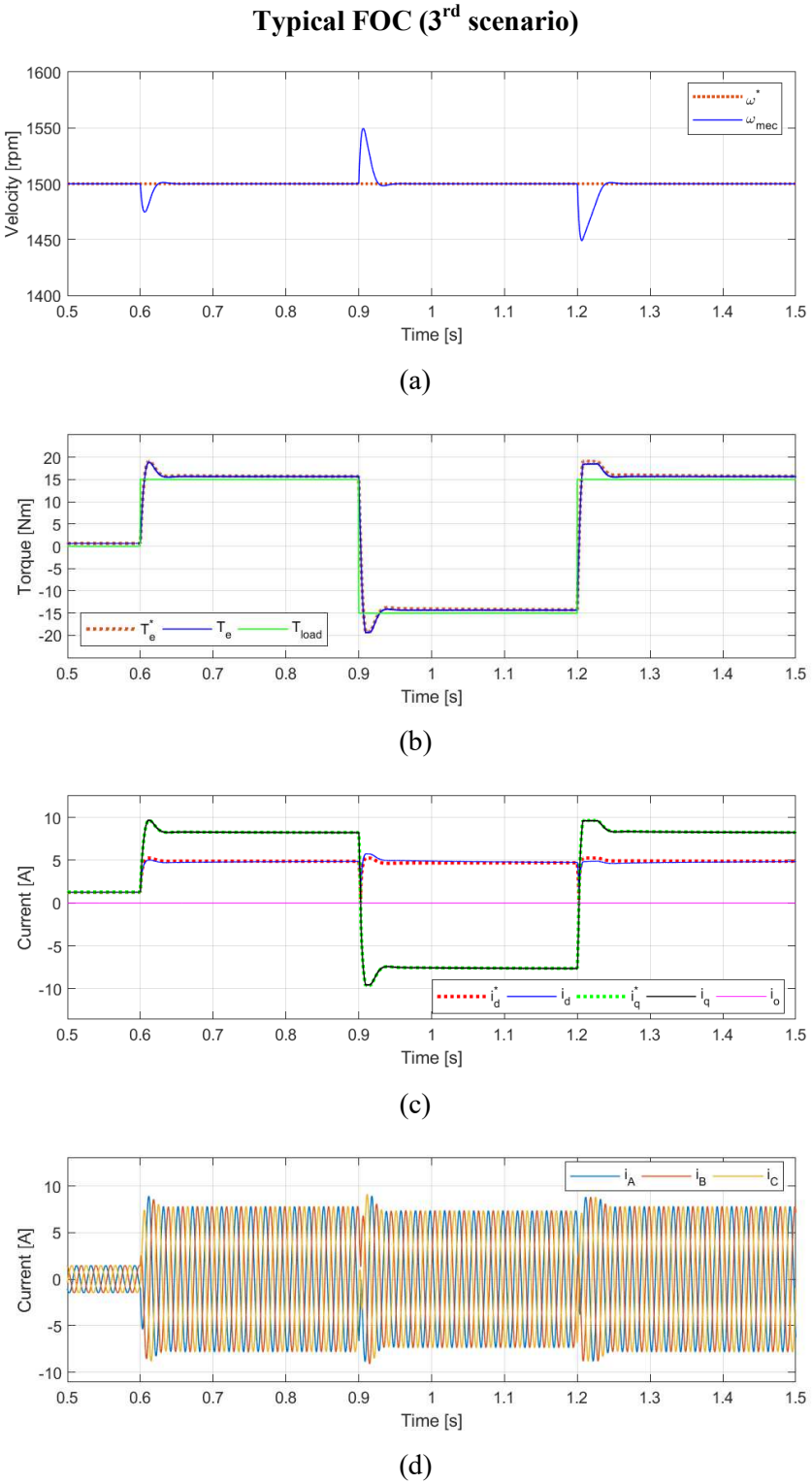


Fig. 4.14. 3rd scenario simulation results of the typical FOC structure, using linear controllers. (a) SynRM speed. (b) SynRM Torque. (c) SynRM currents in the *dqz* reference frame. (d) SynRM stator currents.

Still, the speed deviations of the traditional FOC are bigger (around 50% higher) than in the situation featuring the proposed FOC. This is detailed in Fig. 4.15, where e_ω is shown simultaneously for the two FOC techniques.

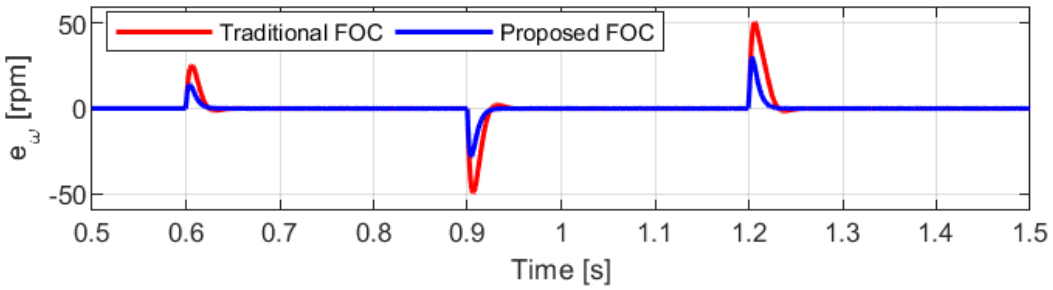


Fig. 4.15. 3rd scenario error in velocity for the two FOC approaches under study.

A detail on the drive torque response for both FOCs to the first load torque step (t=0.6s) of this operating scenario is presented in Fig. 4.16. The torque response with the proposed FOC had a rise time of 2.6 milliseconds while in the case of the traditional FOC it registered 4.5 milliseconds. In terms of overshoot, the traditional FOC also shown a higher overshoot of 21.2% while the proposed technique registered 13.8%.

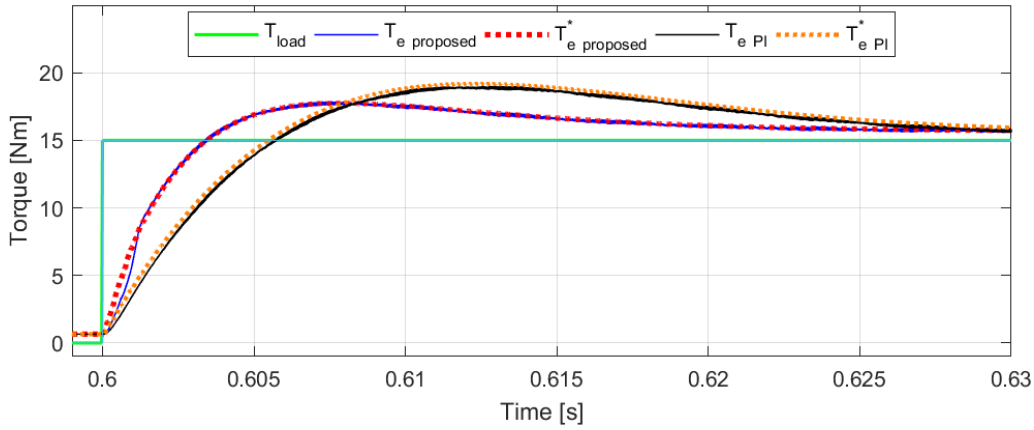


Fig. 4.16. Zoom of the torque waveforms of the 3rd scenario for both FOCs analysed.

Thus, once again the proposed FOC outperforms the traditional PI based FOC technique for this operation scenario.

Conclusion

The simulation results of the three analysed SynRM operation scenarios show that the modifications proposed to the typical FOC algorithm, allowed an improvement in the drive dynamic response by significantly improving the system response to load disturbances while slightly improving the speed tracking performance. The drive dynamic response is enhanced without damaging the drive steady state performance, which is FOC main advantage over other control strategies.

4.3.2 – CMV evaluation of the proposed SVM strategy

The previous subsection focused on the performance comparison between the proposed FOC for the SynRM and the traditional FOC, while using the proposed SVM strategy but didn't go into the details related to the IMC operation for that SVM technique. This subsection focus in analysing the difference between the SVM method proposed in section 4.2 and the SVM method described in subsection 2.3.2 whose objective is to reduce CMV at machine terminals.

The SVM methods are analysed in terms of the quality of both the input and output waveforms, but also in terms of the CMV supplied to the machine terminals. This is performed for both IMC input stage modulation methods, firstly using the maximum dc-link voltage modulation method, and then secondly using the reduced dc-link voltage modulation method. To allow comparison of the different SVM techniques, the analysed scenarios are taken under the same SynRM operation point, this being the SynRM rotating at 1250rpm with a load torque of 15Nm.

Input stage using the maximum dc-link voltage modulation

The results obtained with the SVM technique proposed in section 4.2 are presented in Fig. 4.17 for a reference null IMC input current-to-voltage displacement angle, $\Phi_i=0$. Fig. 4.17 shows the grid currents and IMC input voltages in subfigure (a), then in subfigure (b) the SynRM currents in the *abc* frame, in subfigure (c) the soft dc-link quantities are shown and in subfigure (d) the SynRM phase 'A' winding voltage and current is given. Still in Fig. 4.17, the CMV and its components are shown in subfigure (e), zoomed for better detail in subfigure (f). This exact same operating scenario and plot structure is shown in Fig. 4.18 for the SVM technique featuring only DVSI Group I switching states. By comparing Fig. 4.17 with Fig. 4.18, it is clear that the grid currents harmonic distortion is small for both cases, while the SynRM currents possess much higher harmonic content in Fig. 4.18. This was already observed in the results

presented in section 2.5.2, but is intensified in this scenario due to the lower impedance of the SynRM in the *z* axis, resulting in significantly higher ZSCs for the situation with the SVM method using DVSI Group I switching states.

In terms of CMV and its components, it is possible to conclude that the input stage contribution to CMV (v_{0G}) is the same for both SVM methods, being unaffected under the proposed SVM strategy. On the other hand, the peak CMV is clearly reduced with the proposed SVM technique by selecting the polarity of v_{cm0} to be opposite to the signal of v_{0G}.

Let us now consider a case with non-null reference IMC input current-to-voltage displacement angle, $\Phi_i=\pi/6$. Simulation results for the proposed SVM technique are given in Fig. 4.19 while the results for the SVM strategy with DVSI Group I vectors are given in Fig. 4.21.

It is possible to observe once again that the SynRM currents show extremely higher THD when the DVSI Group I vectors are used, while the input currents appear to possess low THD.

In terms of CMV, once again the proposed SVM method allows a reduction in the instantaneous CMV at the machine terminals.

Another interesting output to take from the results provided through Fig. 4.17 - Fig. 4.20 is on the polarity of the IMC input stage contribution to the CMV, v_{0G}, within a switching period. When null input current-to-voltage displacement angle is selected, the polarities of both input stage switching states are always the same ($sign(v_{0G}^{\rho}) = sign(v_{0G}^{\sigma})$). Only when a non-null displacement angle is set, situations where $sign(v_{0G}^{\rho}) \neq sign(v_{0G}^{\sigma})$ appear. This means that for null input current-to-voltage displacement angle the proposed SVM strategy always operates in the conditions defined in Fig. 4.3, allowing the bidirectional switches to switch without any special multistep commutation logic. Even though it is a quite limiting operating condition, specially by not allowing any kind of input power factor regulation other than the unitary power factor on the drive side added to a capacitive filter component, it is a positive outcome that may be interesting specially for low power industrial variable speed drives.

As predicted in section 4.2, the proposed SVM strategy maintained some of the properties offered from the traditional modulation technique featuring DVSI Group II presented in section 2.3.1, such as better quality of input and output waveforms while decreasing the peak CMV. Being the loss of capability to switch the input stage bidirectional switches without the need of multistep commutation logics in situations where $sign(v_{0G}^{\rho}) \neq sign(v_{0G}^{\sigma})$ the compromise required to achieve peak CMV reduction.

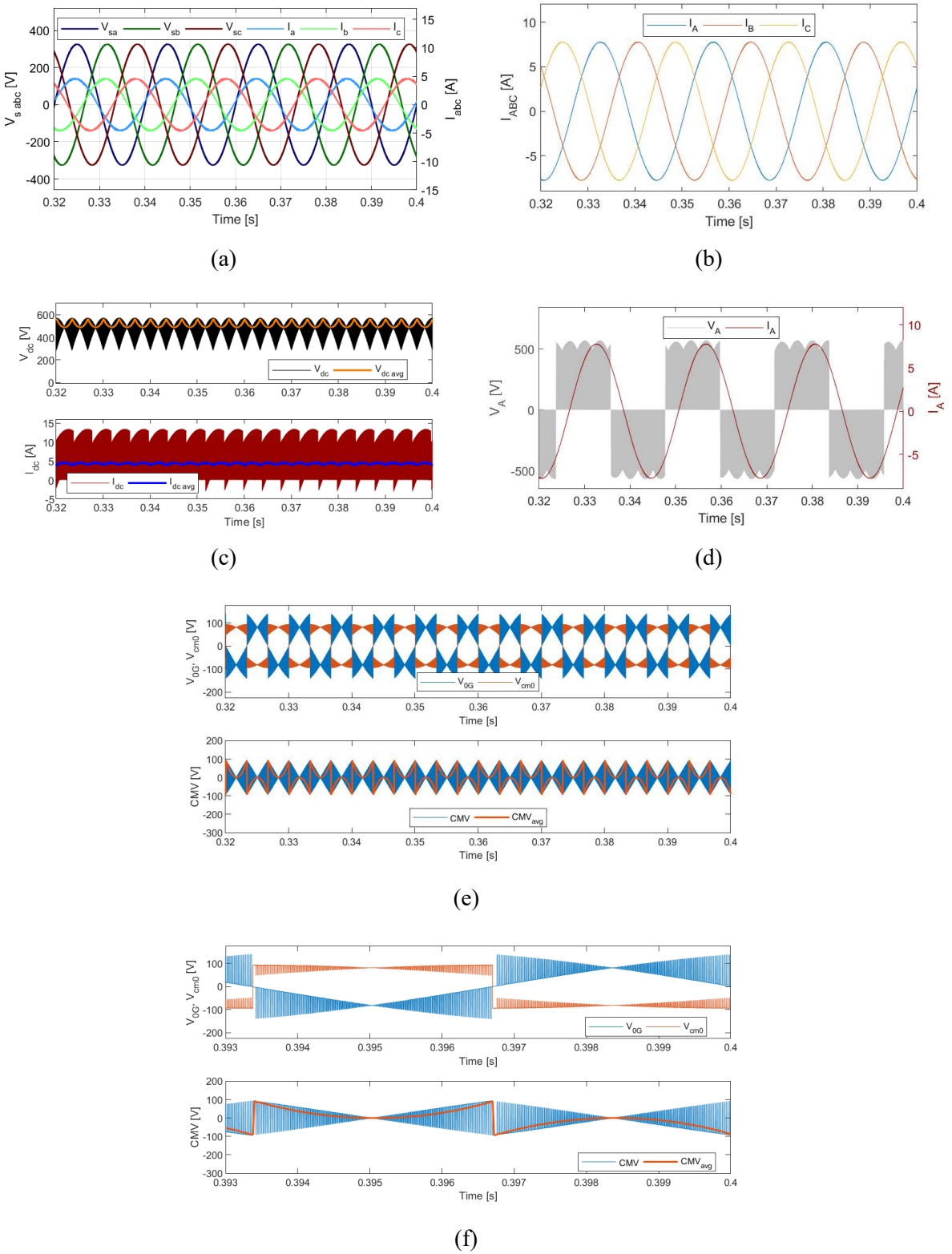


Fig. 4.17. Drive simulation results using the proposed SVM technique presented in section 4.2 featuring maximum dc-link voltage, for a steady state scenario with SynRM rotating at 1250rpm, 15Nm of load torque and input current-to-voltage displacement angle $\Phi_i=0$. (a) grid currents and IMC input voltages, (b) SynRM currents, (c) dc-link voltage and current, (d) current and voltage of SynRM phase A, (e) CMV and its components, (f) detail of CMV.

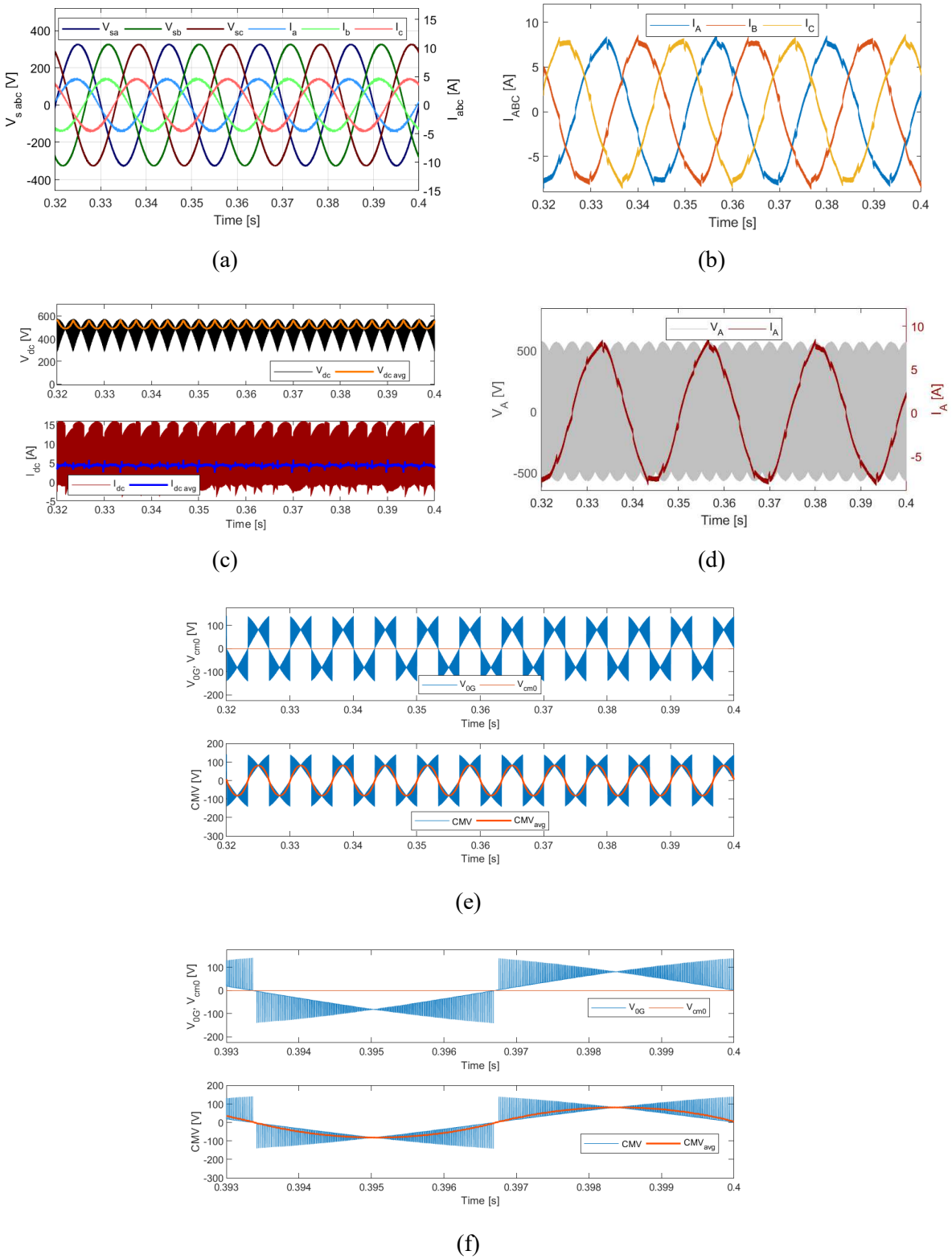


Fig. 4.18. Drive simulation results with the SVM technique that uses only DVSI Group I vectors featuring maximum dc-link voltage. Steady state scenario with SynRM rotating at 1250rpm, 15Nm of load torque and input current-to-voltage displacement angle $\Phi_i=0$. (a) grid currents and IMC input voltages, (b) SynRM currents, (c) dc-link voltage and current, (d) current and voltage of SynRM phase A, (e) CMV and its components, (f) detail of CMV.

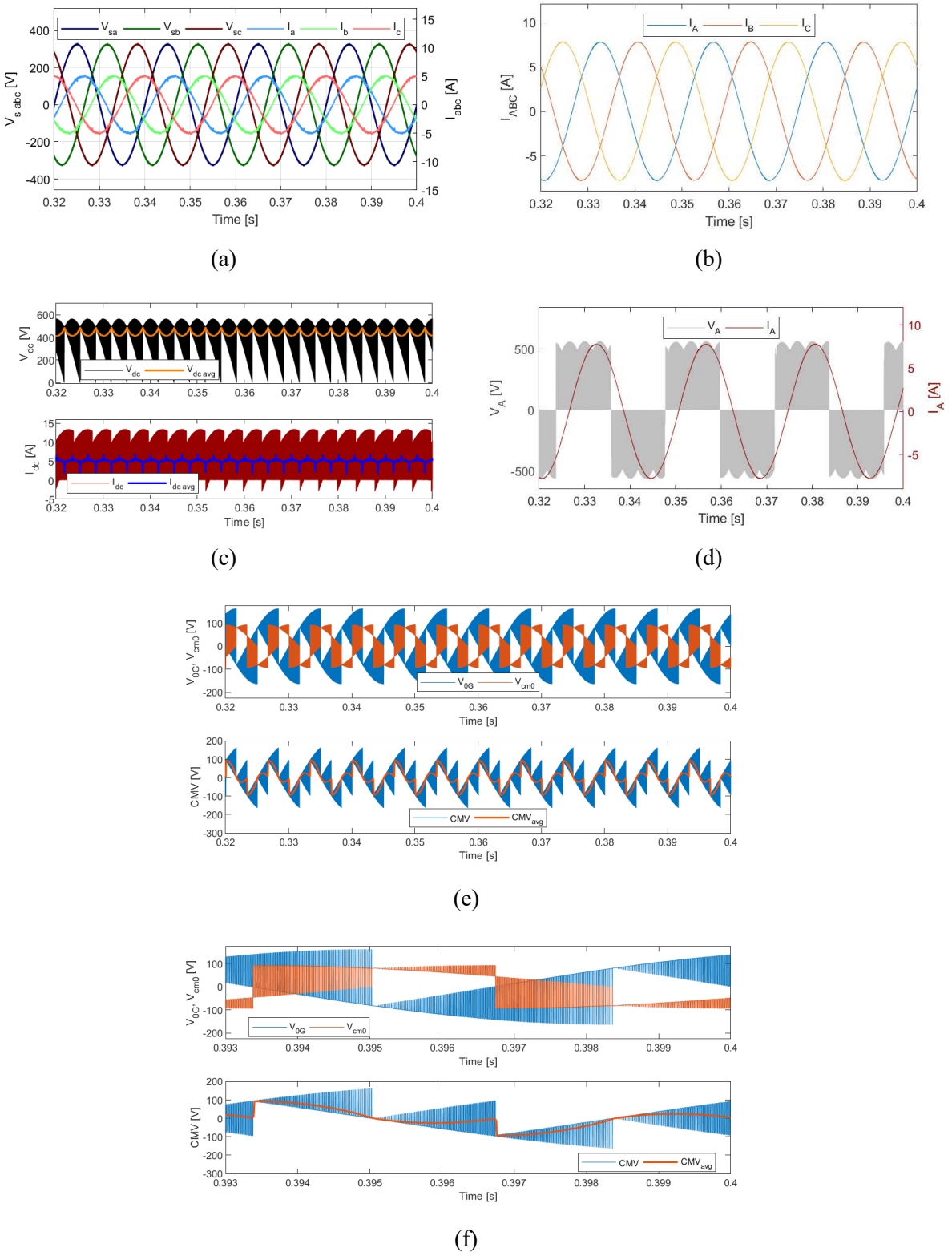


Fig. 4.19. Proposed Drive simulation results, using the SVM technique presented in section 4.2 featuring maximum dc-link voltage, for a steady state scenario with SynRM rotating at 1250rpm, 15Nm of load torque and input current-to-voltage displacement angle $\Phi_i = \pi/6$. (a) grid currents and IMC input voltages, (b) SynRM currents, (c) dc-link voltage and current, (d) current and voltage of SynRM phase A, (e) CMV and its components, (f) detail of CMV.

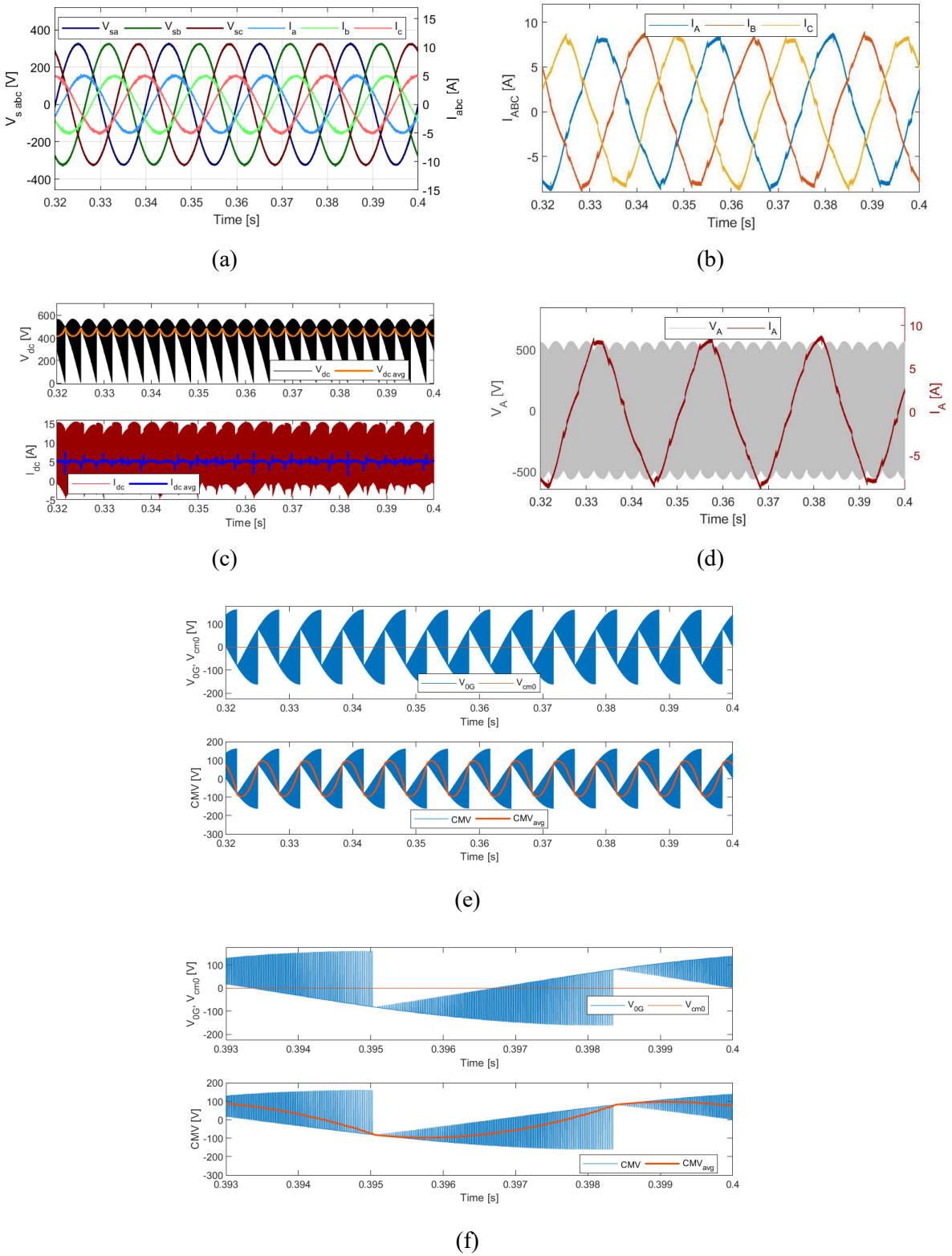


Fig. 4.20. Drive simulation results with the SVM technique that uses only DVSI Group I vectors featuring maximum dc-link voltage. Steady state scenario with SynRM rotating at 1250rpm, 15Nm of load torque and input current-to-voltage displacement angle $\Phi_i = \pi/6$. (a) grid currents and IMC input voltages, (b) SynRM currents, (c) dc-link voltage and current, (d) current and voltage of SynRM phase A, (e) CMV and its components, (f) detail of CMV.

Input stage using the reduced dc-link voltage modulation

The exact same SynRM operating scenario (1250rpm with 15Nm of load torque), is considered here to discuss the simulation results of the SVM techniques under study, featuring the reduced dc-link voltage strategy.

The results obtained with the SVM technique proposed in section 4.2 are presented in Fig. 4.21 for a reference null IMC input current-to-voltage displacement angle, $\Phi_i=0$. Fig. 4.21 shows the grid currents and IMC input voltages in subfigure (a), then in subfigure (b) the SynRM currents in the *abc* frame, in subfigure (c) the soft dc-link quantities are shown, and in subfigure (d) the SynRM phase 'A' winding voltage and current is given. Still in Fig. 4.21, the CMV and its components are presented in subfigure (e), zoomed for better detail in subfigure (f).

The simulation results for the SVM technique featuring only DVSI Group I switching states are shown in Fig. 4.22 with the same plot structure.

Comparing Fig. 4.21 with Fig. 4.22, similarly to the previously analysed results for the maximum dc-link voltage strategy, it is clear that the SynRM currents have much higher harmonic content with the SVM technique featuring only DVSI Group I switching states, while the grid currents are quite similar under both SVM techniques.

In terms of CMV components, the input stage contribution with the reduced dc-link voltage strategy, v_{0G}, possess opposite polarities during the switching period. Meaning that the situation where $sign(v_{0G}^{\rho}) \neq sign(v_{0G}^{\sigma})$, happens in every switching period, requiring the usage of special multistep logic for the commutation of bidirectional switches as discussed in section 4.2. Again, by selecting the polarity of v_{cm0} to be opposite to the signal of v_{0G}, the proposed SVM technique allowed a reduction in the peak CMV at the machine terminals.

Also, a mention should be given to the periodic spikes that are visible in the soft dc-link quantities of both Fig. 4.21 and Fig. 4.22, near the IMC input zone transitions. In these instants, the CSR input voltage is not enough to be safely applied in the dc-link (because the voltage ripple in the input filter capacitors may result in short circuiting the soft dc-link), requiring the input stage modulation strategy to be changed to the maximum dc-link voltage strategy until there is enough voltage, resulting in the spikes that appear not only in the dc-link average voltage and current but also on the CMV waveforms.

To demonstrate that the reduced dc-link voltage strategy allows the adjustment of current-to-voltage displacement angle, Fig. 4.23 presents results for the proposed SVM technique with $\Phi_i=\pi/12$, being the results similar to Fig. 4.21 except for the input power factor.

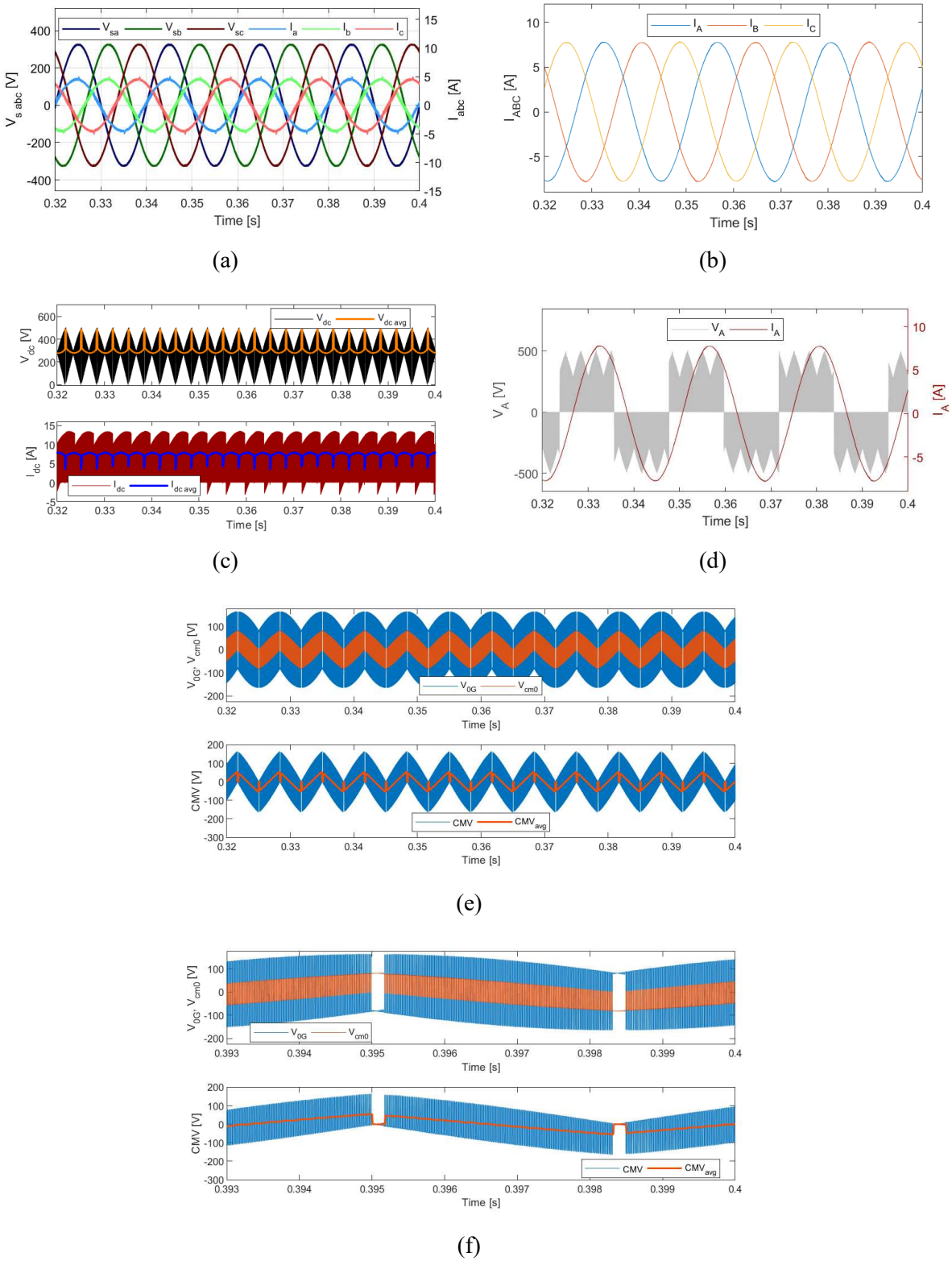


Fig. 4.21. Proposed Drive simulation results, using the SVM technique presented in section 4.2 featuring reduced dc-link voltage, for a steady state scenario with SynRM rotating at 1250rpm, 15Nm of load torque and input current-to-voltage displacement angle $\Phi_i=0$. (a) grid currents and IMC input voltages, (b) SynRM currents, (c) dc-link voltage and current, (d) current and voltage of SynRM phase A, (e) CMV and its components, (f) detail of CMV.

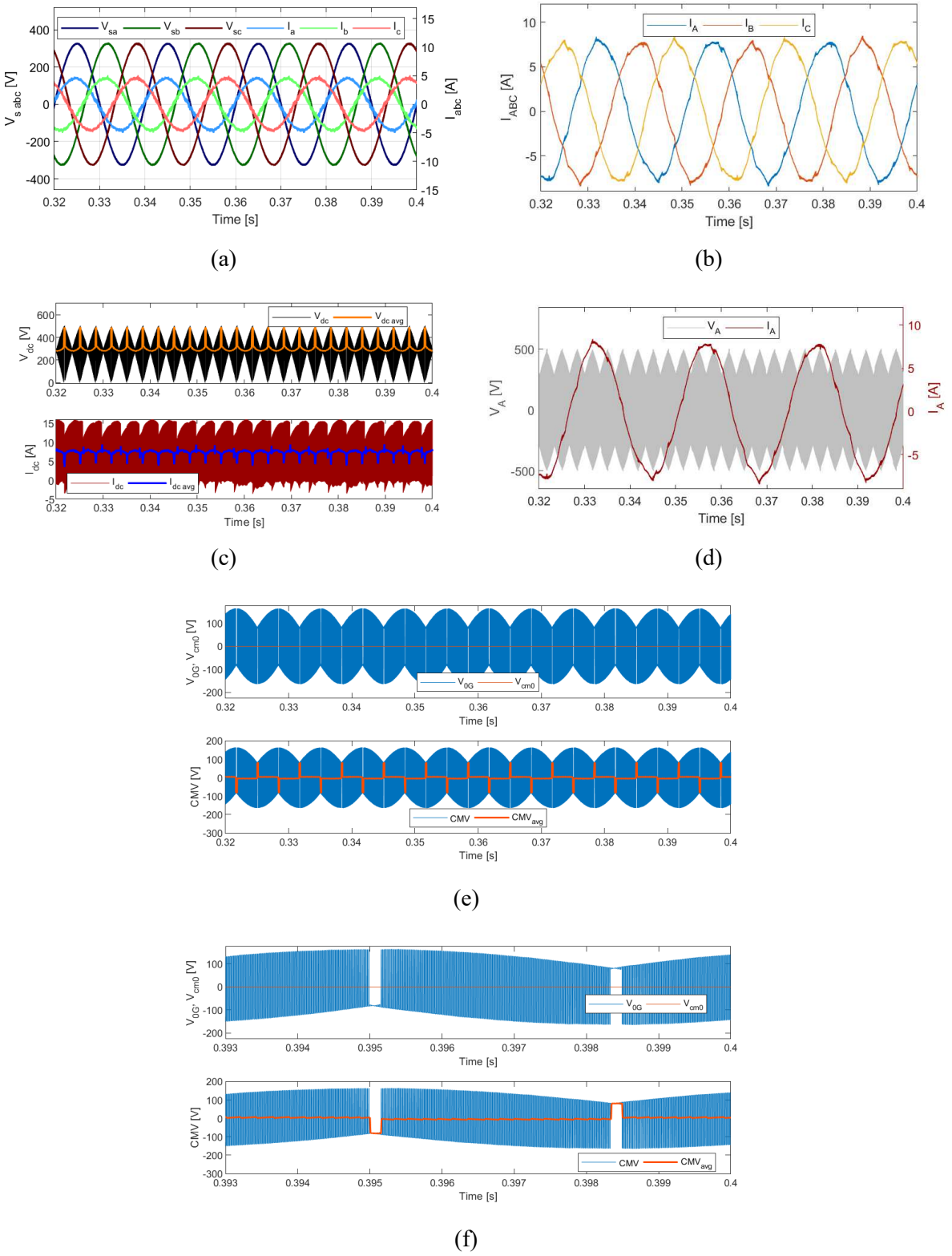


Fig. 4.22. Drive simulation results with the SVM technique that uses only DVSI Group I vectors featuring reduced dc-link voltage. Steady state scenario with SynRM rotating at 1250rpm, 15Nm of load torque and input current-to-voltage displacement angle $\Phi_i=0$. (a) grid currents and IMC input voltages, (b) SynRM currents, (c) dc-link voltage and current, (d) current and voltage of SynRM phase A, (e) CMV and its components, (f) detail of CMV.

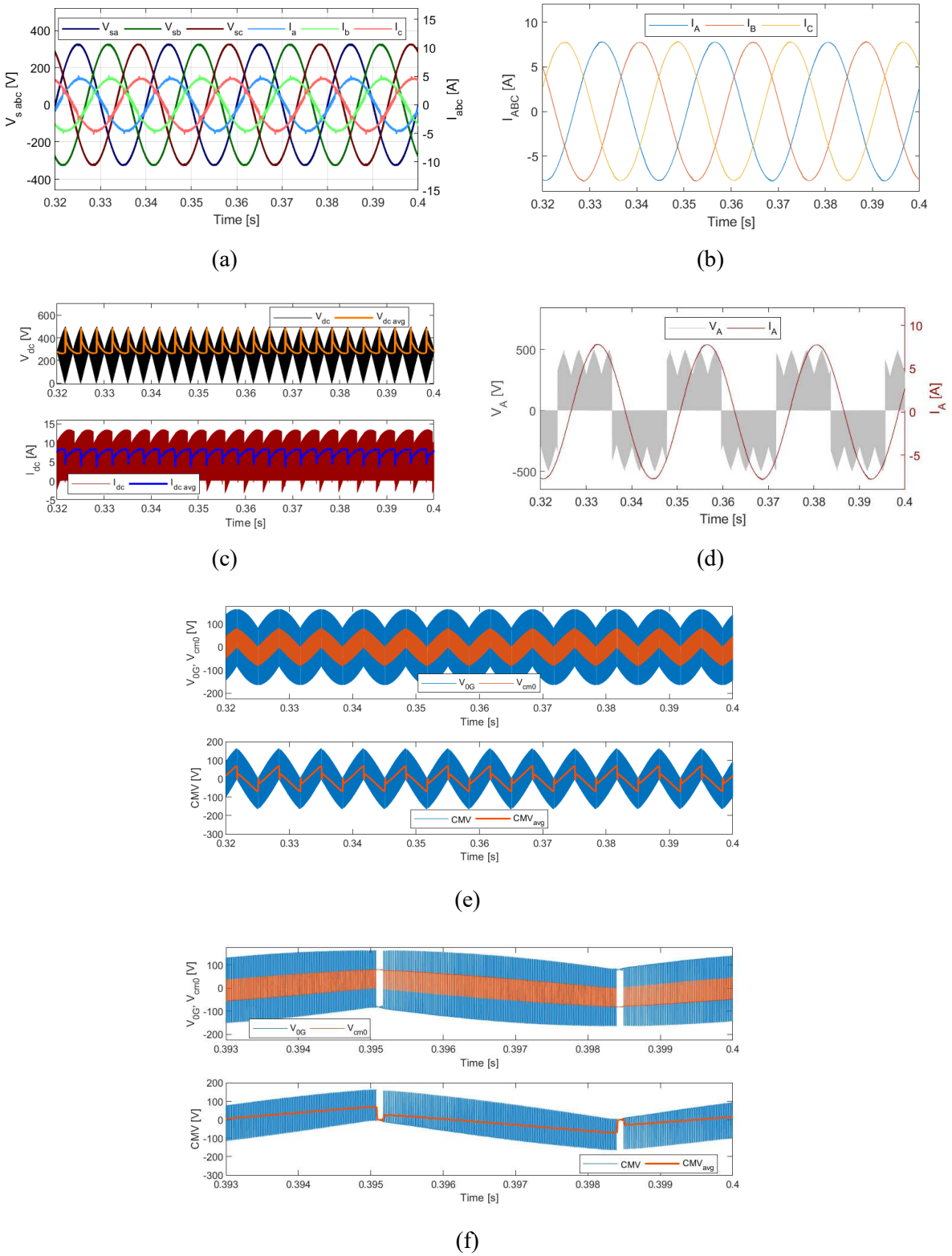
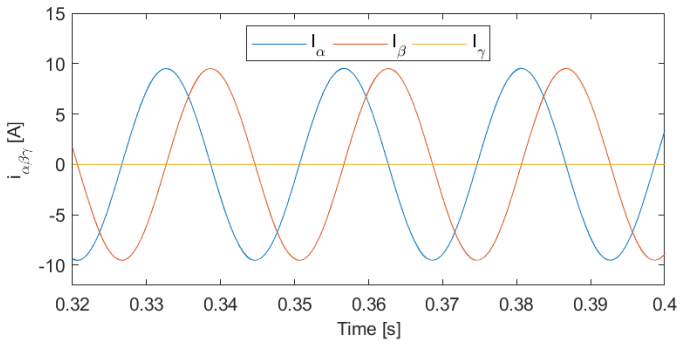


Fig. 4.23. Proposed Drive simulation results, using the SVM technique presented in section 4.2 featuring reduced dc-link voltage, for a steady state scenario with SynRM rotating at 1250rpm, 15Nm of load torque and input current-to-voltage displacement angle $\Phi_i=\pi/12$. (a) grid currents and IMC input voltages, (b) SynRM currents, (c) dc-link voltage and current, (d) current and voltage of SynRM phase A, (e) CMV and its components, (f) detail of CMV.

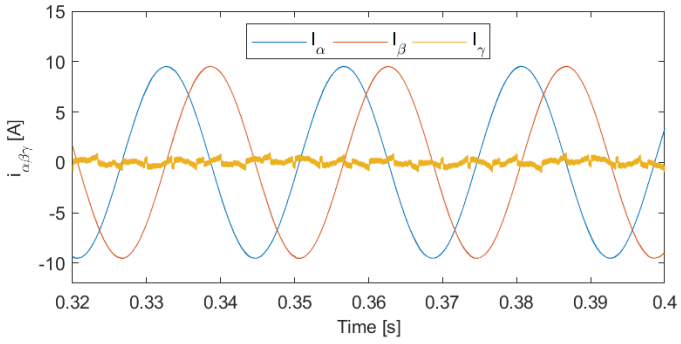
SynRM currents

Regarding the output currents quality, it was observed that the SVM technique featuring only DVSI Group I switching states produces currents with much higher harmonic content than the proposed SVM technique. Although it was already noticed in the simulation results for the RL load presented in subsection 2.5.2 that the output currents THD for the SVM technique featuring DVSI Group I vectors were higher than for the SVM technique featuring DVSI Group II vectors, the difference was nearly as big as the observed in the simulation results presented in this chapter. This happens due to the SynRM zero sequence impedance being much lower than the simulated RL load zero sequence impedance, resulting in higher zero sequence currents.

To illustrate this, the SynRM currents in the $\alpha\beta\gamma$ stationary reference frame are presented in Fig. 4.24 for both SVM strategies in the same exact operating condition that was shown in Fig. 4.17 and Fig. 4.18. The proposed SVM technique SynRM currents are shown in Fig. 4.24.(a) while the results for the SVM technique featuring only DVSI Group I switching states are shown in Fig. 4.24.(b).



(a)



(b)

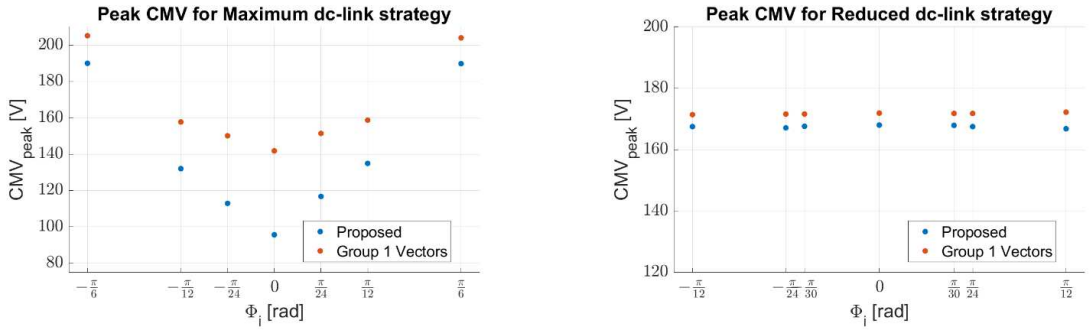
Fig. 4.24. SynRM currents in the $\alpha\beta\gamma$ stationary reference frame for the drive operating in steady state at 1250rpm, 15Nm of load torque, input current-to-voltage displacement angle $\Phi_i=0$, and input stage maximum dc-link voltage modulation strategy. (a) Proposed SVM Technique, (b) SVM technique featuring only DVSI Group I vectors.

It is clear that i_α and i_β are almost identical for both SVM techniques, with the big difference lying in i_γ. Thus, it is demonstrated that the reason for the proposed SVM technique achieving improved SynRM currents lies on the absence of zero-sequence currents.

Conclusion

As predicted in section 4.2, the proposed SVM strategy maintained some of the properties offered from the traditional modulation technique featuring DVSI Group II presented in section 2.3.1, such as better quality of input and output waveforms while decreasing the peak CMV. Being the loss of capability to switch the input stage bidirectional switches without the need of multistep commutation logic in situations where $sign(v_{0G}^{\rho}) \neq sign(v_{0G}^{\sigma})$ the compromise required to achieve peak CMV reduction.

A comparison of the peak values of CMV for the proposed SVM strategy and the technique only featuring DVSI Group I switching states is given in Fig. 4.25.(a) for the input stage modulation with maximum dc-link voltage and in Fig. 4.25(b) for the reduced dc-link voltage strategy. One may conclude that the effectiveness of the proposed SVM technique to reduce CMV differs depending on the input stage modulation strategy and on the input displacement angle reference. When the input stage is modulated for maximum dc-link voltage, the CMV peak value reduction is significant for input displacement angles closer to zero, achieving its maximum reduction of approximately 45V when $\Phi_i=0$, losing impact with the increase of Φ_i amplitude. On the other hand, when the input stage is modulated for reduced dc-link voltage, although there is some reduction, the CMV peak value reduction is much smaller than in the previous case.



(a) (b)

Fig. 4.25. Peak CMV at the SynRM terminals. Comparison between the proposed SVM strategy and the SVM strategy featuring DVSI Group 1 vectors. (a) For the input stage modulation strategy with Maximum dc-link voltage. (b) For the input stage modulation strategy with Reduced dc-link voltage.

It is worth noting that the input stage modulation strategy for maximum dc-link voltages results in a significantly lower CMV peak value than the input stage modulation strategy for reduced dc-link voltages.

CHAPTER 5

EXPERIMENTAL VALIDATION

5.1 – Laboratorial Prototype Implementation

In chapter 4 several simulation results of both the proposed SVM strategy and the non-linear modified FOC were presented. The next step is to implement the proposed techniques in a laboratory prototype to validate the proposed approaches.

The built laboratory prototype has been divided into 5 modules:

- Mechanical Test bench;
- Signal Acquisition board;
- Dual Voltage Source Inverter (Output Stage);
- Current Source Rectifier (Input Stage);
- Control Board.

A brief description to each of the laboratory prototype modules is provided bellow.

5.1.1 – Mechanical Test bench

The mechanical test bench consists of two electrical machines (the SynRM under test and a load machine) coupled by a torque sensor. The SynRM under test is a 3kW SynRM from ABB, that was characterized in chapter 3 with its main catalogue characteristics stated in Table 3.1. The load machine is a 3kW induction machine which is supplied by an ACS600 DTC controller both from ABB. The position sensor is a magnetic actuated encoder with both absolute and incremental functions, model RM44SI0010B20F2E10 from RLS. The torque sensor is the model 8645-5017,5 from burster. However, due to second order oscillations, it is not used within any control loop, being its only purpose the torque waveform visualization. A picture of the test bench is given in Fig. 5.1.

It is relevant to refer that the ACS600 drive used to control the induction machine is not bidirectional in terms of power flow. Thus, the power flow must be from the grid to the ACS600 drive.

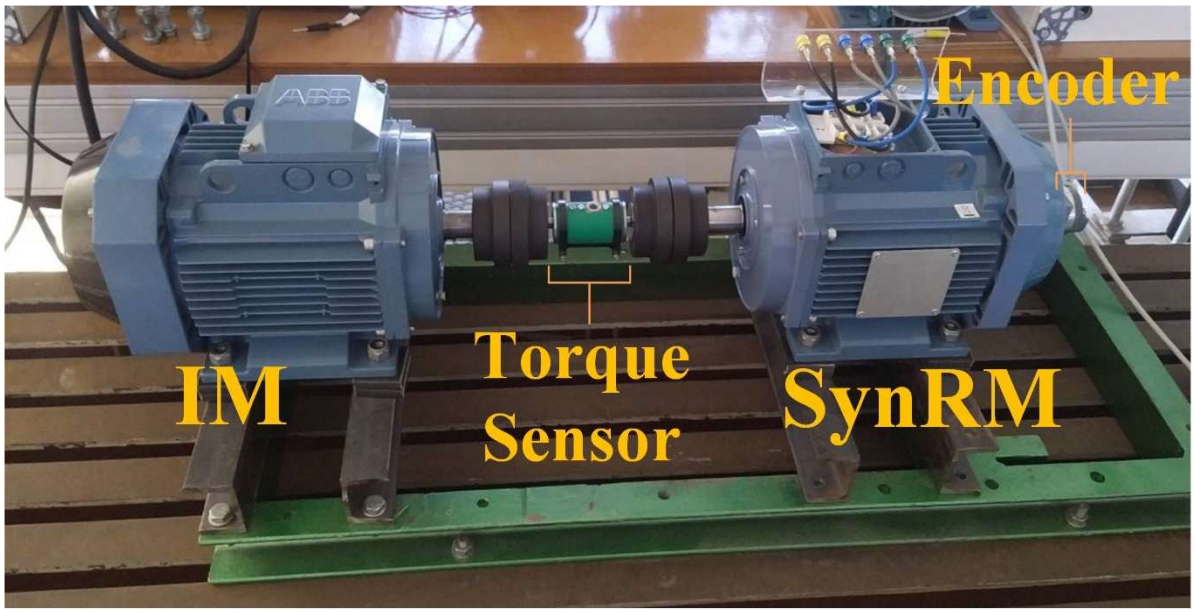
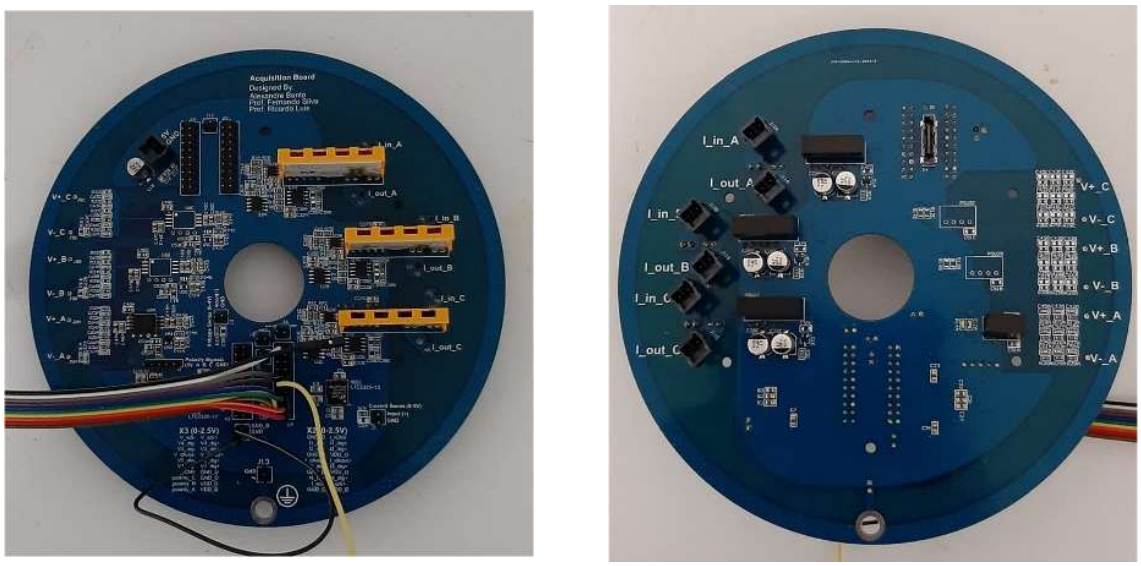


Fig. 5.1. Mechanical test bench composed by an induction machine, a torque sensor and the OEW SynRM under test. The ABB drive supplying the induction machine is not shown.

5.1.2 – Signal Acquisition Board

The measurement of the currents and voltages of the power loops has been centralized in a single round PCB (with dimensions to fit inside the machine) that features 3 isolated current measurements based on the CMS3015 from Sensitec, 3 isolated voltage measurements based on the ISO224B IC from Texas instruments and 2 LTC2325-12 ADCs from Analog Devices. A photo of the acquisition board is shown in Fig. 5.2 (a) top view and Fig. 5.2 (b) bottom view. The design documents of this board are provided in Appendix B.

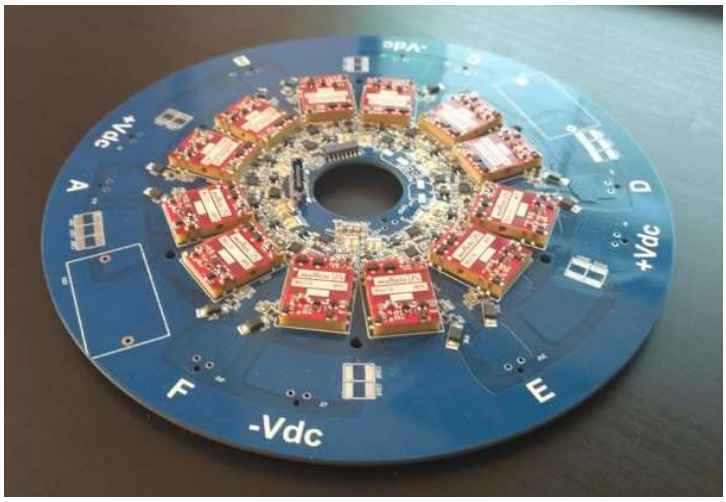


(a) (b)

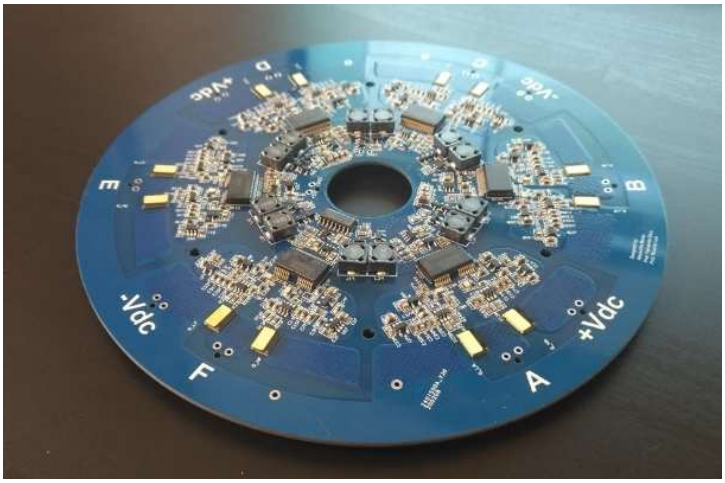
Fig. 5.2. Acquisition Board Photography. (a) Top view. (b) Bottom view.

5.1.3 – Dual Voltage Source Inverter

The DVSI board features 12 GaN HEMT GS66508T devices from the manufacturer GaN Systems that are switched ON at 6V and switched OFF at -3V. For this, the gate driver circuit of each GaN Arm utilizes one 2ED020I12-F2 manufactured by Infineon, providing isolation and over current protection using the DESAT function, while the drive of each of the HEMT gates is performed by one UCC27511A-Q1 from Texas instruments. The design documents of this board are provided in appendix C. A photo of the assembled DVSI board without heatsink is provided in Fig. 5.3. It is worth mentioning that the DVSI board has been designed with the possibility to connect dc-link capacitors. This allows the system to be connected to a CSR to operate as an IMC with DVSI when no dc-link capacitors are mounted or to be directly supplied by a dc-link voltage from a dc power supply or a battery bank to operate simply as a DVSI or a back-to-back converter. Also, the Acquisition board is designed to fit on top of the DVSI, their assemblage is shown in Fig. 5.4.



(a)



(b)

Fig. 5.3. Dual Voltage Source Inverter Board. (a) Top view. (b) Bottom view.

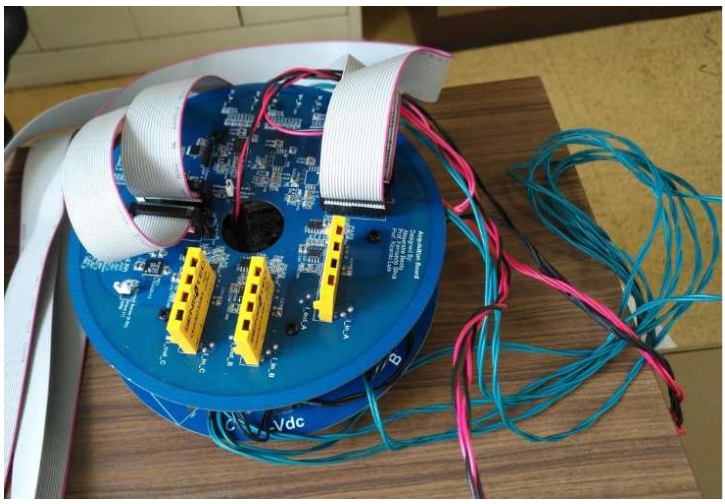


Fig. 5.4. Assembled DVSI + Acquisition board.

5.1.4 – Current Source Rectifier

The CSR designed features 12 G3R160MT12D SiC MOSFET and 12 GD10MPS12A SiC Schottky diodes from GeneSiC Semiconductor. The gate drive circuit utilizes one isolated 2ED020I12-F2 IC from Infineon per bidirectional switch, turning the SiC devices ON at 15V and OFF at -5V. A picture of the input stage board is presented in Fig. 5.5, while the design documents of this board are provided in appendix D.

The option of using SiC semiconductors in the input stage while using GaN devices in the output stage is due to the DVSI effective switching frequency being twice of the input stage, while the peak currents flowing through the input stage switches being higher than those in the output stage semiconductors. Thus, the option of using GaN devices for the output stage due to their lower switching losses characteristic, while using SiC devices for the input stage due to the lower switching frequency requirements and higher current rating requirement.

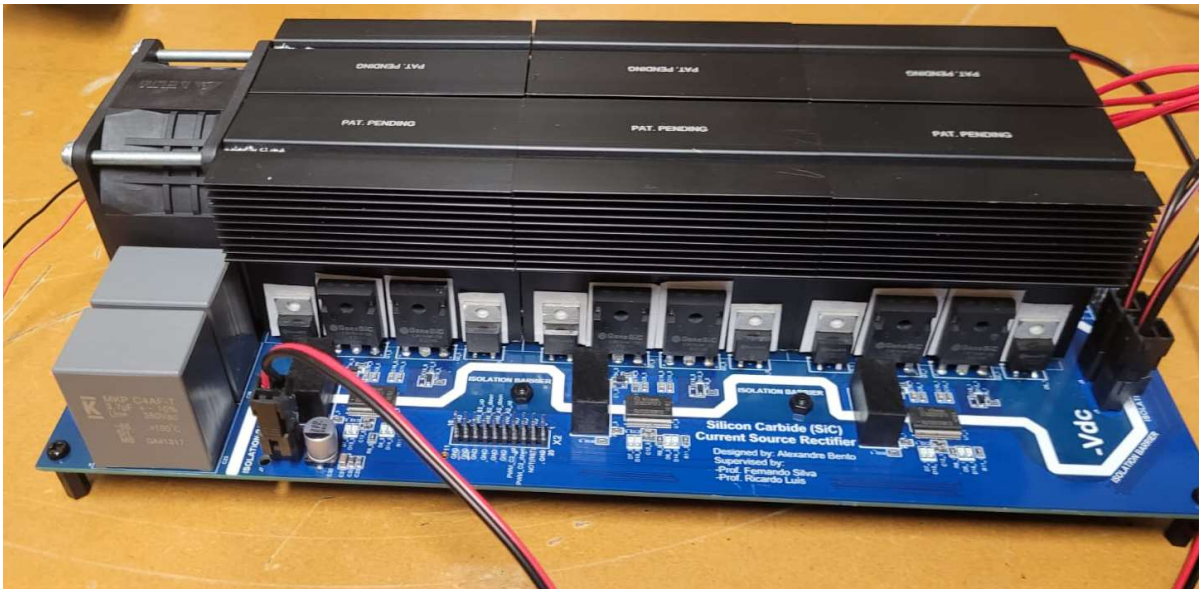


Fig. 5.5. Current Source Rectifier.

5.1.5 – Control Board

The control loops are implemented in a Xilinx System on Chip (SoC) module that combines both a programmable logic (PL) and a processing system (PS) on the same chip. This allows the implementation of the modulation method, its required multistep commutation logic, and the digital signal processing blocks such as controller loops, signal acquisition and observers in the FPGA fabric (programmable logic), while allowing easy integration with other systems by running Linux in the processing system. In this thesis, the PS is used to create a graphical user

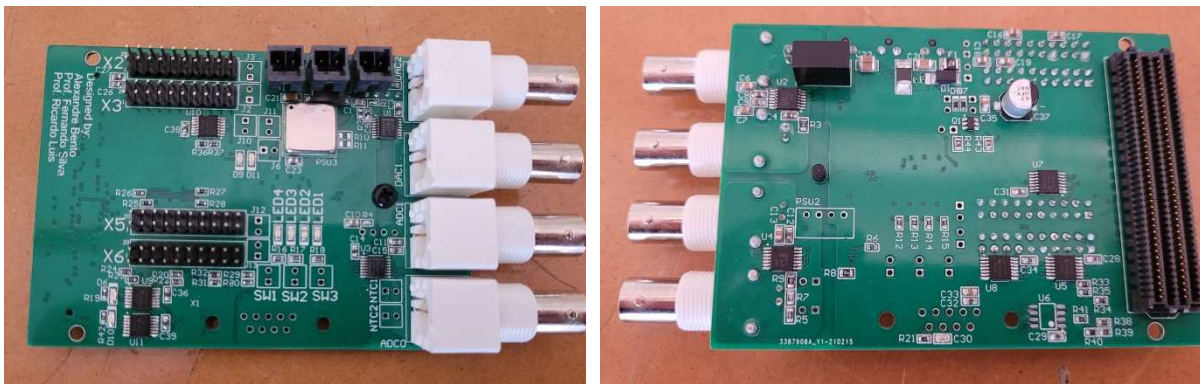
interface (GUI) in a webpage that not only allows the user to parameterize, provide setpoints and receive data of the drive state, but at the same time enables the visualization of real-time data of the drive, such as waveforms of currents, voltages, speed, estimated quantities, select the signal to be outputted to the DACs, etc. The specific control board used is a "Xilinx Zynq-7000 SoC ZC706 Evaluation Kit", presented in Fig. 5.6.

Fig. 5.6. Xilinx Zynq-7000 SoC ZC706 Evaluation Kit.

In order to interface the control board with the power boards, the acquisition board and the SynRM position sensor two other PCBs were designed:

- FPGA Mezzanine Card (FMC) Board;
- Isolation board for RS422 communication.

The FMC board features 4 SN74LV4T125PWR ICs for level translation (2.5V to 5V) to adapt the FPGA pins logic level to the Infineon driver ICs, a DC-DC converter (12V to 5V) to supply all the other boards, 2 MCP4922T-E/ST digital to analogue converters (DACs) and 2 MCP3302-CI/ST analogue to digital converters (ADCs). A picture of the assembled FMC board is provided in Fig. 5.7, while its design documents are provided in appendix E.

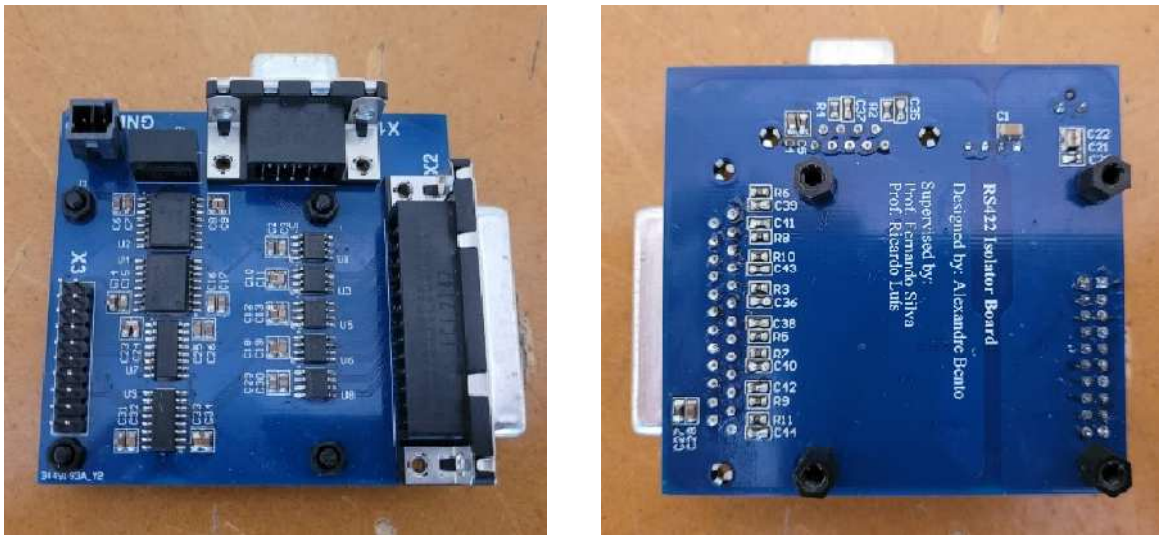


(a) (b)

Fig. 5.7. FMC board. (a) Top view. (b) Bottom view.

The RS422 isolation board provides 5 isolated digital inputs and outputs. One input and one output channels are used to interface with the SynRM position sensor, remaining 4 isolated bidirectional channels that can be used for extra DACs in the future. A photo of the assembled RS422 isolation board is provided in Fig. 5.8, while its design documents are provided in appendix F.

As mentioned above, the PS of the SoC produces a GUI on a webpage that is accessible through a computer or a smartphone within the same network. This GUI allows the user to turn on or shut down the system, to send references to the control loops, to select the signals to output by the DACs, and to visualize the waveforms of currents and voltages and other internal variables from the control loops. This webpage is shown in Fig. 5.9.



(a) (b)

Fig. 5.8. RS422 isolation board. (a) Top view. (b) Bottom view.

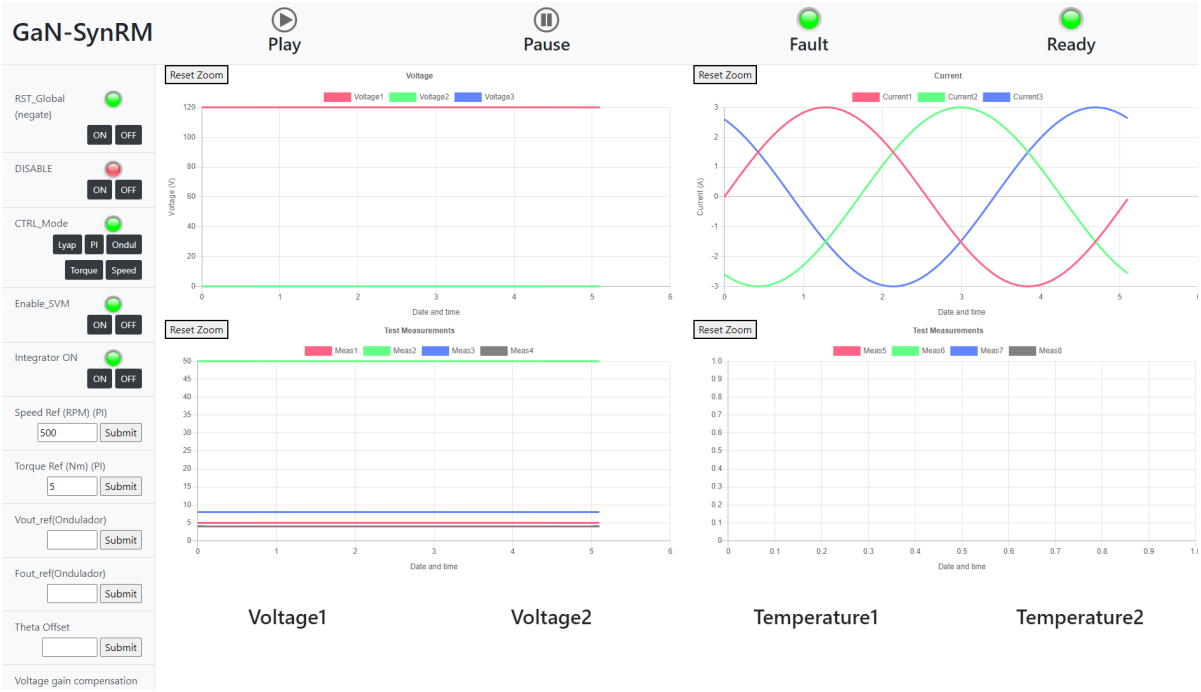


Fig. 5.9. Webpage produced by the SoC for graphical user interface.

5.2 – Adaptive non-linear Backstepping Speed controller for SynRM

The worldwide shortage of semiconductors and integrated circuit (IC) chips due to COVID-19 introduced a significant delay in the experimental work of this thesis. This led to some parts of the prototype to be fully assembled and commissioned later than others. This had special implication on the input stage converter which was only possible to be assembled very close to the PhD deadline. This forced the experimental validation of the proposed SynRM speed controller to be performed with a different laboratorial setup (with no CSR stage) than planned at the beginning by supplying the output stage directly from a DC power supply. This section presents experimental results for the Adaptive SynRM speed FOC based on the backstepping non-linear control technique.

Due to unexpected noise in the position sensor incremental function, the speed measurement is performed using the derivative of the absolute position given by the encoder absolute function. This required an additional low-pass filtering stage in the speed control loop. Furthermore, to reduce the oscillations introduced by the torque sensor elastic shaft in the machines coupling, the time constant for torque convergent, τ_e, has been selected to be 40ms (approximately half of L_q/R_s), which is higher than the value used in the simulation model, resulting in a reduction of the speed control loop gains.

On the proposed FOC, the gains also needed to be reduced. According to the theory proposed in section 4.1, to guarantee stability the only requirement is that the gains k_ω, k_I, k_q and k_d are positive constants, allowing the tunning of the gains to be performed according to the desired behaviour of the system. According to (4.12), the 1st layer of the proposed FOC controller gains are tuned for $\omega_0 = R_s / L_q$ and $\zeta=1$, while the 2nd and 3rd control loop gains are selected to improve the quality of SynRM currents waveforms.

The above conditions and the unavailability of the CSR input stage (due to the worldwide shortage of semiconductors) constrained to supply the DVSI board directly by one available BK Precision 9206B DC power supply. This power supply rated power is 600W with the maximum output voltage being 150V and its maximum output current being 10A. A picture of the laboratorial prototype is shown in Fig. 5.10.

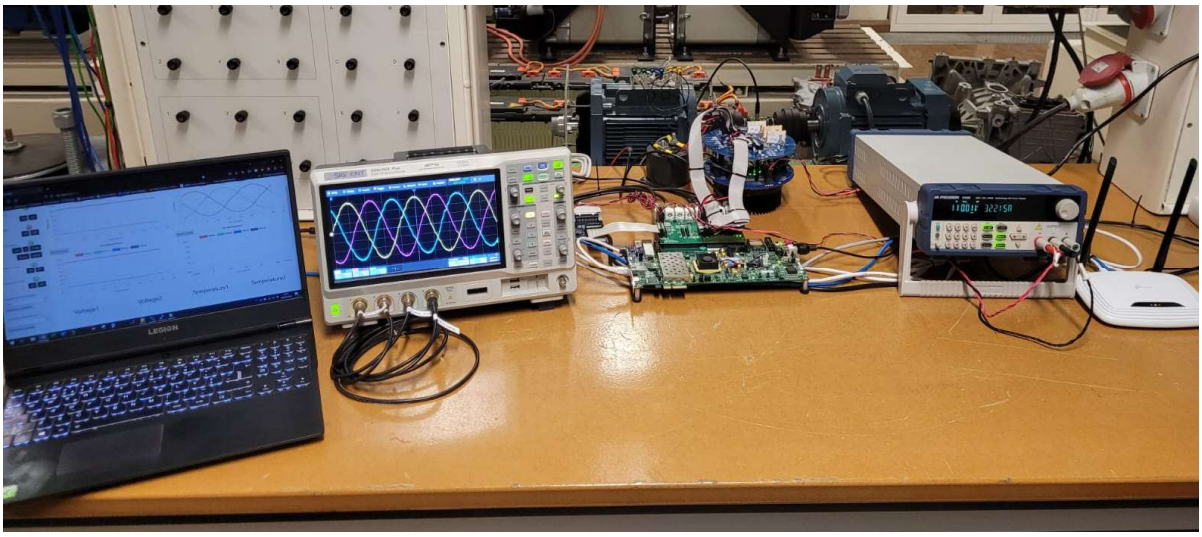


Fig. 5.10. Picture of the prototype used for experimental validation.

As seen in Fig. 5.11, for a dc-link voltage of 150V the maximum torque that could be produced at 1500rpm is around 1.5Nm. Also, if the operating speed is reduced to 750rpm, at the same dc-link voltage it is possible to develop around 10Nm of torque that would result in a mechanical power of 785W, which is already higher than the power supply rated power. For this reason, it is necessary to narrow the SynRM range of operation in terms of the speed used in the experimental tests and the maximum torque allowed to the controller. Thus, the maximum allowed torque reference for both controllers has been set to 5Nm and the speed reference for the tests has been chosen as 500rpm.

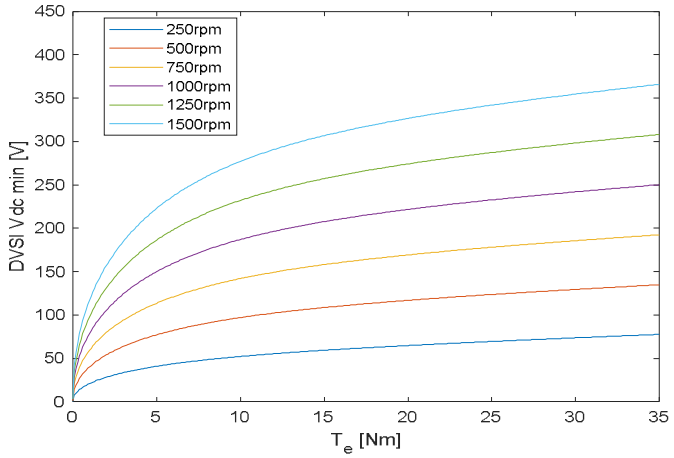


Fig. 5.11. Minimum required dc-link voltage to operate the SynRM with a given torque for different speeds (according to the MTPA trajectory).

Both FOC strategies have been computed at the rate of 10kHz, with a switching frequency of 50kHz. The controller gains used in the experimental validation for the two FOC strategies are presented in Table 5.1. Also, it is worth mentioning that the SVM strategy used for the experimental results is the one proposed in subsection 2.3.1.

To assess the performance of the proposed FOC and to compare it with the typical FOC, three different operation scenarios are introduced. In the 1st scenario, the objective is to assess the steady state behaviour, while the 2nd and 3rd scenarios have been introduced to evaluate the proposed FOC performance in transient behaviour. The corresponding operation details of each scenario are as follow:

- 1st Scenario: steady state operation for a load torque of 3Nm while the SynRM is rotating at 500rpm;
- 2nd Scenario: from standstill, a step of 500rpm in the speed reference is applied. Then after 2 seconds the reference speed is stepped to 500rpm in the opposite direction, and after again 2 seconds the reference speed returns to standstill. The load torque is almost null during this scenario;
- 3rd Scenario: while the SynRM is in steady operation at 500rpm with null load torque, a quick variation of 3Nm is applied as load torque.

Table 5.1. Laboratorial prototype control gains for both FOC strategies

Typical FOC	$k_{P\omega}$	0.2
	$k_{I\omega}$	1.21
	k_{Pd}	999
	k_{Id}	7083
	k_{Pq}	542
	k_{Iq}	7083
Proposed FOC	k_{ω}	22.7
	k_I	129
	k_q	750
	k_d	500

The figures that contain experimental results are divided in 3 subplots. Subplot (a) shows the reference speed and measured speed in CH1 and CH2 respectively, while the torque reference and the torque measured are provided in CH3 and CH4. In subplot (b) the direct axis current reference and its measured value are given in CH1 and CH2 respectively, while the quadrature axis reference current and measured value are provided in CH3 and CH4. The subplot (c) shows the SynRM currents (CH1-i_A, CH2-i_B, CH3-i_C) with the CH4 being used to show the reference torque in the scenarios that involve transient behaviour (2nd and 3rd scenarios). It is worth noting that the waveforms in subplots (a) and (b) are obtained through DACs whose output ranges from 0 to 5V, meaning that the zero is around 2.5V of the value shown in the oscilloscope.

5.2.1 – 1st Scenario: Steady State Operation

This scenario is intended to evaluate the steady state performance of both FOC strategies for a load torque of 3Nm. The results of the typical FOC are presented first in Fig. 5.12 while the proposed FOC experimental results are shown in Fig. 5.13.

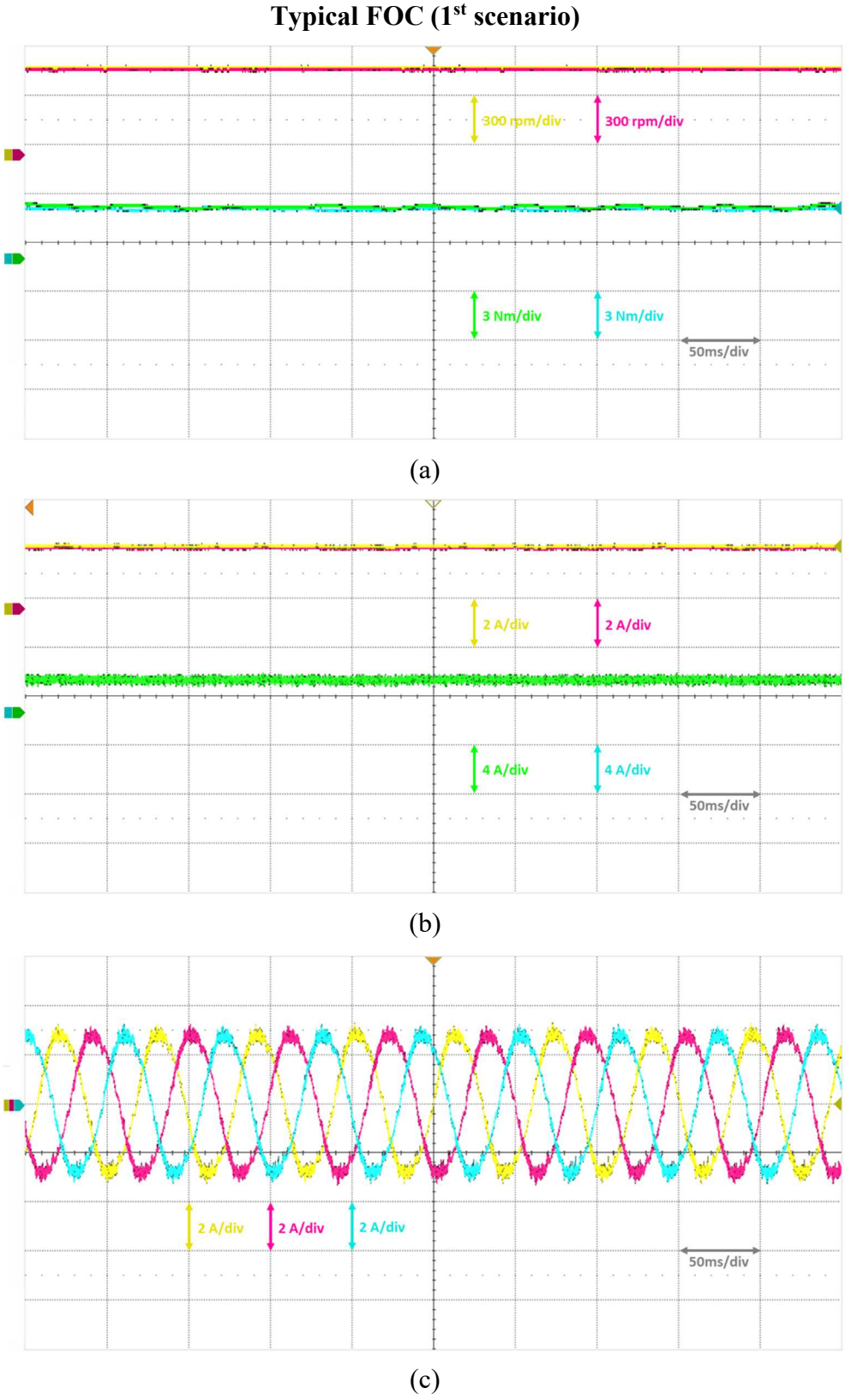


Fig. 5.12. 1st scenario experimental results of the typical FOC (ω_{ref}=500rpm, T_{load}=3Nm). (a)CH1-ω_{ref}, CH2-ω, CH3-T_e^*, CH4-T_e (b) CH1-i_d^*, CH2- i_d, CH3- i_q^*, CH4- i_q (c) CH1-i_A, CH2- i_B, CH3- i_C.

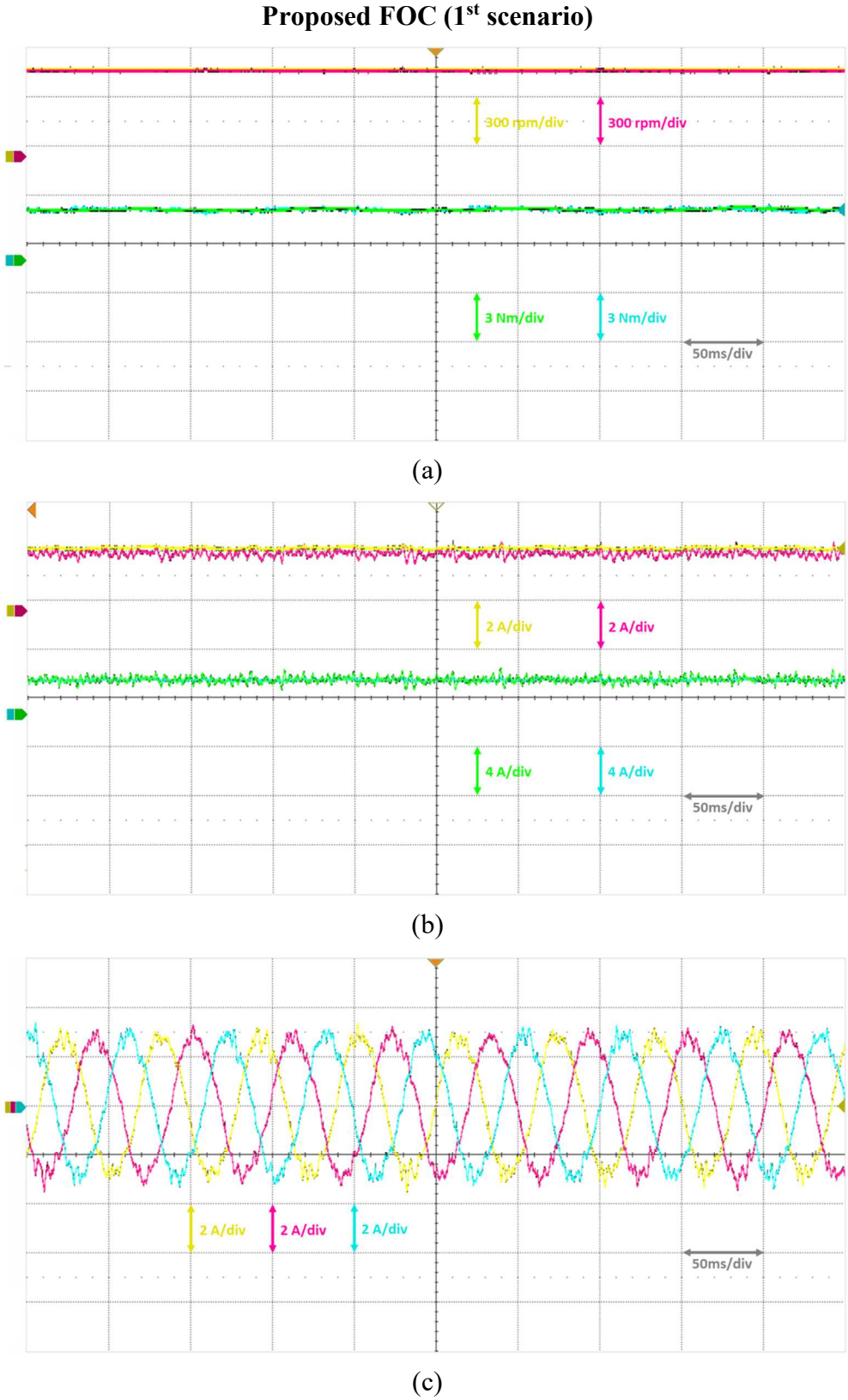


Fig. 5.13. 1st scenario experimental results of the proposed FOC (ω_{ref}=500rpm, T_{load}=3Nm). (a)CH1-ω_{ref}, CH2-ω, CH3-T_e^*, CH4-T_e (b) CH1-i_d^*, CH2- i_d, CH3- i_q^*, CH4- i_q (c) CH1-i_A, CH2- i_B, CH3- i_C.

In the simulation results presented in section 4.3.1 the steady state performance of both FOC schemes was undistinguishable. This is not totally true in the experimental setup. Let us compare individually each subplot of Fig. 5.12 and Fig. 5.13.

Subplot 1: In steady state it is seen that both FOC strategies track the reference speed and reference torque accurately. In the typical FOC scheme it is seen some very slight oscillations of the measure torque on top of the reference, while in the proposed FOC these slight oscillations are not seen.

Subplot 2: Direct and quadrature axes current control is analysed in this subplot. The typical FOC technique presents both axes currents clearly controlled, with the direct axis current being very smooth while the quadrature axis current presenting high frequency ripple. On the other hand, the proposed FOC controller achieves currents that present lower frequency ripple on both axes, being the quadrature current right on top of its reference while the direct axis current showing steady state error by being slightly lower than the reference current. This is explained by the absence of an integrator in the current control loops of the proposed FOC technique which relies on the observed inductance values to achieve null steady state error. It is known that the RLS observer does not perform optimally in the lower speed range. However, because of the backstepping term that introduces a term proportional to the velocity error and the direct axis current on the quadrature voltage reference, as given by (4.18), the electromagnetic torque produced by the SynRM is smother than in the typical FOC case.

Subplot 3: Similar to the direct and quadrature axes currents, the SynRM phase currents of the typical FOC technique present higher frequency ripple than the proposed FOC. Still, the lower frequency ripple in the SynRM currents of the proposed FOC appears to be slightly bigger than the high frequency ripple of the typical FOC.

Thus, the steady state performance of both controllers is not undistinguishable as it seemed from the simulation results, but it is very similar with the main difference being in the frequency of the ripple present in the SynRM currents.

5.2.2 – 2nd Scenario: Rapid SynRM acceleration and deacceleration

This scenario is intended to evaluate how the SynRM drive reacts to a rapidly changing speed reference. The typical FOC experimental results under this scenario are presented in Fig. 5.14 while the proposed FOC technique results are shown in Fig. 5.15

From subplot (a), it is concluded that as expected both FOC techniques accurately track the speed reference, with the proposed FOC technique converging approximately 50% faster and with lower overshoot than the PI based FOC. On the torque developed by the SynRM, in the period right after the steps in the speed reference are applied, the measured torque do not follow the reference torque in neither of the FOC approaches. On the other hand, it is seen that for the typical FOC, the direct and quadrature axes reference currents are perfectly tracked. This means that the discrepancy observed in the torque measured by the PI based FOC should be due to the torque sensor operation being based on extensometers measuring the sensor shaft deformation, which introduce an unmodeled dynamic effect of a spring in the shaft. Thus, the torque sensor is measuring something that is created by itself on top of the torque developed by the SynRM. With regard to the proposed FOC approach, it is seen that during the periods while the machine is rapidly accelerating and deaccelerating, the quadrature axis current is higher than its reference value. This happens due to the backstepping term that introduces additional voltage to the quadrature axis reference voltage in order to stabilize the system faster, which results in higher quadrature current and higher developed torque when the speed error is large. This situation was not observed in the simulation results because the speed variations were performed as a ramp instead of a step.

Regarding the quality of the current waveforms, it is relevant to state that the SynRM currents while operating at no load with the typical PI based FOC are significantly better than the SynRM currents while operating with the proposed control method. This is observed in both subplot (b) and subplot (c), being explained by the proposed FOC providing a faster and more aggressive response to changing operating conditions but also to small errors in the quantities measured.

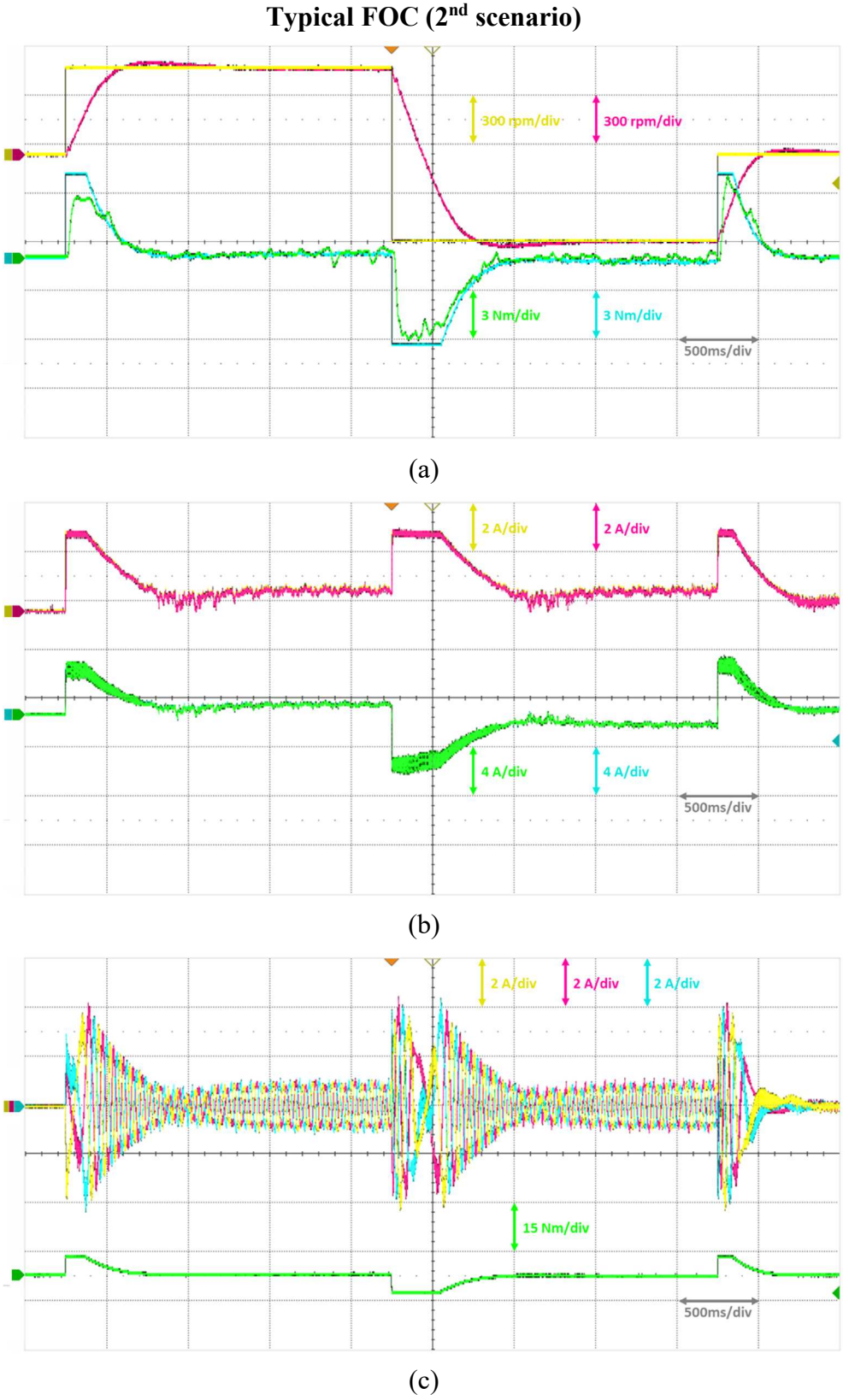
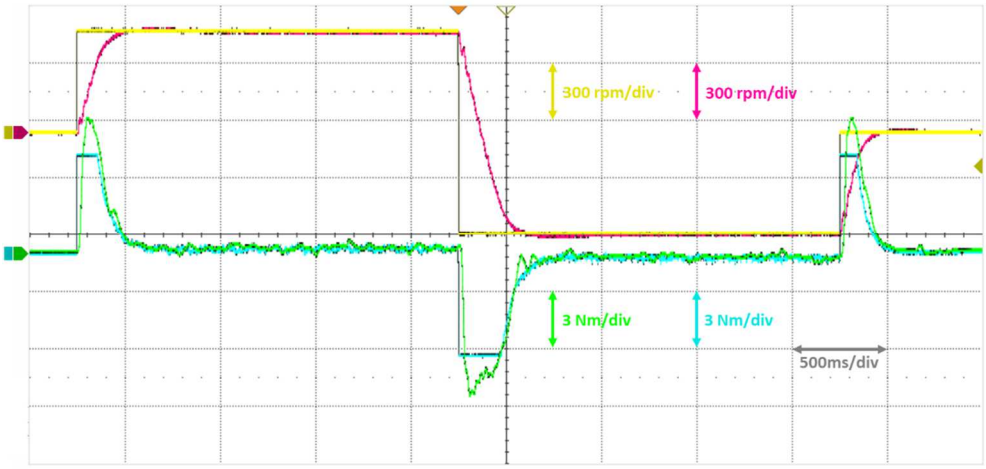
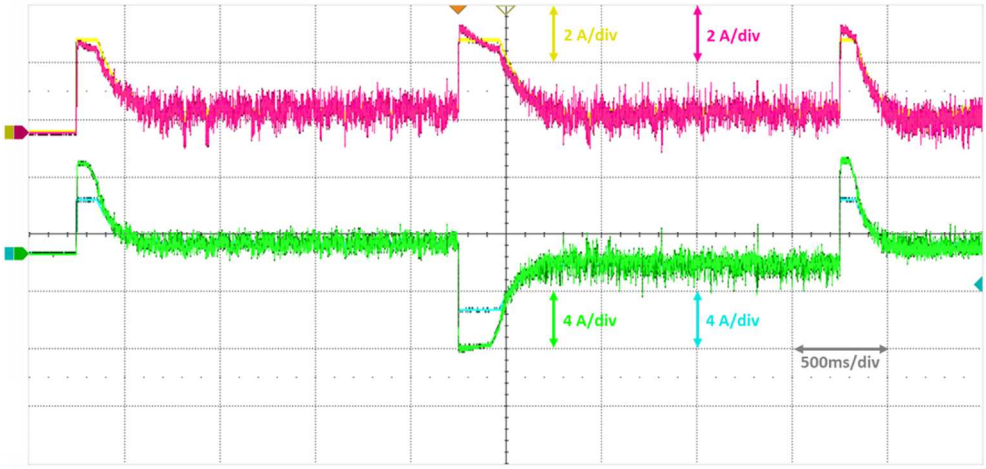


Fig. 5.14. 2nd scenario experimental results of the typical FOC (T_{load}=0Nm). (a)CH1-ω_{ref}, CH2-ω, CH3-T_e^*, CH4-T_e (b) CH1-i_d^*, CH2-i_d, CH3-i_q^*, CH4-i_q (c) CH1-i_A, CH2-i_B, CH3-i_C., CH4-T_e^*

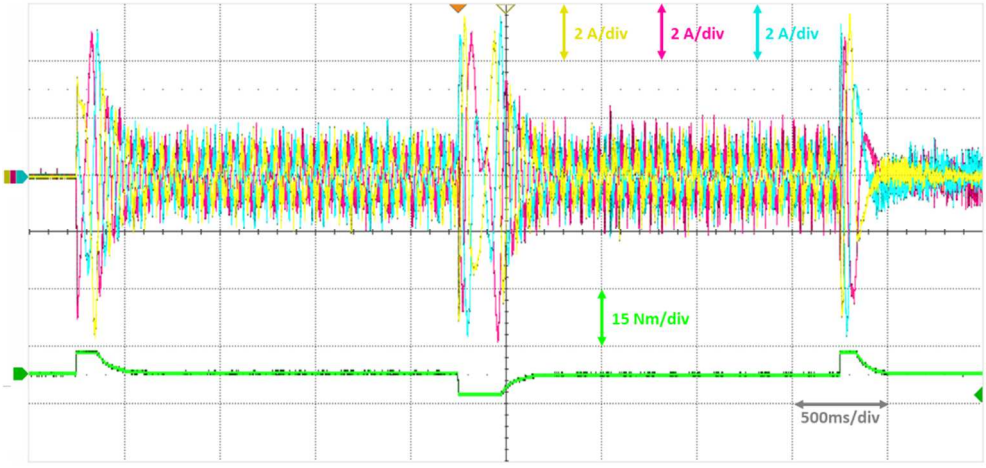
Proposed FOC (2nd scenario)



(a)



(b)



(c)

Fig. 5.15 2nd scenario experimental results of the proposed FOC (T_{load}=0Nm). (a)CH1-ω_{ref}, CH2-ω, CH3-T_e^*, CH4-T_e (b) CH1-i_d^*, CH2-i_d, CH3-i_q^*, CH4-i_q (c) CH1-i_A, CH2-i_B, CH3- i_C., CH4-T_e^*

5.2.3 – 3rd Scenario: Load Torque Step

This operating scenario is meant to assess the capability of handling abrupt load torque variations while maintaining a fixed reference speed. In this case the load torque applied is 3Nm while the speed reference is kept at 500rpm. The typical FOC experimental results under this scenario are presented in Fig. 5.16 while the proposed FOC technique results are shown in Fig. 5.17.

By comparing the subplot (a) of both FOC strategies, it is possible to observe that the speed deviation due to the load torque variation in the PI based FOC is approximately double than the speed deviation obtain with the proposed FOC technique. Regarding the developed torque it is visible that the proposed FOC achieves the final load torque about 60ms faster than the PI based strategy. Also, it is worth mentioning that during the ramp of the reference torque in both FOC methods, there are oscillations in the developed torque while oscillations are not seen in the direct and quadrature currents, which once again may be explained by the torque sensor introducing an unmodeled dynamic effect of a spring in the shaft, creating those oscillations.

On the SynRM direct and quadrature axis currents, it is seen that in both cases the current references are tracked. It is worth mentioning that for the proposed FOC technique, due to the velocity error being kept small, the backstepping term effect on the quadrature axis current is not visible.

Regarding the quality of the SynRM currents, in subplot (c) it is clearly seen that the PI based FOC currents with null mechanical load (begin of the test) are significantly better than in the proposed FOC. However, this is faded out as the mechanical load increases and ultimately by the end of this scenario the steady state documented in scenario 1 is achieved.

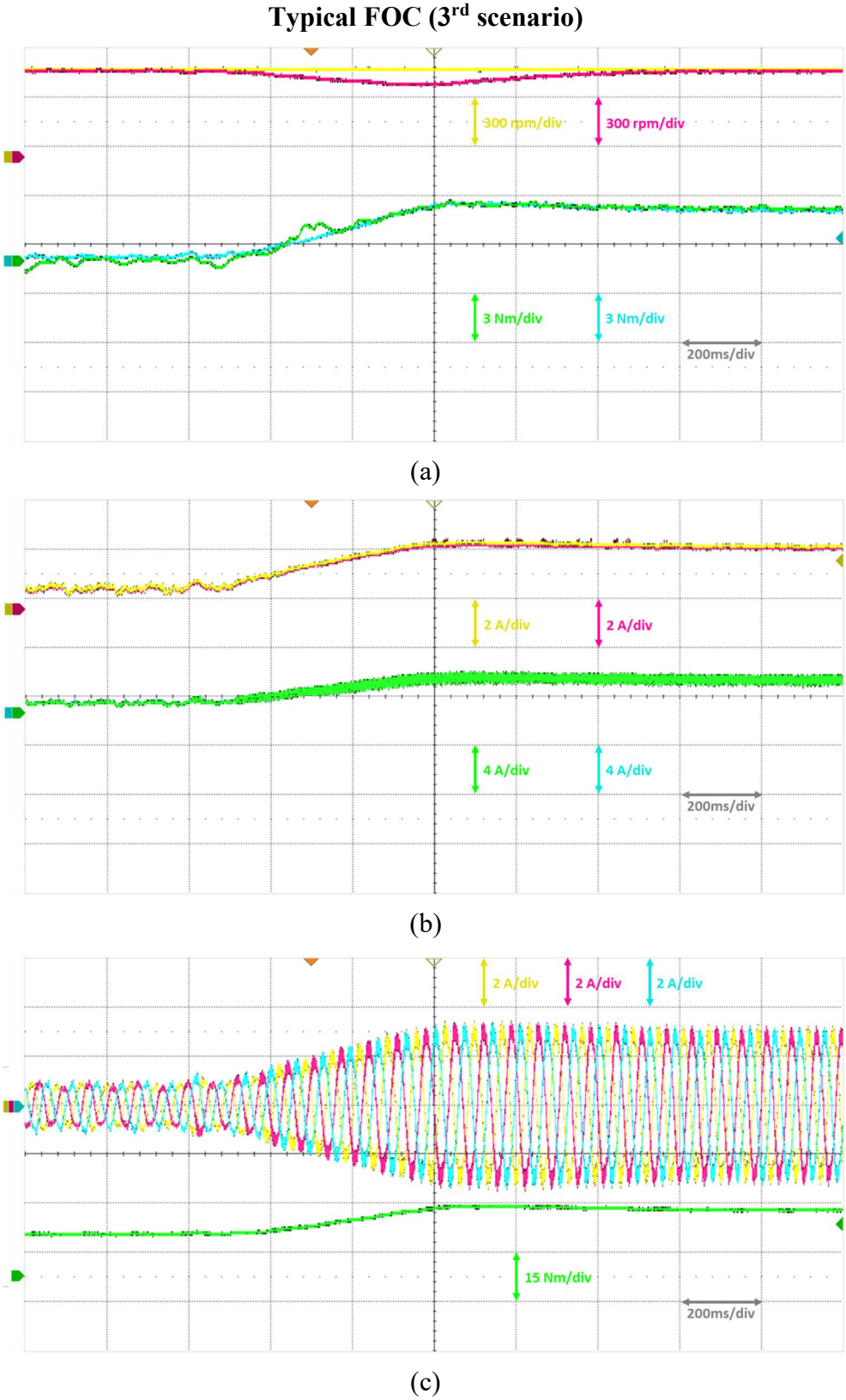


Fig. 5.16. 3rd scenario experimental results of the typical FOC (ω_{ref}=500rpm). (a) CH1-ω_{ref}, CH2-ω, CH3-T_e^*, CH4-T_e (b) CH1-i_d^*, CH2-i_d, CH3-i_q^*, CH4-i_q (c) CH1-i_A, CH2-i_B, CH3- i_C., CH4-T_e^*

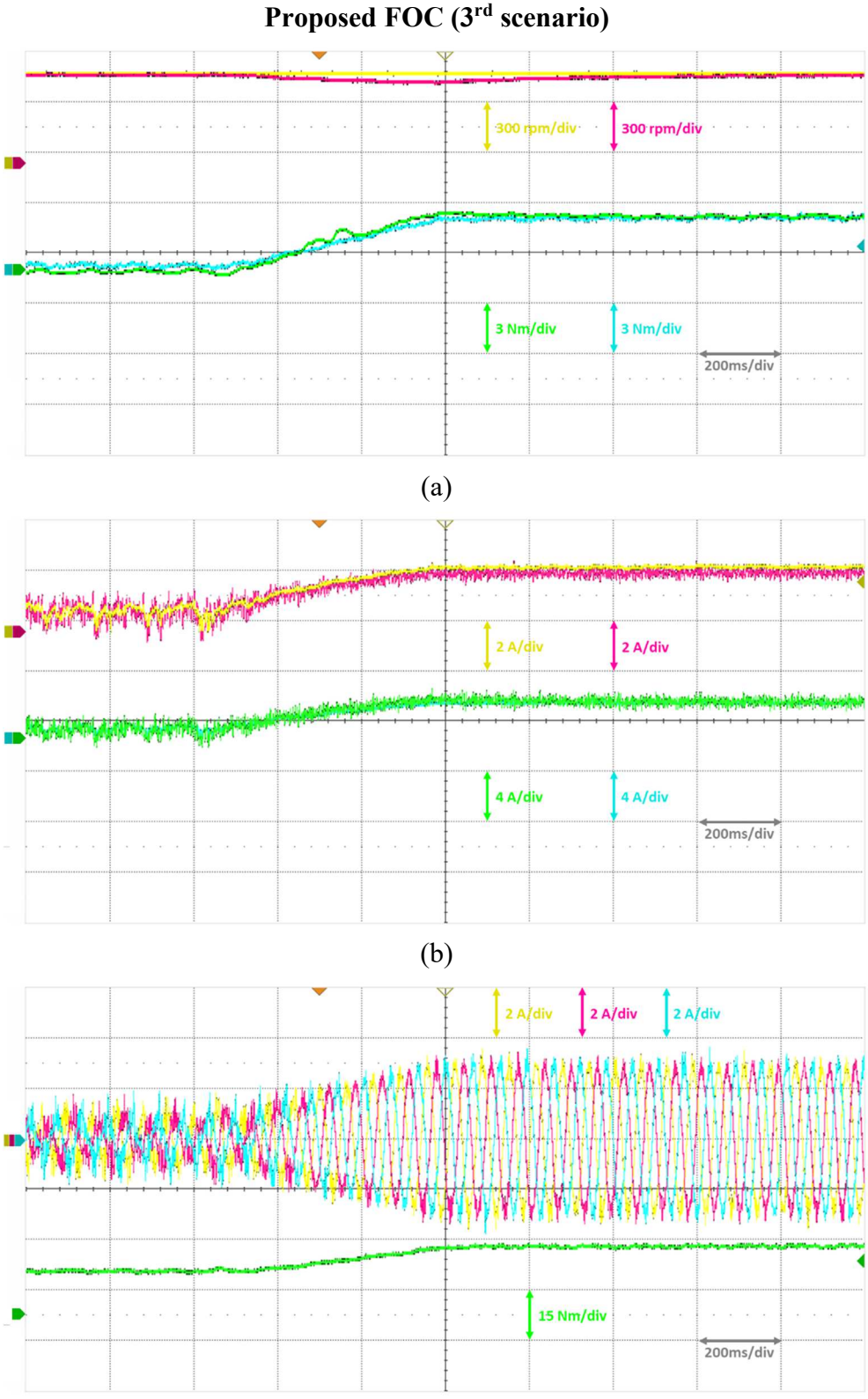


Fig. 5.17. 3rd scenario experimental results of the proposed FOC (ω_{ref}=500rpm). (a) CH1-ω_{ref}, CH2-ω, CH3-T_e^*, CH4-T_e (b) CH1-i_d^*, CH2-i_d, CH3-i_q^*, CH4-i_q (c) CH1-i_A, CH2-i_B, CH3-i_C., CH4-T_e^*

5.3 – Novel SVM strategy for CMV reduction

As stated in the previous section, it was only possible to assemble the input stage of the converter by the end of the PhD. This section focus on presenting experimental results of the proposed SVM technique for the IMC with DVSI output supplying the SynRM under study while using the proposed non-linear speed controller. A picture of the full assembly is shown in Fig. 5.18.

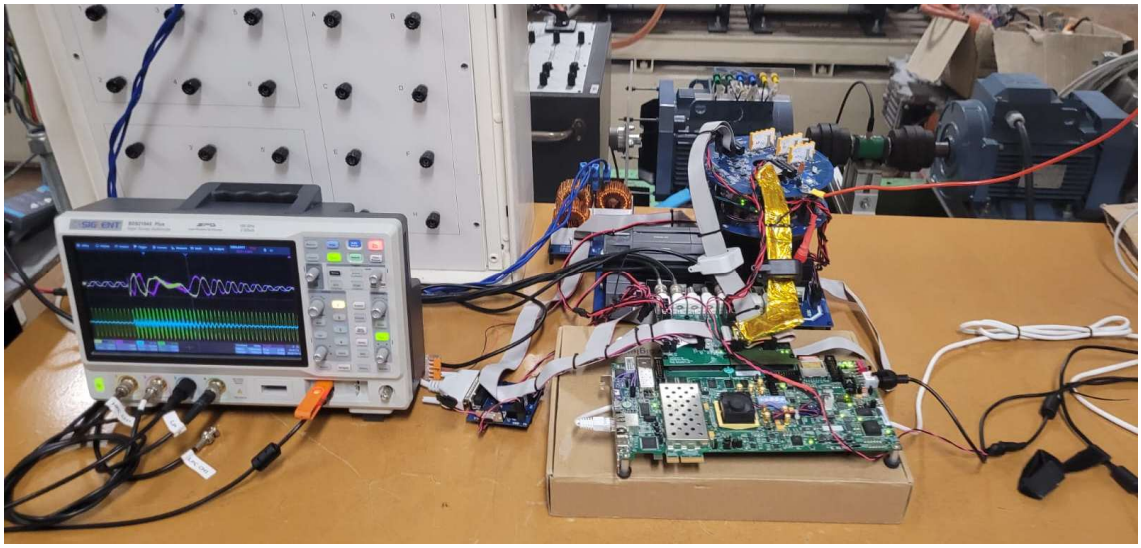
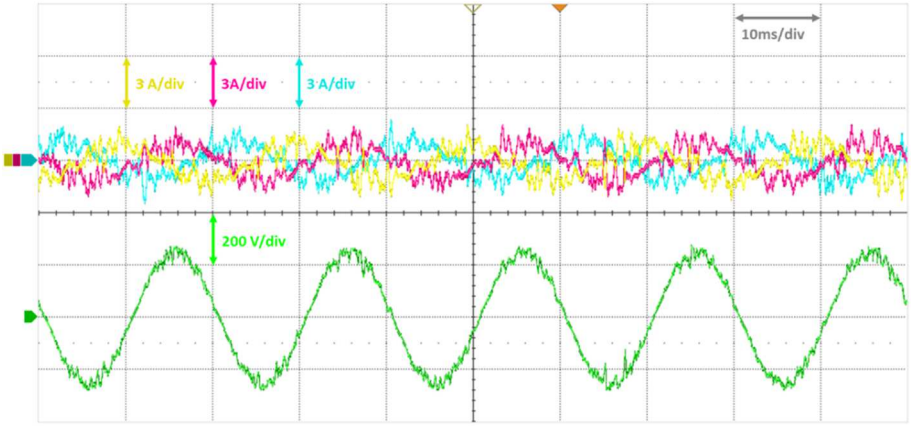


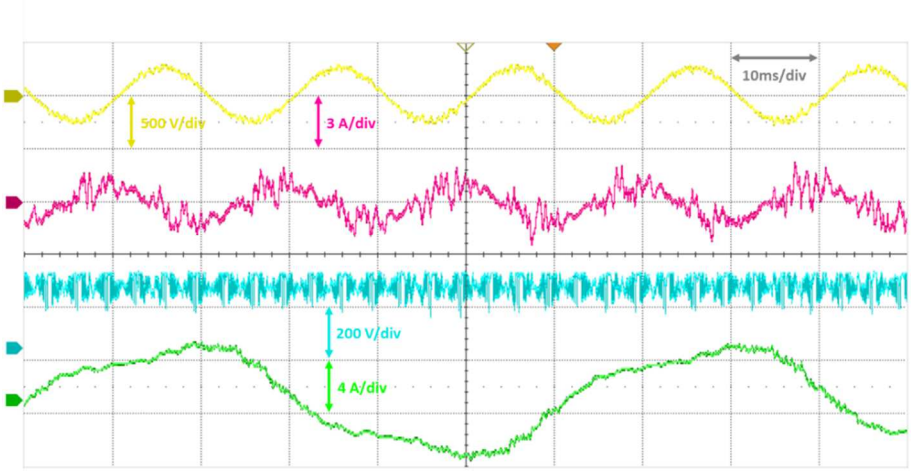
Fig. 5.18. Complete prototype of the proposed drive.

As concluded by the simulation results presented in section 4.3.2, the input stage modulation technique that allows bigger reduction in the CMV at the machine terminals is the one that results in maximum dc-link voltage. At the same time, due to the high *dv/dt* and *di/dt* typical of wide band gap devices, the measurements of the acquired signals were suffering from communication noise. This was slightly reduced by placing extra decoupling capacitors and by adding shielding to the flat cables used for digital communication between the FPGA and the ADCs, being the more significant measure the addition of ferrites to those same flat cables. However, this did not entirely solve the problem and extra shielding between the power board and the acquisition board should be added with proper grounding. For this reason, the input voltage level used in this section had to be reduced to a value where no communication noise was observed, this voltage level was 100V of $V_{ph\ rms}$. Thus, this section solely provides results of the proposed SVM strategy for CMV reduction featuring the input stage modulation with maximum dc-link voltage. These results are presented in Fig. 5.19 for a unity power factor

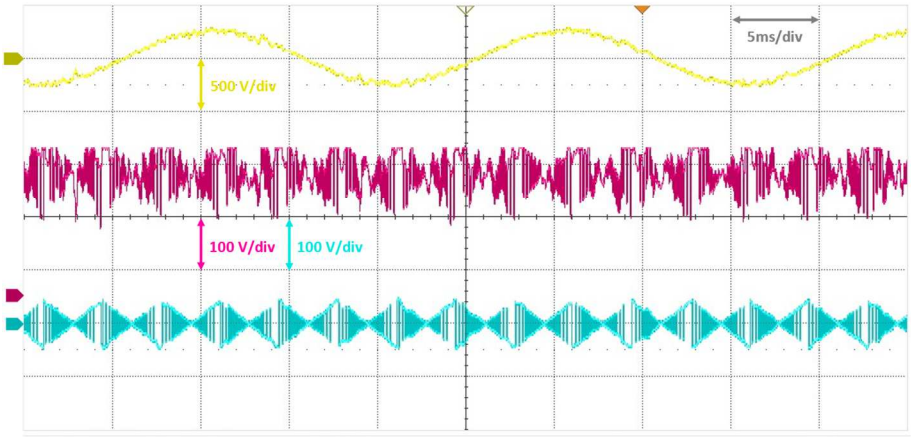
operation while the SynRM is operated as a generator at 500rpm and load torque of -9Nm using the control method proposed in section 4.1 and the control gains indicated in section 5.2.



(a)



(b)



(c)

Fig. 5.19. Experimental waveforms of the proposed SVM Technique (ω=500rpm, T_{load} = - 9Nm, Φ_i=0, $V_{ph\ rms}$=100V). (a) CH1-i_a, CH2- i_b, CH3- i_c, CH4- v_{ab}. (b) CH1- v_{ab}, CH2- i_a, CH3- v_{dc}, CH4- i_A. (c) CH1- v_{ab}, CH2- v_{dc}, CH3- *CMV*

The grid currents and the line-to-line voltage measured at one of the filter capacitors are shown in Fig. 5.19.(a). Comparing the phase 'a' current with the line-to-line voltage 'V_{ab}', it is possible to observe that the drive is injecting power into the grid. Regarding the harmonic content present in the waveforms, it is clearly noticeable high frequency ripple in the currents but also in the filter capacitor voltage. This is due to the filter being designed for 230V of $V_{ph\ rms}$, meaning that at 100V of $V_{ph\ rms}$ the filter lacks energy stored in the capacitors and should be modified for operation at this voltage levels.

On subplot (b) of Fig. 5.19, the line-to-line voltage 'V_{ab}' measured at the filter capacitor is shown along with the phase 'a' grid current, the soft dc-link voltage and the SynRM phase 'A' current. Note that just as the high frequency ripple is noticeable in the filter waveforms, it is also noticeable at the dc-link voltage, which once again is explained with the filter not being properly designed for the present operating condition. On the SynRM phase 'A' current, the high frequency ripple is not noticeable. However, note that the current waveform is not perfectly sinusoidal which can be explained by asymmetries in the SynRM magnetic circuit.

On subplot (c) of Fig. 5.19, it is given detail to the soft dc-link voltage in CH2 while the CMV waveform is shown in CH3. Note that the CMV waveform is very similar to the CMV waveform obtained in the simulation results of subsection 4.3.2, with a lower peak value due to the lower voltage level at the input of the converter. The peak CMV with 100V of $V_{ph\ rms}$ is bellow 50V.

Regarding choosing the SynRM as an ideal candidate for the power converter integration due to offering more favourable thermal conditions due to absence of rotor currents. An interesting result is presented in Fig. 5.20.(a) where a thermal image of the mechanical testbench is shown, being the SynRM the machine on the left, while the induction machine is the machine on the right. It is clearly seen that the SynRM operates with significant lower temperature than the induction machine. Still, it is worth mentioning that because the SynRM is operating as generator, the induction machine is processing slightly more power than the SynRM which should result in a temperature increase. In subplot (b) of Fig. 5.20, a thermal figure of the power converters is shown, where it is possible to observe that the output stage is slightly warmer than the input stage. This is explained by better heatsink design on the input stage with capability of active cooling through fan and by the usage of the input stage modulation with maximum dc-link voltage which results in higher switching losses on the DVSI while reducing the conduction losses in the CSR.

(a) (b)

Fig. 5.20. Thermal picture of the experimental setup. (a) Electric machines, SynRM on the left and Induction machine on the right. (b) IMC with DVSI output, DVSI on top and CSR on the bottom.

5.4 – Experimental Work Conclusions

Over the course of this PhD thesis, a laboratorial prototype with significant complexity has been designed, assembled, and tested. This consisted of five different PCBs, whose applications range from an expansion board (such as the two FMC boards), to two interface boards such as the RS422 isolator to integrate the SynRM position sensor and the acquisition board for isolated voltage and current measurements, to two power converters based on WBG technologies such as the DVSI (featuring GaN HEMT devices) and the CSR (featuring SiC MOSFET devices). In addition to the built hardware, the prototype also includes several blocks of Hardware Description Language for the control, modulation, 4 step commutation logic, communication protocols to interface with sensors, ADCs and DACs, and software to create the GUI.

The design, construction, and commissioning of such prototype from scratch added to a worldwide shortage of semiconductors due to a pandemic event is challenging. Ultimately, this led to the CSR being assembled only very close to the end of the PhD deadline, which required the experimental validation of the novel SynRM speed controller and the novel SVM strategy to be performed separately.

The “Adaptive non-linear Backstepping Speed controller for SynRM” experimental validation was performed with the DVSI being supplied through a DC power supply with a low voltage and current rating compared to the SynRM under study. This required the SynRM operation

range to be adapted and narrowed to properly fit the operating range of the DC power supply used. With this said, both FOC strategies were implemented successfully, being the laboratorial results obtained very similar to the simulation model results. Thus, it was observed that the proposed FOC technique allows an improvement in the dynamic response of the system to load disturbances and speed reference abrupt changes. Regarding steady state operation, it was observed that the PI based FOC technique in no load scenarios achieves SynRM currents with significantly better quality than the ones obtained with the proposed FOC. This effect is faded out as even a light mechanical load is coupled to the shaft. It is then concluded that the proposed FOC technique may represent an edge for high-performance motors drive applications that typically require improved dynamic response. On the other hand, for applications that most of the time work in steady state and where the computation power is a limiting factor, the traditional PI based FOC may be a better fit due to not requiring the observation of SynRM quantities.

The ”Novel SVM strategy for CMV reduction” experimental validation was performed. However, there are some optimizations to do on the prototype to eliminate noise in the acquired signals. This required the decrease of the converter input voltage to operate safely the converter due to the dependence on the acquired signals for the multistep commutation logic inherent of matrix converters. The reduction of the input voltage level on one side allowed the elimination of the communication noise between the FPGA and the ADCs, but on the other side resulted in the input filter being poorly designed for the voltage levels used which resulted in noisy input currents and voltages in the filter. However, despite the difficulties it was possible obtain experimental results on the CMV of the proposed SVM technique, being the obtained waveform extremely similar to the results obtained through simulation in section 4.3.2.

CHAPTER 6

CONCLUSIONS

6.1 – Final Considerations

This thesis deals with technologies that may enable the concept of grid-connected smart and embedded motor drives. Such drive requires solutions to challenges that pass through improving the power density, robustness, efficiency, and controller performance of variable speed drives, facilitating the integration of the power electronic converter and its control inside the electrical machine. The inside of electrical machines is characterized by harsh conditions in terms of operating temperature, vibrations, and lack of available space. For this reason, this thesis focuses on the usage of a specific class of power converters, the matrix converters. These converters are majorly based on power semiconductors, not requiring any intermediate energy storage devices in the dc-link, excusing the dc-link capacitor, which is one of the bulkier and more prompt to fail components of switched power converters. On the other hand, traditional matrix converters input to output voltage gain is limited to 0.866 representing a significant drawback of such converters due to limiting the speed range of electrical machines, and consequently decreasing the constant power speed range of VSDs.

Meanwhile, it is well known that electric machines fed by switched power converters suffer from high-frequency bearing currents, due to the pulsed CMV supplied by the converter. These currents are in the origin of most VSDs premature failures. This thesis proposes the usage of a converter topology that replaces the VSI found in the output stage of traditional IMCs by a DVSI, allowing the electric machine to be connected in an OEW configuration improving the converter input to output voltage gain to 1.5.

Then, a novel SVM strategy for the IMC with DVSI is proposed, which consists in utilizing the CMV contribution of the output stage, to counteract the CMV contribution of the input stage, ultimately resulting in the overall reduction of CMV. When compared with the state of art SVM strategy to reduce the CMV in IMC with DVSI, the proposed SVM technique allowed a significant reduction in the CMV peak values at the load terminals using the input stage

modulation method that provides maximum dc-link average voltage. The size of CMV reduction depends on the reference phase for the grid current. When the modulated grid current phase is null (unity power factor operation) the obtained CMV reduction is around 30%. On the quality of the input and output currents of the drive, the proposed SVM strategy clearly achieves currents with significantly lower THD in simulation results.

When compared with the SVM technique that disregards the value of CMV, the proposed SVM scheme maintains the low THD of the input and output current waveforms but loses the ability to switch the input stage bidirectional switches without any multistep commutation logic. Thus, the cost of reducing CMV in such drive is the requirement for multistep commutation processes for switching the input stage bidirectional switches. Note that in the state of art SVM technique for CMV reduction, this was already a requirement.

With respect to the electric machine itself, this thesis focused on the control of SynRMs. This type of machine operates based on the reluctance principle, not requiring any permanent magnets of rare earth materials nor currents in its rotor. SynRMs combine low cost and robustness due to the absence of permanent magnets when compared to PMSMs, while providing a cold rotor and improved efficiency due to the absence of currents in its rotor when compared to induction machines. This thesis introduced a novel FOC algorithm based on the replacement of the usual linear controllers by an adaptive non-linear backstepping controller featuring a RLS algorithm for electrical parameter observation. The proposed controller can maintain the excellent steady state performance of typical of FOCs, while improving the drive dynamic performance, the weakness of typical FOCs regarding other non-linear control strategies.

6.2 – Future Work

This PhD thesis touches various relevant topics for variable speed drives. However, it is not possible during the course of a PhD to dive very deeply into most topics which although being promising and interesting, at some point must be considered as they are outside of the thesis work plan. The following future research topics are suggested:

SynRM parameter identification:

- Evaluate how the proposed SynRM parameter identification method compares with the typical and more complex SynRM identification methods that are presented in the

literature in terms of obtained direct and quadrature axes inductances and SynRM operating trajectories.

- Evaluate how the zero-sequence current impact the direct and quadrature axes inductances. There may be room for controlling the zero-sequence current in a way that saturates faster the quadrature axis regarding the direct axis, allowing an edge in the direct and quadrature axis inductances difference term, which is proportional to the SynRM produced torque.

Proposed FOC:

- Overcome the necessity of a position sensor in the proposed drive, transforming the proposed FOC in a sensorless FOC scheme.
- Incorporate a SynRM stator resistance estimation algorithm in the proposed FOC technique. This should work in parallel with the RLS used to estimating the direct and quadrature axes inductances.
- Evaluate the performance and required computational burden of running the proposed FOC technique with other non-linear control techniques such as the MPC and DTC with fixed switching frequency.

Proposed SVM technique:

- Extend the modulation method and the CMV reduction strategy to multiphase machines.
- Elimination of the passive damping element of the input filter, including an active damping mechanism in the proposed drive. This would require a new controller for the grid current injection.

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APPENDIX A

TRADITIONAL FOC GAINS COMPUTATION

In section 4.3 the proposed FOC technique (based in Lyapunov control theory) was compared to the typical FOC (based in PI controllers). Thus, it is relevant to present how the linear controller gains were tuned.

As shown in Fig. 3.9, the typical FOC algorithm contains three PI controllers, see Fig. A.1. The first PI outputs the reference electromagnetic torque based on the speed tracking error, the other two (one for each electrical axis, *d* and *q*) compute the reference output voltage based in the currents error.

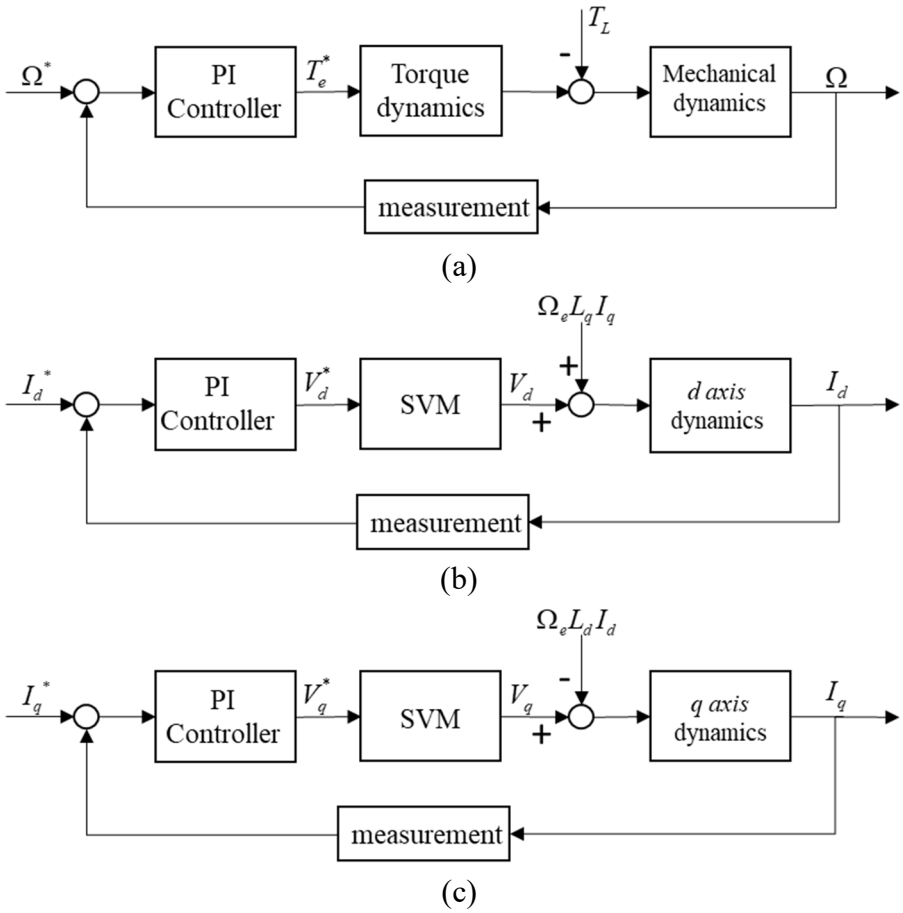


Fig A.1. Block diagrams of the three PI controllers of typical FOCs. (a) speed control loop, (b) *d* axis current control loop, (c) *q* axis current control loop.

Speed Control Loop

The Linear controller transfer function has $k_{p\omega}$ as proportional gain and $k_{i\omega}$ as the integral gain. Its transfer function is given by:

$$\frac{T_e^*}{E_\Omega} = \frac{sk_{P\omega} + k_{I\omega}}{s}$$

The developed torque convergence to the reference torque depends on the performance of the current control loops. Let us assume that the torque developed by the electric machine follows the reference torque, T_e^*, with a given time constant, τ_e, and with a gain, K_T. In such scenario, the torque dynamics can be written by:

$$\frac{T_e}{T_e^*} = \frac{K_T}{1 + s\tau_e}$$

The electric machine mechanical dynamics formulation presented in section 3.1 in the time domain, can be written in the frequency domain using the Laplace transformation, resulting in the transfer function given by:

$$\frac{\Omega}{T_e - T_L} = \frac{1}{sJ + K_d}$$

For generality, let us define α_ω as the velocity measurement gain.

Thus, the resulting block diagram for the speed control loop is shown in Fig. A.2.

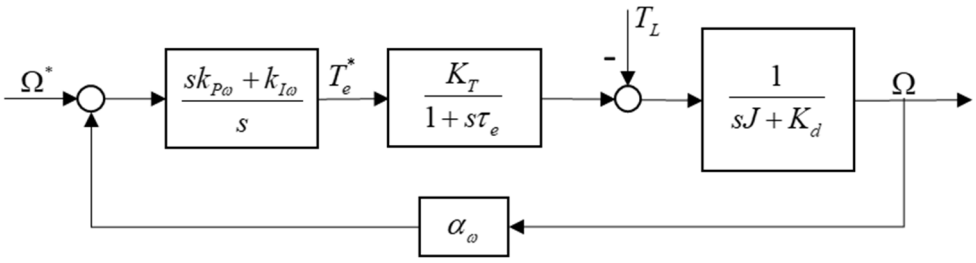


Fig A.2. Block diagram of the speed control loop.

The closed loop transfer functions can be computed using the superposition methods in relation to both system inputs (Ω^* and T_L):

$$\frac{\Omega}{\Omega^*} = \frac{s\left(k_{P\omega}K_T\right) + k_{I\omega}K_T}{s^3\left(\tau_e J\right) + s^2\left(k_D\tau_e + J\right) + s\left(\alpha_\omega K_T k_{P\omega} + k_D\right) + \alpha_\omega K_T k_{I\omega}}$$

$$\frac{\Omega}{T_L} = \frac{s\left(\tau_e s + 1\right)}{s^3\left(-J\tau_e\right) + s^2\left(-J - k_D\tau_e\right) + s\left(\alpha_\omega K_T k_{P\omega} - k_D\right) + \alpha_\omega K_T k_{I\omega}}$$

The steady state value of Ω to step variations of the system inputs, Ω^* and T_L, can be computed using the Final value theorem:

$$\lim_{t\to\infty}\Omega\Big|_{T_L=0} = \lim_{s\to 0} s\frac{\Omega}{\Omega^*}\Omega^* = \lim_{s\to 0} s\frac{s\left(k_{P\omega}K_T\right) + k_{I\omega}K_T}{s^3\left(\tau_e J\right) + s^2\left(k_D\tau_e + J\right) + s\left(\alpha_\omega K_T k_{P\omega} + k_D\right) + \alpha_\omega K_T k_{I\omega}}\frac{1}{s} = \frac{1}{\alpha_\omega}$$

$$\lim_{t\to\infty}\Omega\Big|_{\Omega^*=0} = \lim_{s\to 0} s\frac{\Omega}{T_L}T_L = \lim_{s\to 0} s\frac{s\left(\tau_e s + 1\right)}{s^3\left(-J\tau_e\right) + s^2\left(-J - k_D\tau_e\right) + s\left(\alpha_\omega K_T k_{P\omega} - k_D\right) + \alpha_\omega K_T k_{I\omega}}\frac{1}{s} = 0$$

Thus, it is possible to conclude that when steady state is reached, the machine speed is related to the reference speed by a constant gain, α_ω, the velocity measurement gain, while being robust to a step variation of the load torque.

To compute the PI controller gains, the symmetrical optimum criteria (with a=2) is used. In this case the denominator coefficients should obey the following rule:

$$b_k^2 = a b_{k-1} b_{k+1}$$

Thus, it results in a system of two equations that is solved in order to the controller gains:

$$\begin{cases} b_2^2 = a b_1 b_3 \\ b_1^2 = a b_0 b_2 \end{cases} \Leftrightarrow \begin{cases} \left(k_D\tau_e + J\right)^2 = a\left(\alpha_\omega K_T k_{P\omega} + k_D\right)\left(\tau_e J\right) \\ \left(\alpha_\omega K_T k_{P\omega} + k_D\right)^2 = a\left(\alpha_\omega K_T k_{I\omega}\right)\left(k_D\tau_e + J\right) \end{cases} \Leftrightarrow \begin{cases} k_{P\omega} = \dfrac{J^2 + 4Jk_D\tau_e + k_D^2\tau_e^2}{2\alpha J K_T \tau_e} \\ k_{I\omega} = \dfrac{\left(J + k_D\tau_e\right)^3}{8\alpha J^2 K_T \tau_e^2} \end{cases}$$

d axis **Current Control Loop**

Similarly to the speed control loop, the PI controller transfer function is given by:

$$\frac{V_d^*}{E_d} = \frac{sk_{Pd} + k_{Id}}{s}$$

The reference voltage computed by the PI controller is not immediately applied to the machine, because the controller, SVM, deadtimes and semiconductors switching dynamics introduce a delay, let us call it τ_u. For generality, let us assume that the SVM method also introduces the gain K_u. The transfer function that models this behavior is given by:

$$\frac{V_d}{V_d^*} = \frac{K_u}{1 + s\tau_u}$$

The electrical dynamics of the *d* axis was introduced in section 3.1. Note that the electromotive force from the opposite axis is considered as a perturbation. Thus, the *d* axis transfer function is given by:

$$\frac{I_d}{V_d + \Omega_e L_q I_q} = \frac{1}{sL_d + r_s}$$

For generality, let us define α_d as the *d* axis current measurement gain. The resulting block diagram is given in Fig. A.3.

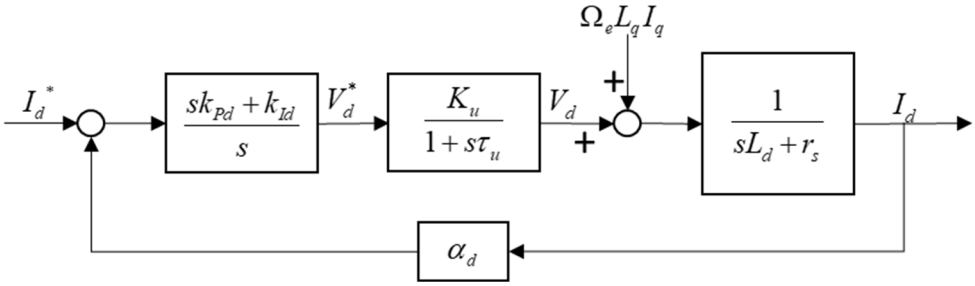


Fig A.3. Block diagram of the *d* axis current control loop.

This block diagram has the same structure as the block diagram obtained for the speed control loop. Thus, the same approach could be utilized. However, better results were obtained by using the zero of the PI controller to cancel the pole of the electrical dynamics and by tunning the controller gains using the ITAE criteria.

By using the PI controller zero to cancel the *d* axis electrical dynamic pole, the following relation appears:

$$s\frac{k_{Pd}}{k_{Id}} + 1 = s\frac{L_d}{r_s} + 1 \quad \Rightarrow \quad k_{Pd} = \frac{L_d}{r_s} k_{Id}$$

The Closed loop transfer function (I_d / I_d^*) becomes:

$$\frac{I_d}{I_d^*} = \frac{\frac{K_u k_{Id}}{r_s \tau_u}}{s^2 + s\left(\frac{1}{\tau_u}\right) + \frac{\alpha_d K_u k_{Id}}{r_s \tau_u}}$$

By comparing the obtained closed loop transfer function to the 2nd Order Systems Characteristic Equation, and setting the ITAE criteria damping ratio ($\xi = \sqrt{2}/2$) in combination with the

relation obtained by using the PI controller zero to cancel de *d* axis electric dynamics pole, it is possible to compute the controller gains:

$$\begin{cases} s^2 + s\left(\frac{1}{\tau_u}\right) + \frac{\alpha_d K_u k_{Id}}{r_s \tau_u} = s^2 + s\left(2\xi\omega_0\right) + \omega_0^2 \\ \xi = \sqrt{2}/2 \\ k_{Pd} = \frac{L_d}{r_s} k_{Id} \end{cases} \Rightarrow \begin{cases} k_{Id} = \frac{r_s}{2\tau_u K_u} \\ k_{Pd} = \frac{L_d}{2\tau_u K_u} \end{cases}$$

To improve the robustness of the controller in respect to the perturbation introduced by the electromotive force term, a cross term is added to the output of the PI to cancel the term depending on Ω_e. Thus, the PI output is given by:

$$V_d^* = \frac{sk_{Pd} + k_{Id}}{s} E_d - \frac{\Omega_e L_q I_q}{K_u}$$

<u>*q axis* Current Control Loop</u>

Identically to the *d* axis and speed PI controller transfer functions, swapping the indexes, the *q* axis PI controller transfer function is given by:

$$\frac{V_q^*}{E_q} = \frac{sk_{Pq} + k_{Iq}}{s}$$

The transfer function that considers the delay introduced by the controller, SVM, deadtimes and semiconductors switching dynamics is the identical, given by:

$$\frac{V_q}{V_q^*} = \frac{K_u}{1 + s\tau_u}$$

The electrical dynamics of the *q* axis current is given by:

$$\frac{I_q}{V_q - \Omega_e L_d I_d} = \frac{1}{sL_q + r_s}$$

Again, let us define α_q as the *q* axis current measurement gain. The resulting block diagram if shown in Fig. A.4.

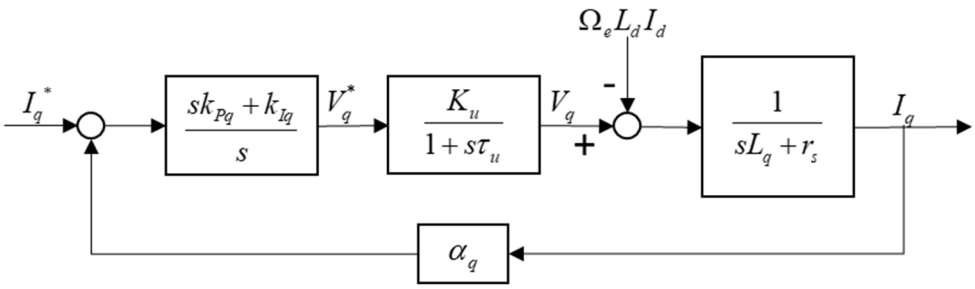


Fig A.4. Block diagram of the *q* axis current control loop.

The exact same approach used to tune the gains of the *d* axis can be utilized to tune the PI controller gains in the *q* axis, resulting in the gains given by:

$$\begin{cases} k_{Iq} = \dfrac{r_s}{2\tau_u K_u} \\ k_{Pq} = \dfrac{L_q}{2\tau_u K_u} \end{cases}$$

Similarly to the *d* axis, to improve the robustness of the controller in respect to the perturbation introduced by the electromotive force term, a cross term is added to the output of the PI to cancel the term depending on Ω_e. Thus, the PI output is given by:

$$V_q^* = \frac{sk_{Pq}+k_{Iq}}{s} E_q + \frac{\Omega_e L_d I_d}{K_u}$$

Gains Computation

The controller gains have been computed as function of the system parameters. In some cases, these parameters can be measured or estimated such as the case of parameters r_s, L_d, L_q, J and k_D. In other cases, such as τ_e and τ_u this is not possible.

Let us focus on τ_u first. This is the delay introduced by the control loops running in the FPGA (acquisition, controllers, SVM), the deadtimes and the semiconductors switching dynamics. This results in a sequence of delays in the form:

$$\frac{1}{(s\tau_{acquisition}+1)} \frac{1}{(s\tau_{controller}+1)} \frac{K_u}{(s\tau_{SVM}+1)} \frac{1}{(s\tau_{deadtimes}+1)} \frac{1}{(s\tau_{switching}+1)}$$

After expansion, a 5th order transfer function is obtained. It is typical to disregard the higher order terms, and to keep only the 1st order term:

$$\frac{1}{\left(s\tau_{acquisition}+1\right)}\frac{1}{\left(s\tau_{controller}+1\right)}\frac{K_u}{\left(s\tau_{SVM}+1\right)}\frac{1}{\left(s\tau_{deadtimes}+1\right)}\frac{1}{\left(s\tau_{switching}+1\right)}\cong\frac{K_u}{\left(s\tau_u+1\right)}$$

Where τ_u is the sum of all the delays considered:

$$\tau_u=\tau_{acquisition}+\tau_{controller}+\tau_{SVM}+\tau_{deadtimes}+\tau_{switching}$$

For this reason, τ_u was considered to be 6 times the switching period. Also, the implemented SVM has unitary gain (K_u=1).

At this point the system is capable of controlling currents. As indicated above, the time constant τ_e depends on the performance of the current control loops. This was assessed in simulation, where it was concluded that the developed torque would take 2ms to converge after a step in the reference torque (τ_e=2ms).

Lastly, all the measurement gains are unitary just like the torque gain introduced above (K_T=1). This resulted in the controller gains provided in Table 4.2.

APPENDIX B

SIGNAL ACQUISITION BOARD

B1. Top Schematic

Fig B.1. Signal Acquisition Board Top Schematic.

B2. Current Sensing Schematic

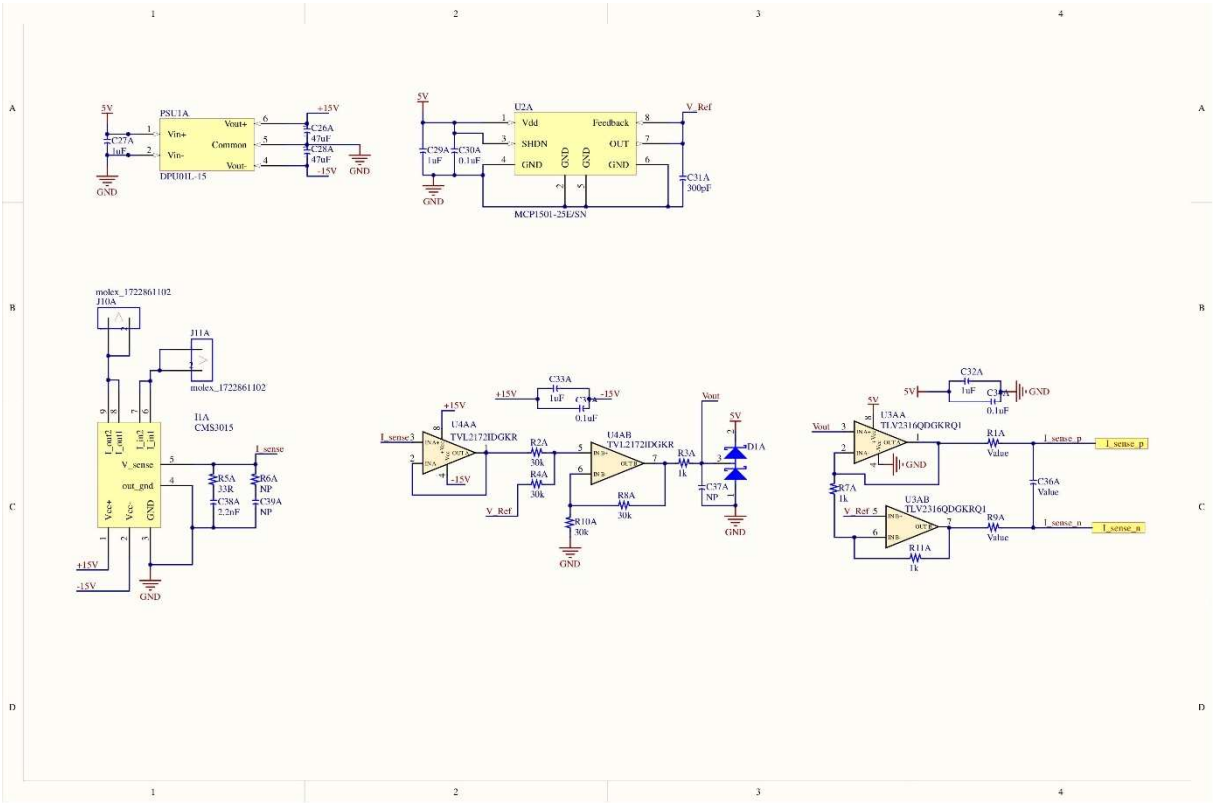


Fig B.2. Signal Acquisition Board Current Sensing Schematic.

B3. Voltage Sensing Schematic

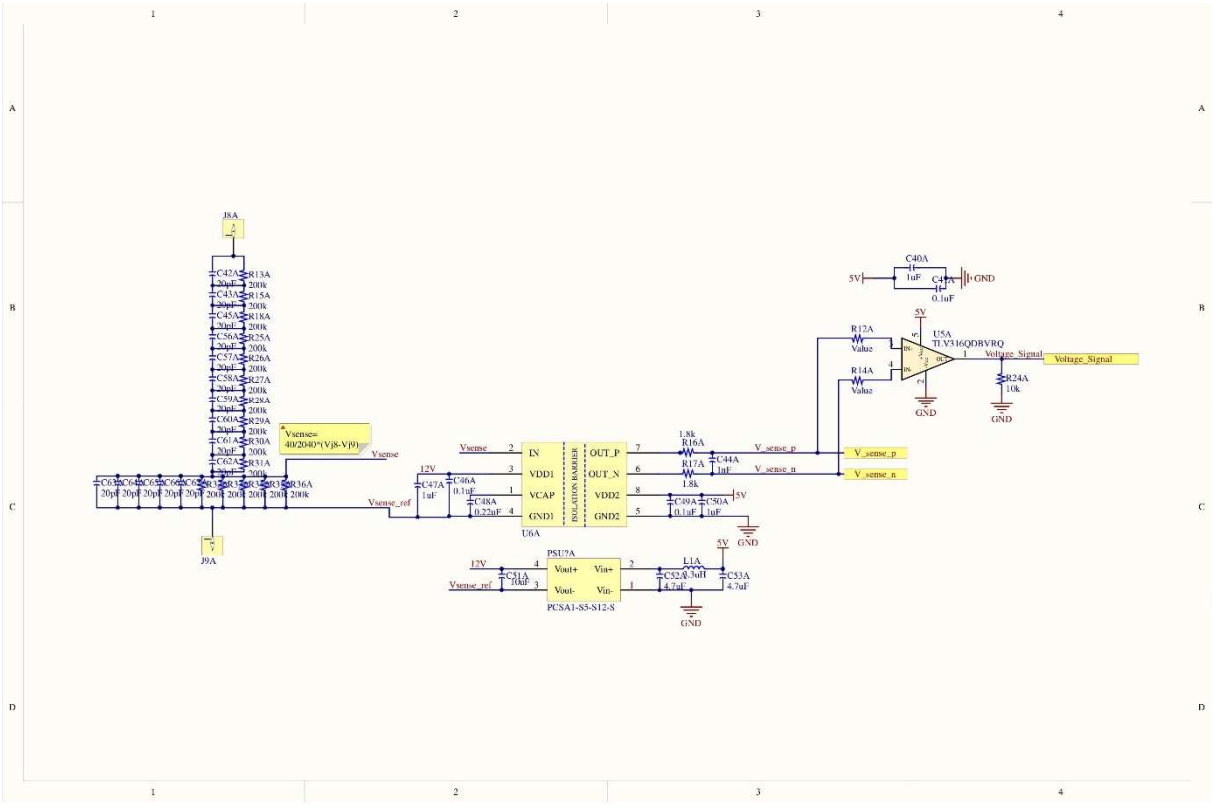


Fig B.3. Signal Acquisition Board Voltage Sensing Schematic.

B4. Analog to Digital Converters

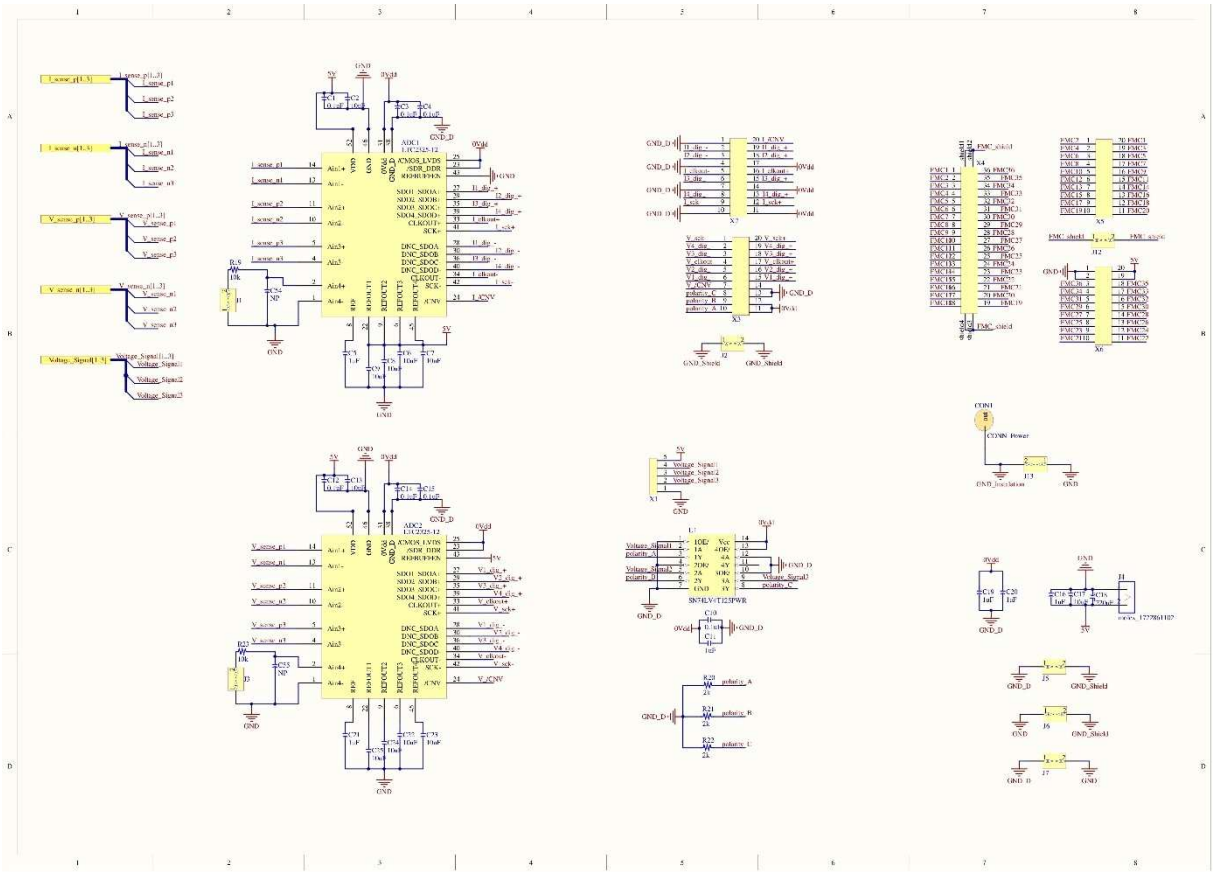
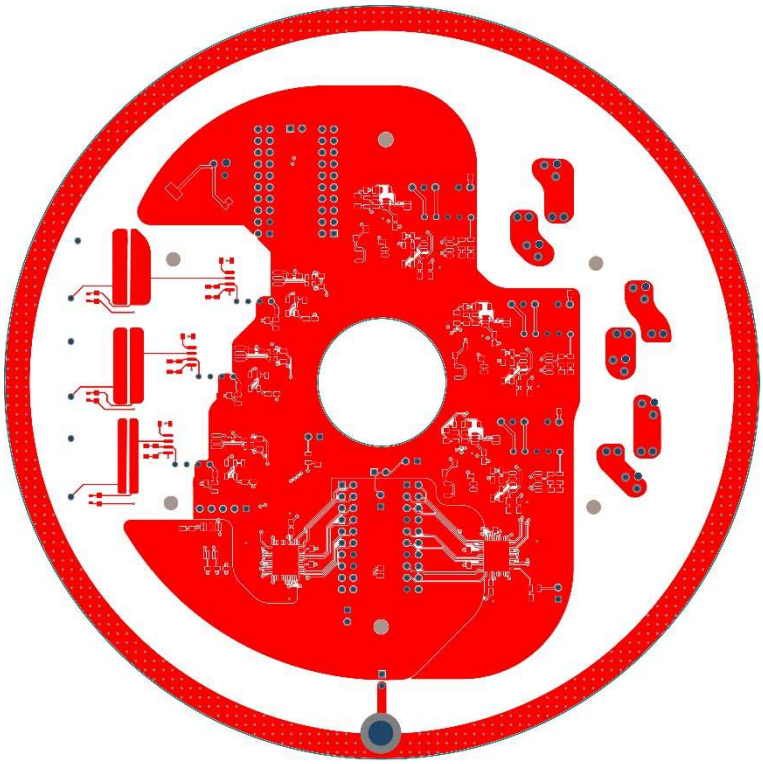
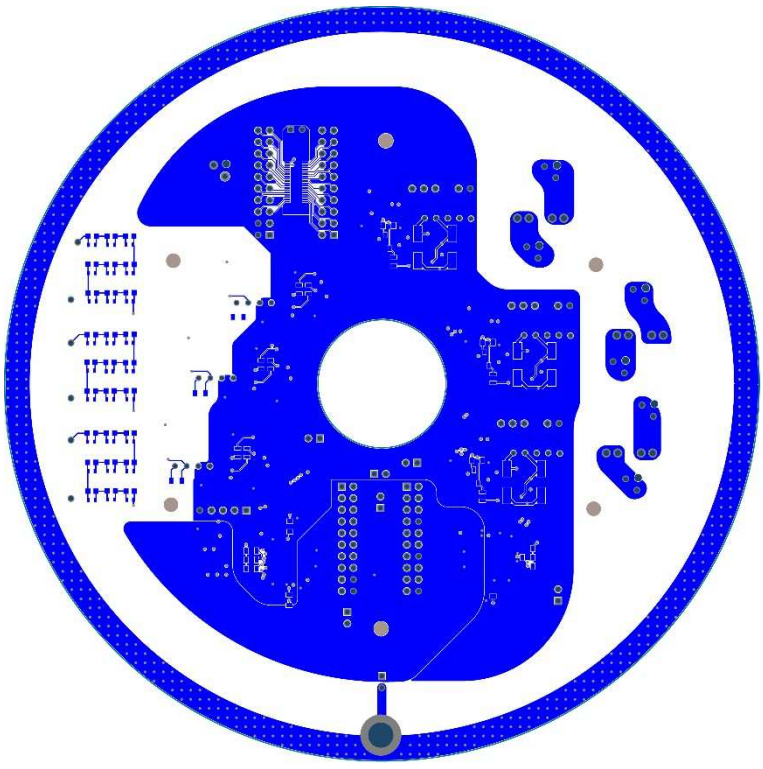


Fig B.4. Signal Acquisition Board Analog to Digital Converters Schematic.

B5. Printed Circuit Board Copper Layers

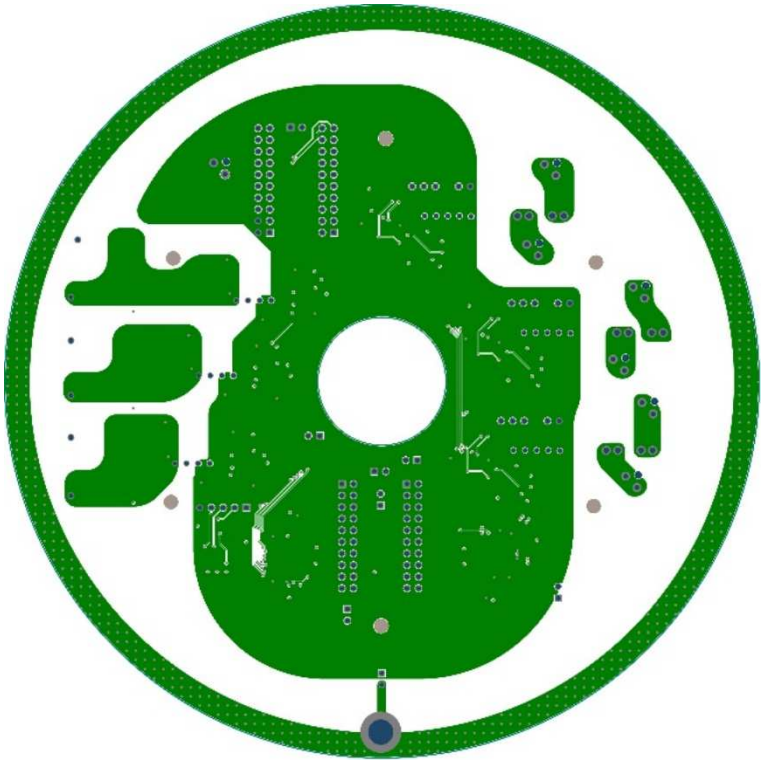


(a)

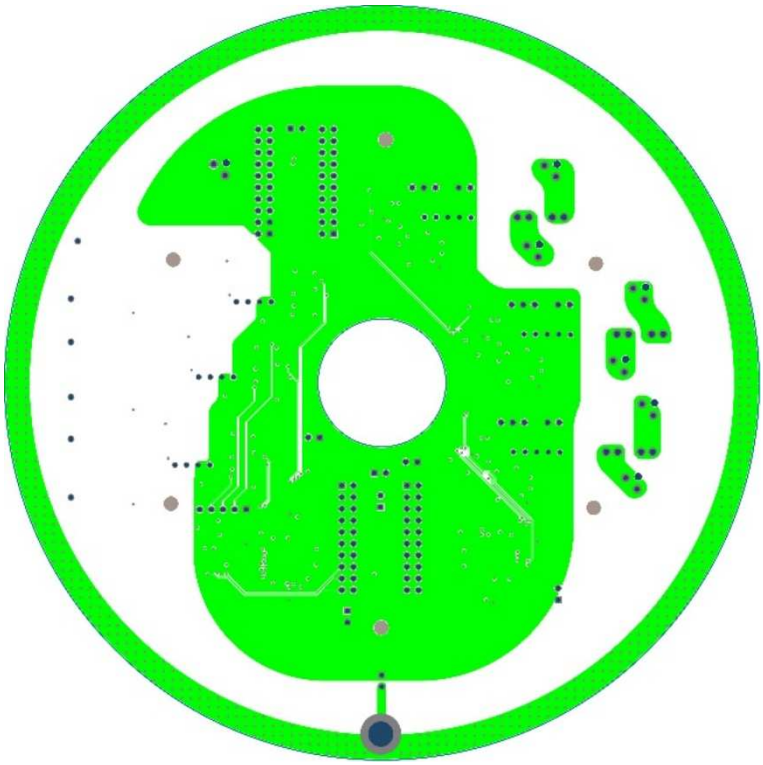


(b)

Fig B.5. Signal Acquisition Board external copper layers. (a) Top layer. (b) Bottom layer.



(a)



(b)

Fig B.6. Signal Acquisition Board internal copper layers. (a) Top inner layer. (b) Bottom inner layer.

APPENDIX C

DUAL VOLTAGE SOURCE INVERTER BOARD

C1. Top Schematic

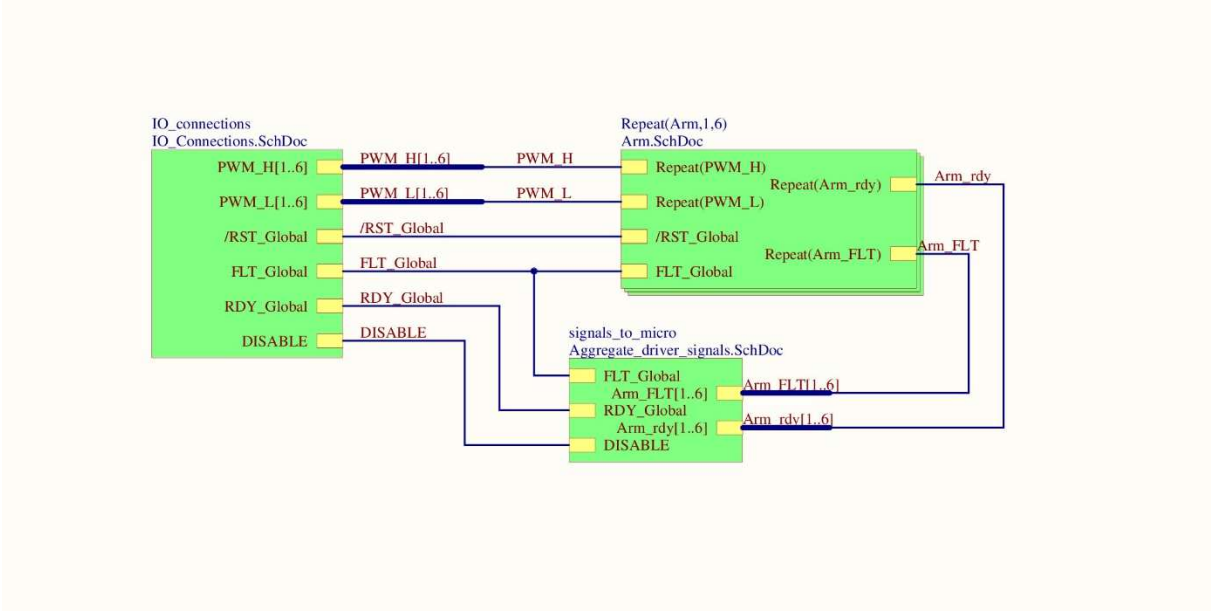


Fig C.1. Dual Voltage Source Inverter Top Schematic.

C2. GaN Arm Schematic

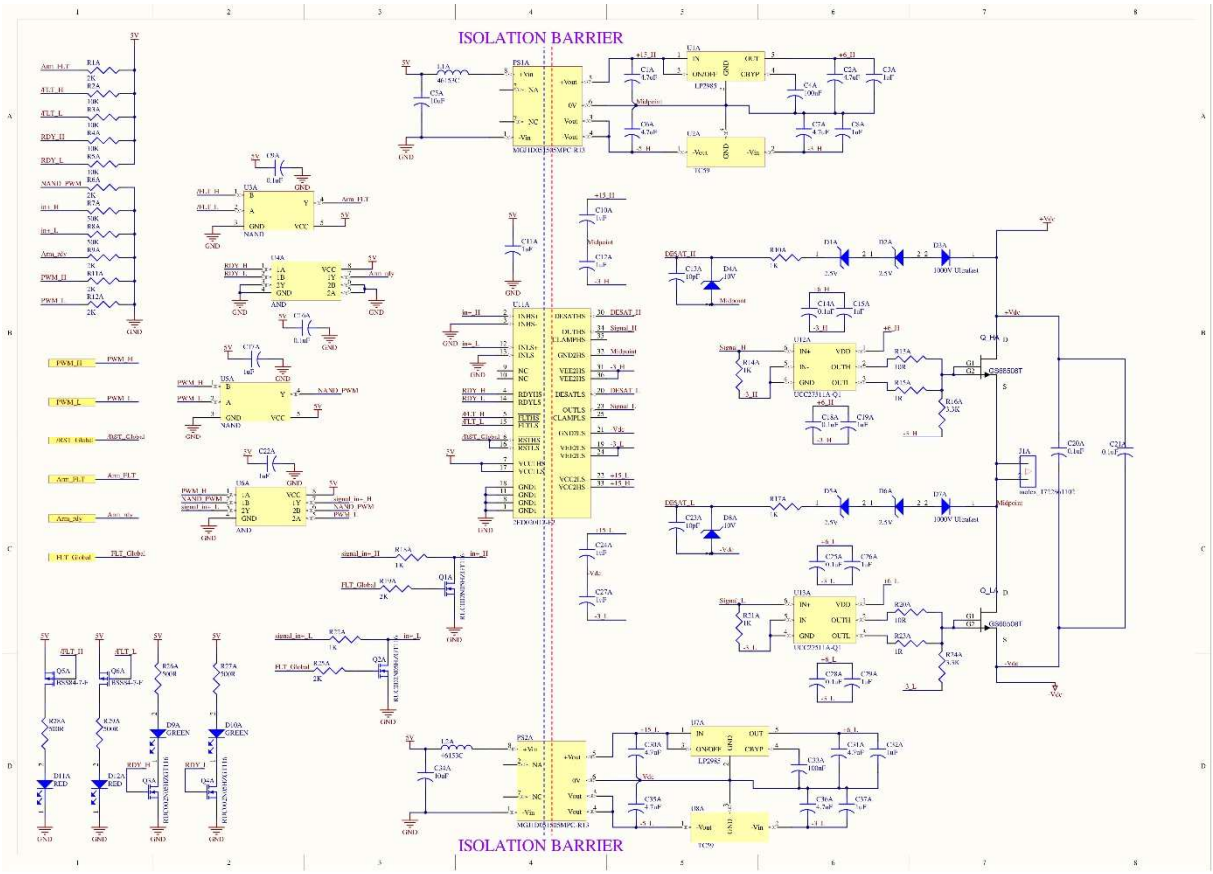


Fig C.2. Dual Voltage Source Inverter GaN Arm schematic.

C3. Aggregation of Driver Signals Schematic

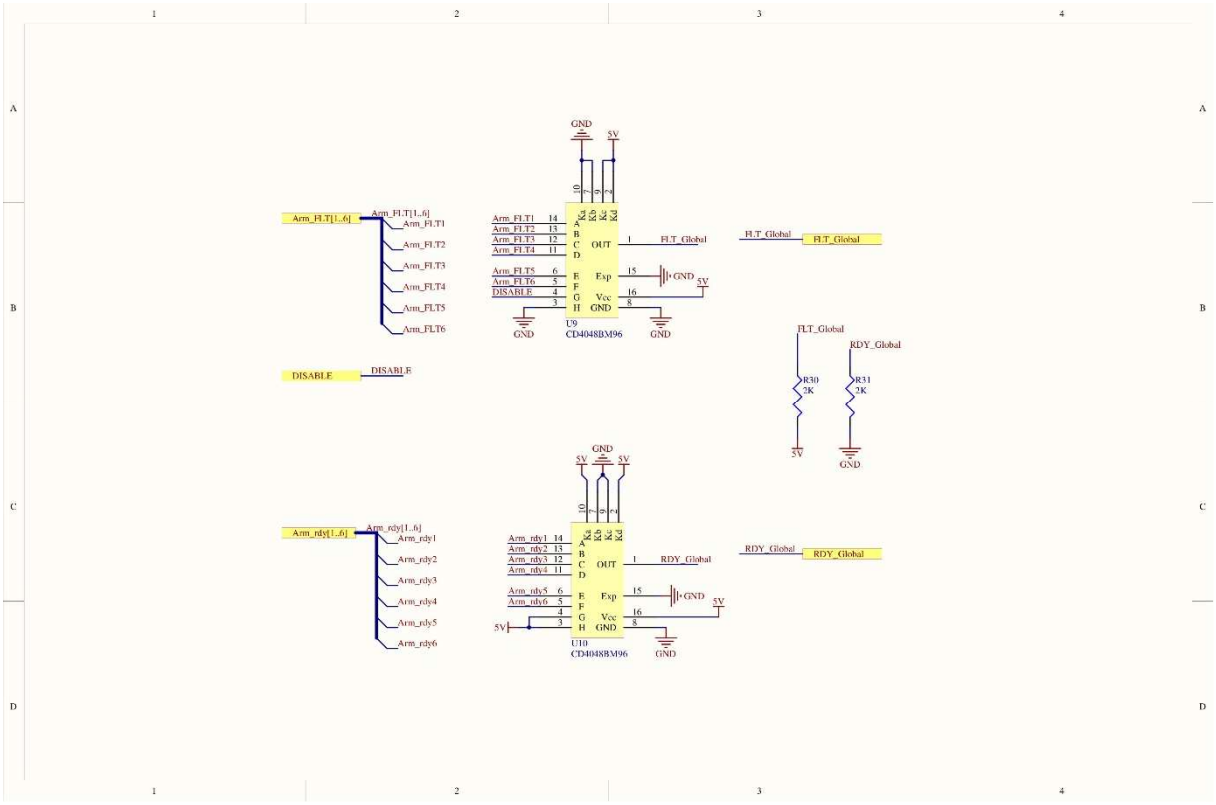


Fig C.3. Dual Voltage Source Inverter aggregation of driver signals schematic.

C4. I/O Schematic

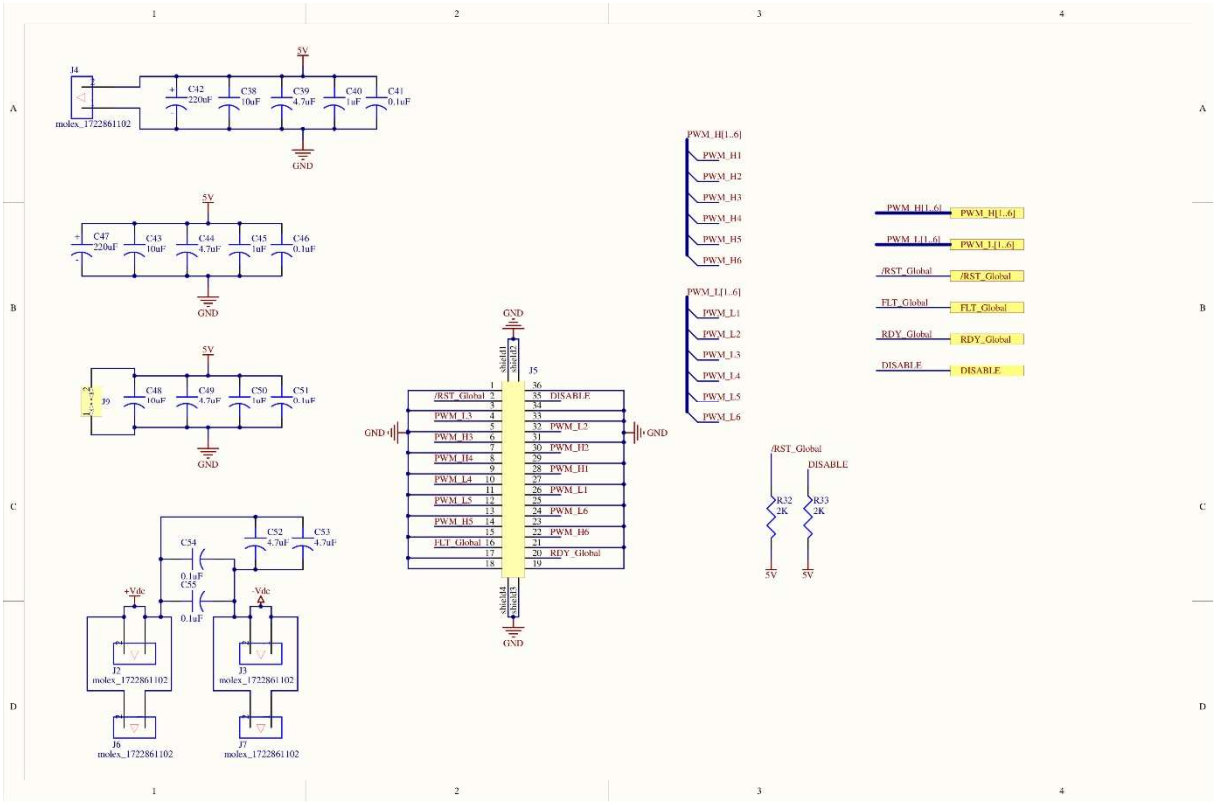
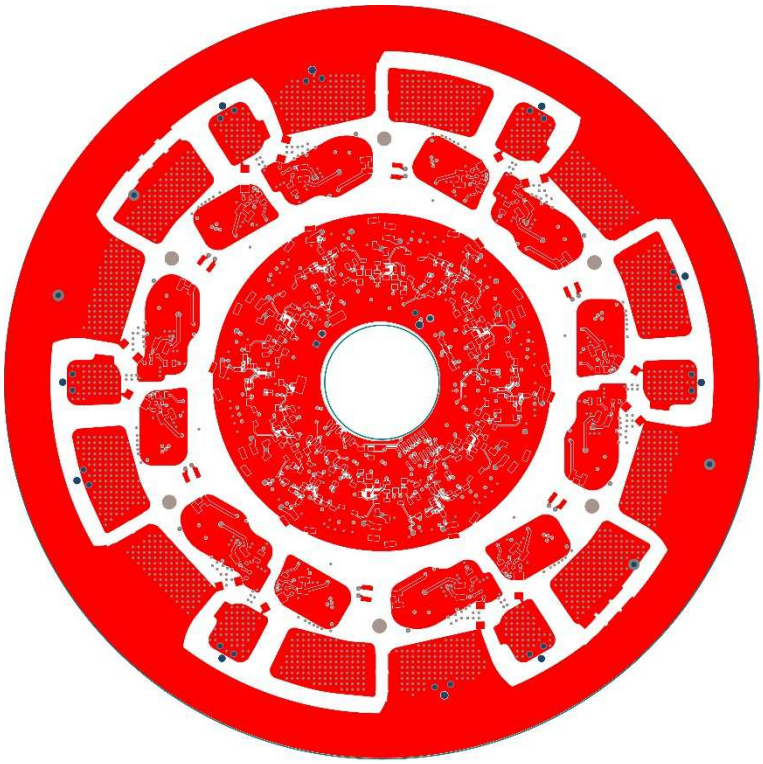
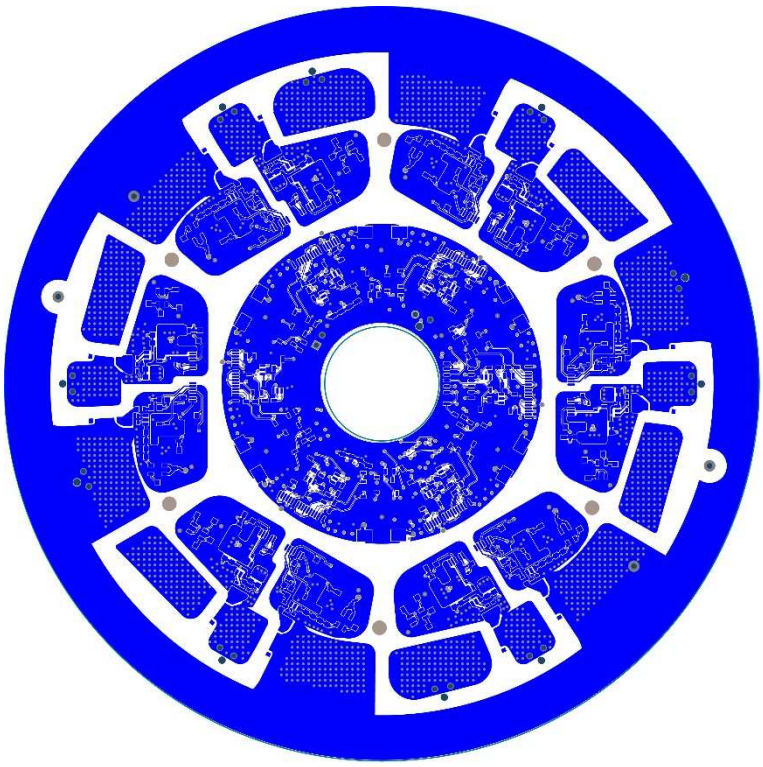


Fig C.4. Dual Voltage Source Inverter I/O schematic.

C5. Printed Circuit Board Copper Layers

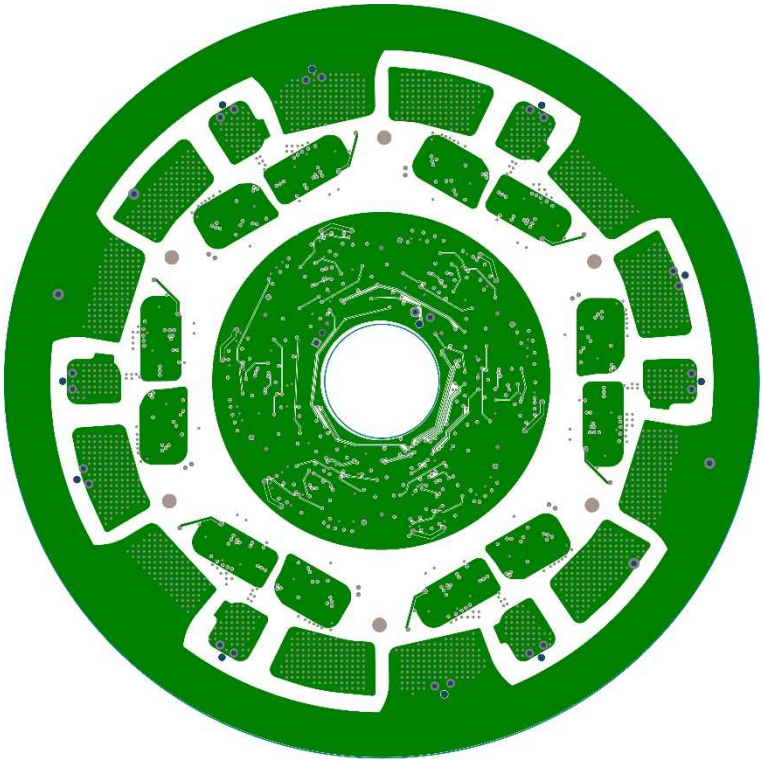


(a)

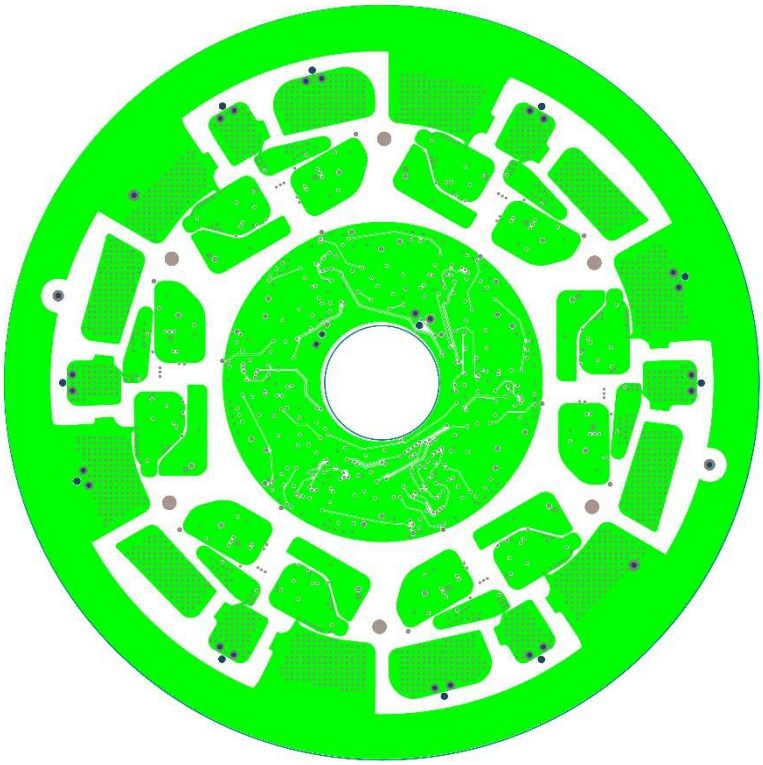


(b)

Fig C.5. Dual Voltage Source Inverter external copper layers. (a) Top layer. (b) Bottom layer.



(a)



(b)

Fig C.6. Dual Voltage Source Inverter internal copper layers. (a) Top inner layer. (b) Bottom inner layer.

APPENDIX D

CURRENT SOURCE RECTIFIER BOARD

D1. Top Schematic

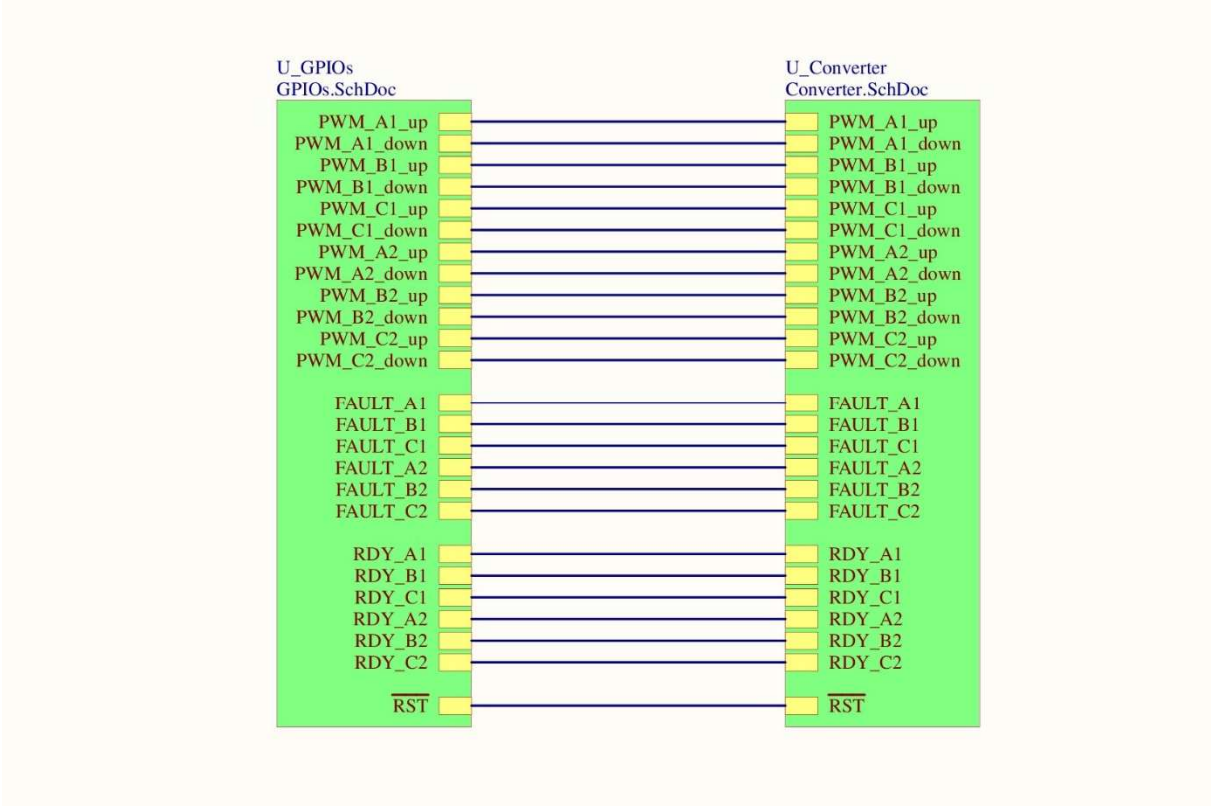


Fig D.1. Current Source Rectifier Top Schematic.

D2. Current Source Rectifier Schematic

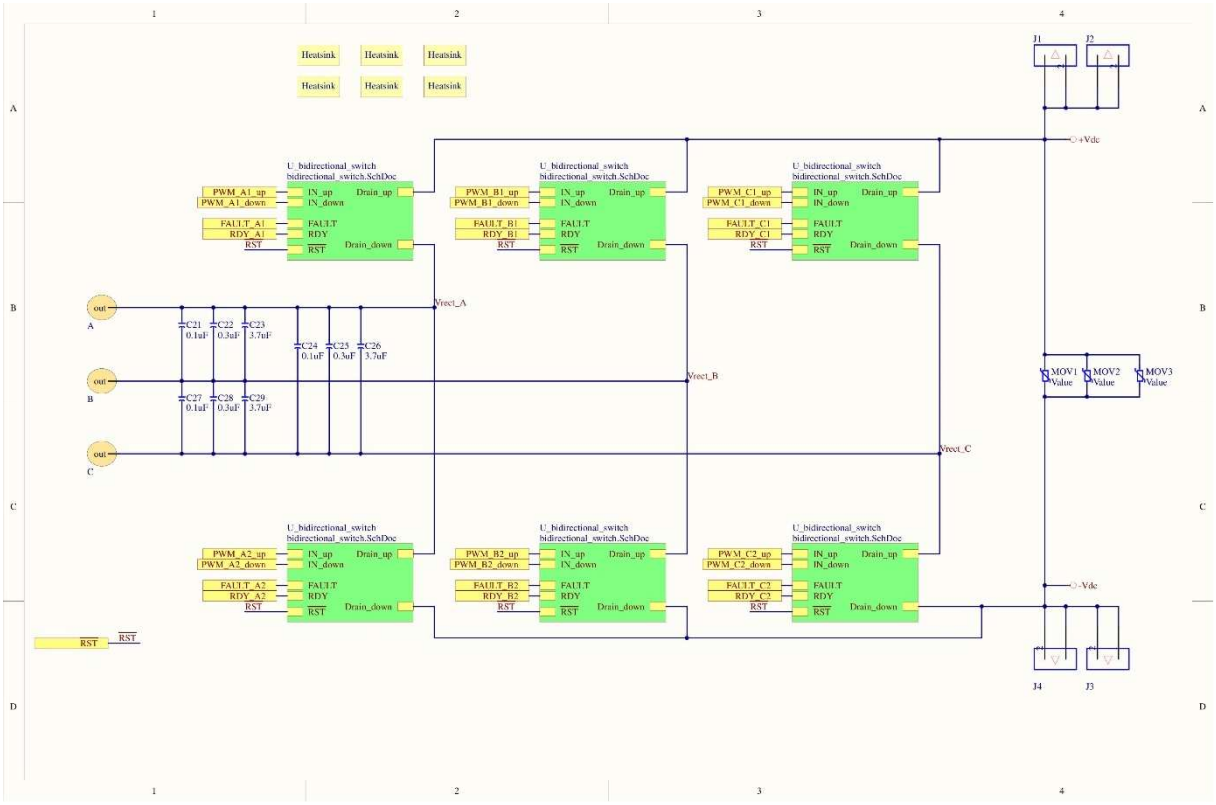


Fig D.2. Current Source Rectifier Converter schematic.

D3. Bidirectional Switch Schematic

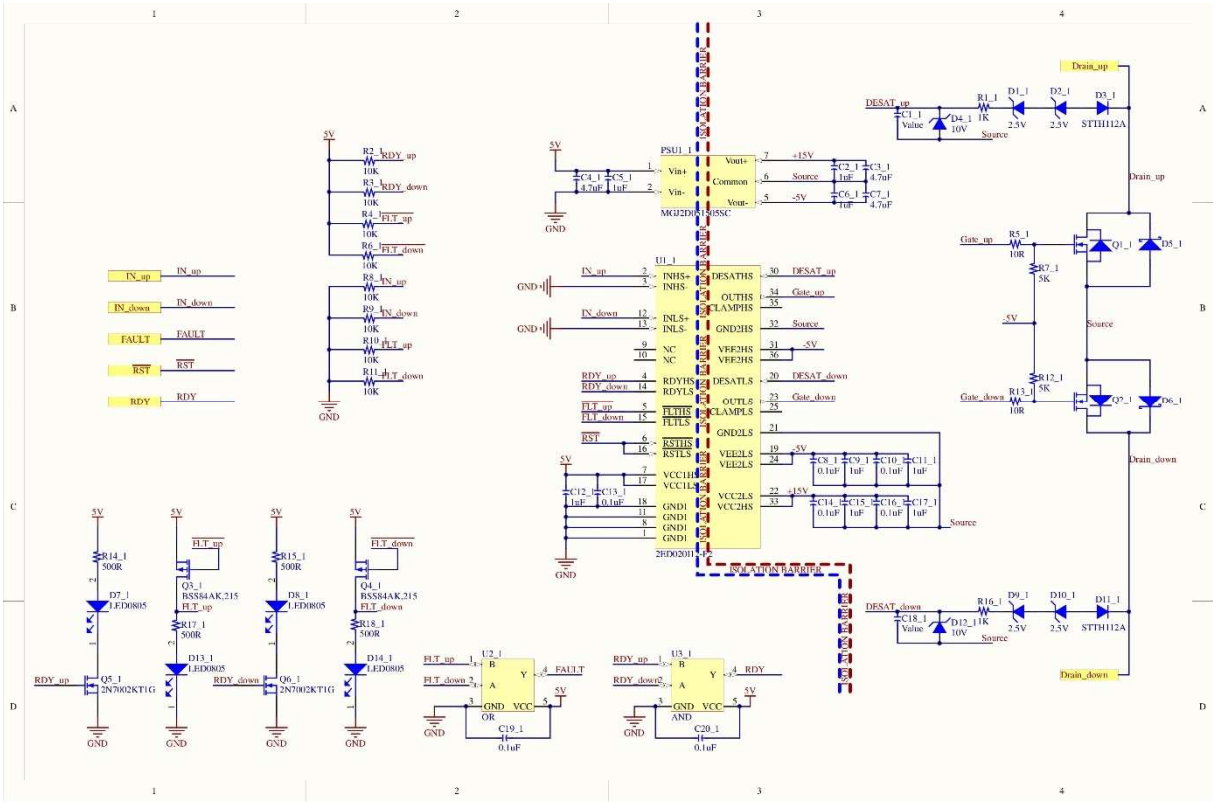


Fig D.3. Current Source Rectifier Bidirectional Switch Schematic.

D4. I/O Schematic

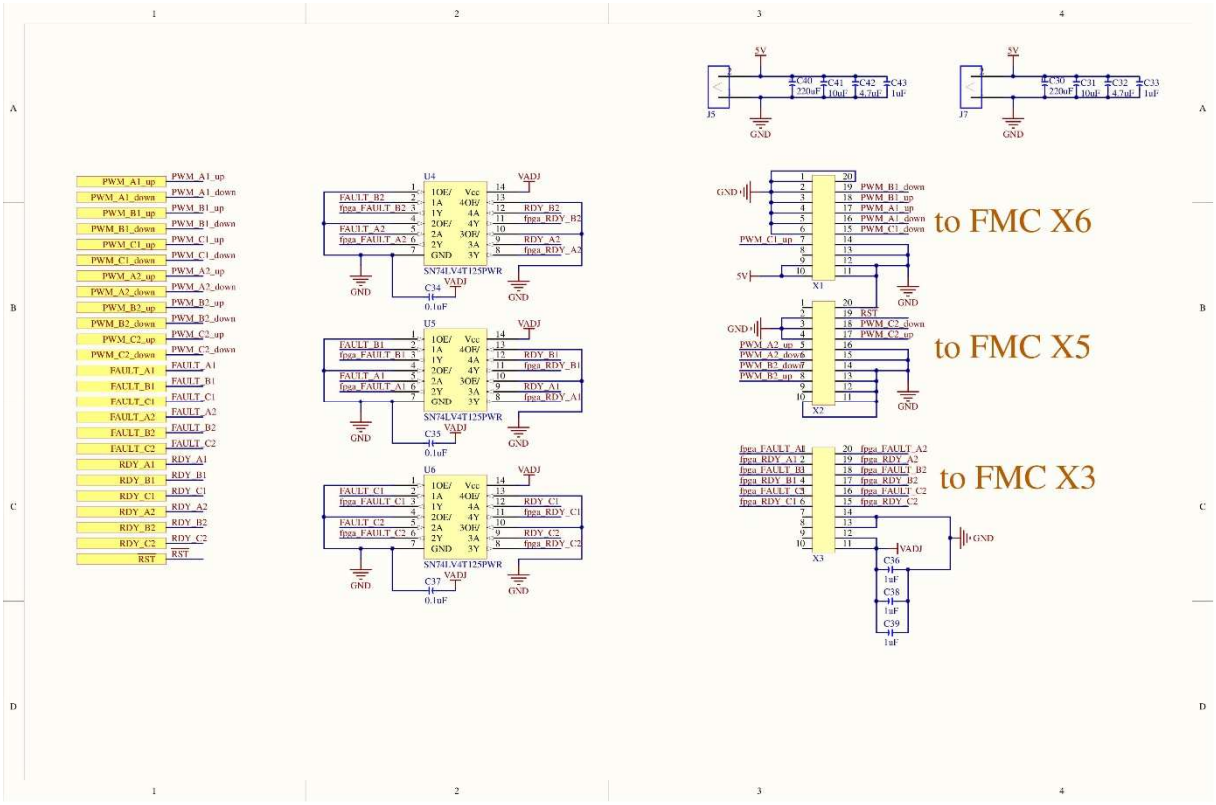
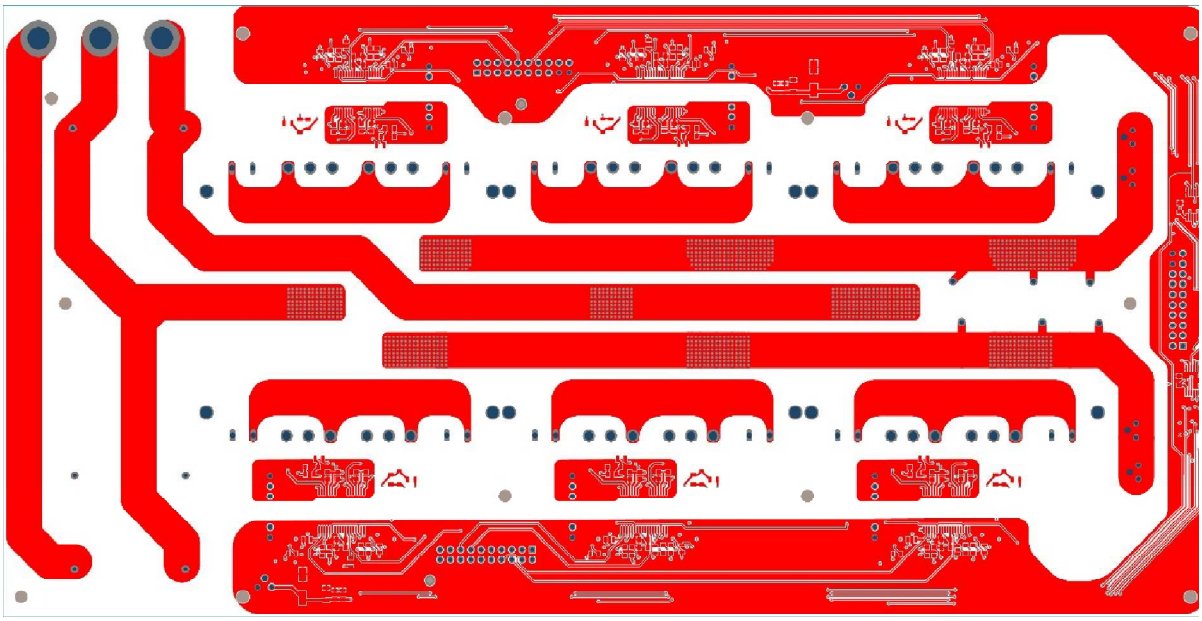
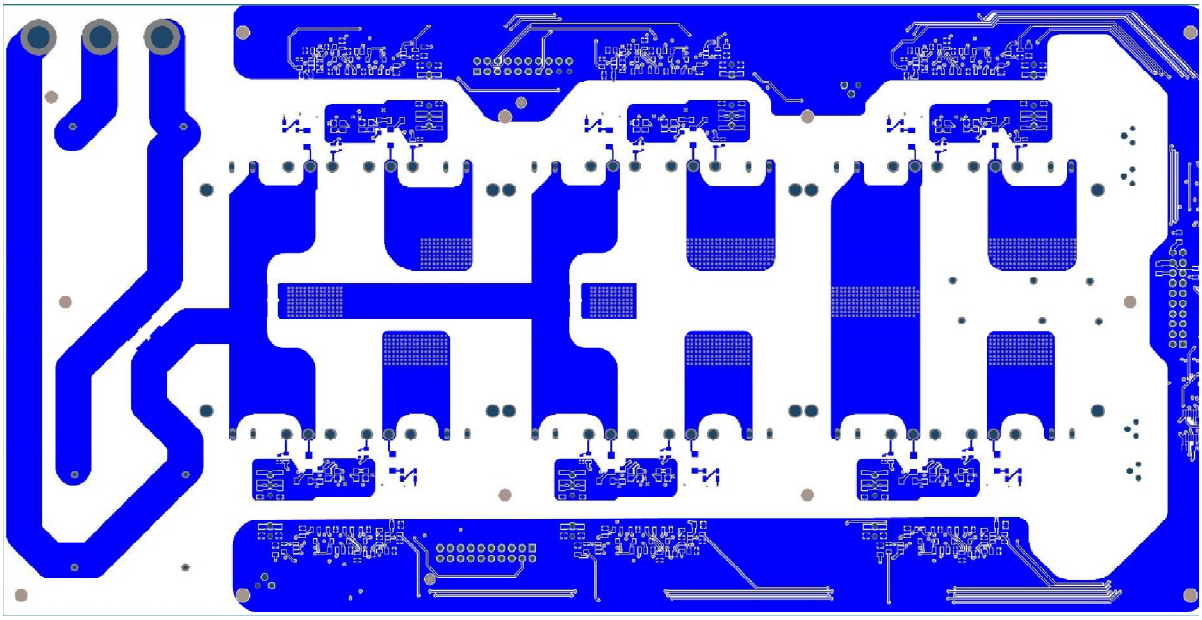


Fig D.4. Current Source Rectifier I/O schematic.

D5. Printed Circuit Board Copper Layers

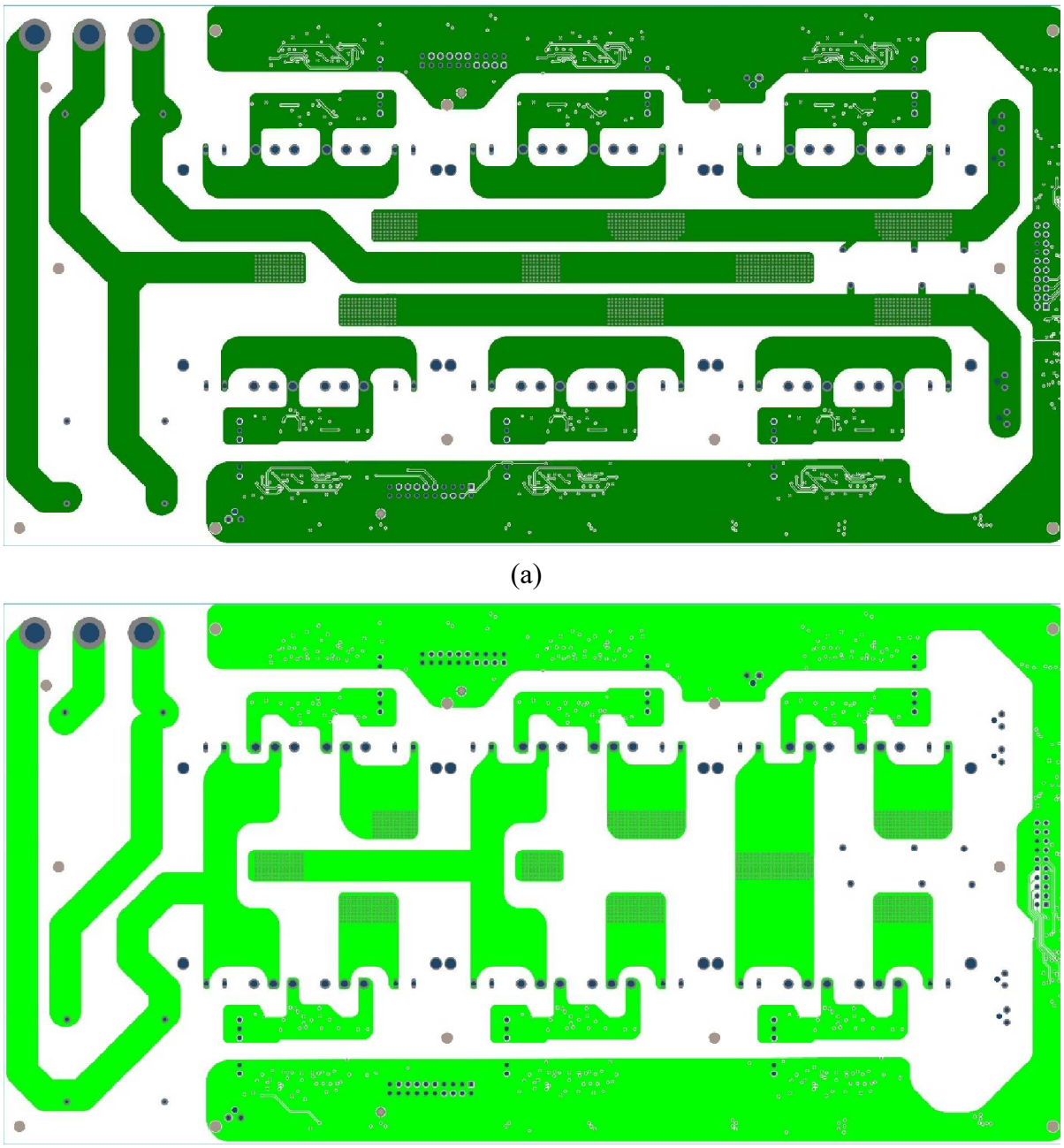


(a)



(b)

Fig D.5. Current Source Rectifier external copper layers. (a) Top layer. (b) Bottom layer.



(a)

(b)

Fig D.6. Current Source Rectifier internal copper layers. (a) Top inner layer. (b) Bottom inner layer.

APPENDIX E

FMC BOARD

E1. Top Schematic

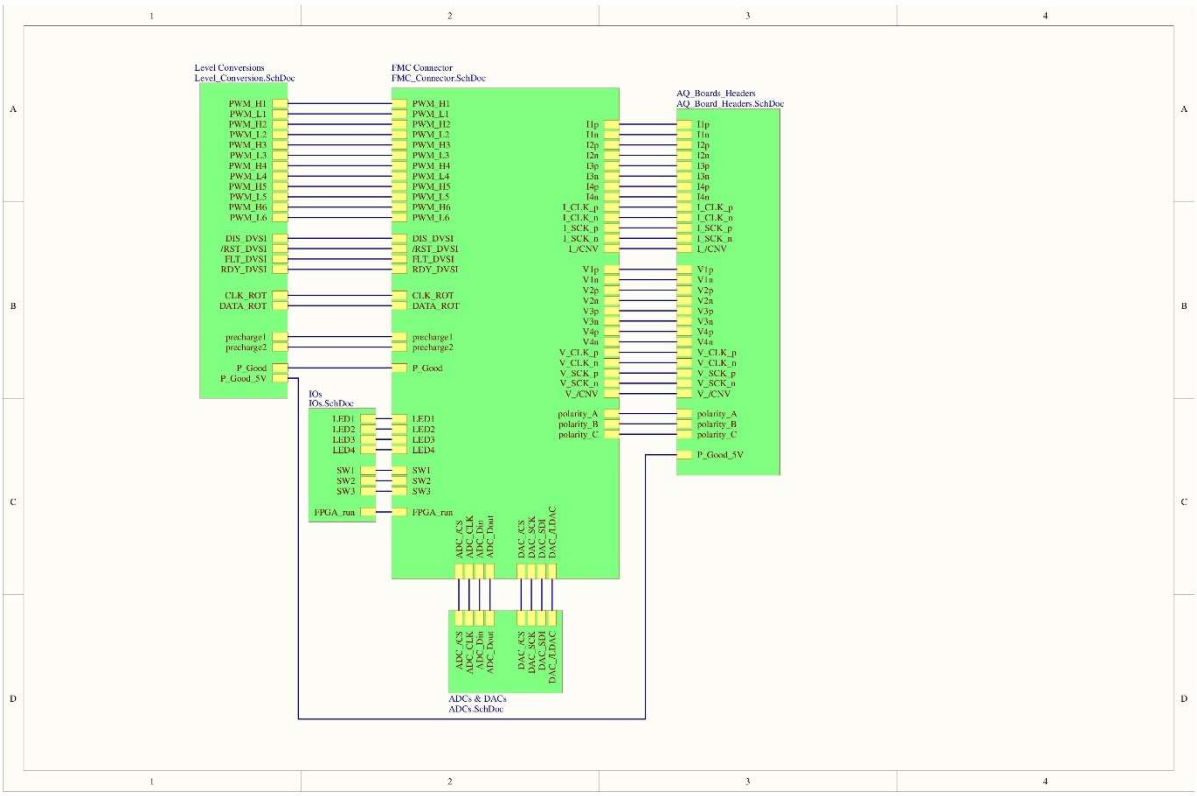


Fig E.1. FMC Board Top schematic.

E2. FMC Connector Schematic

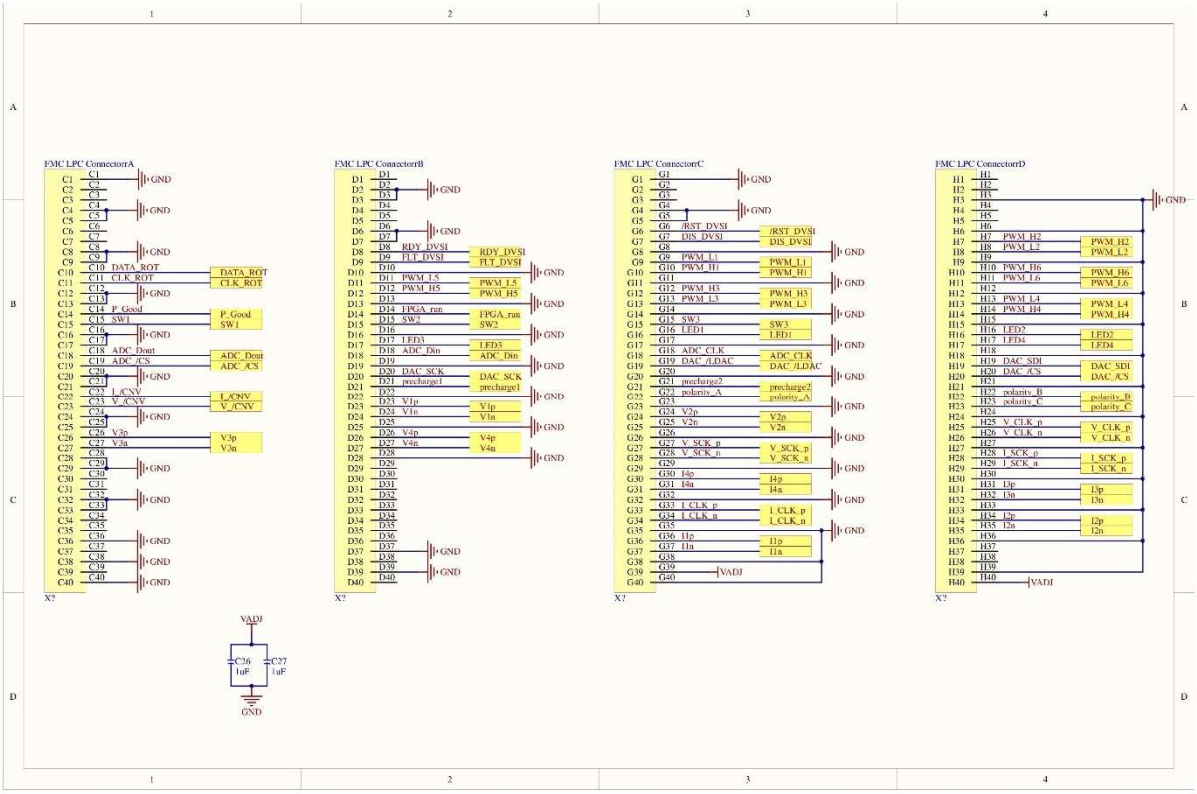


Fig E.2. FMC Board – FMC connector schematic.

E3. Power Supply and Acquisition Board I/O Schematic

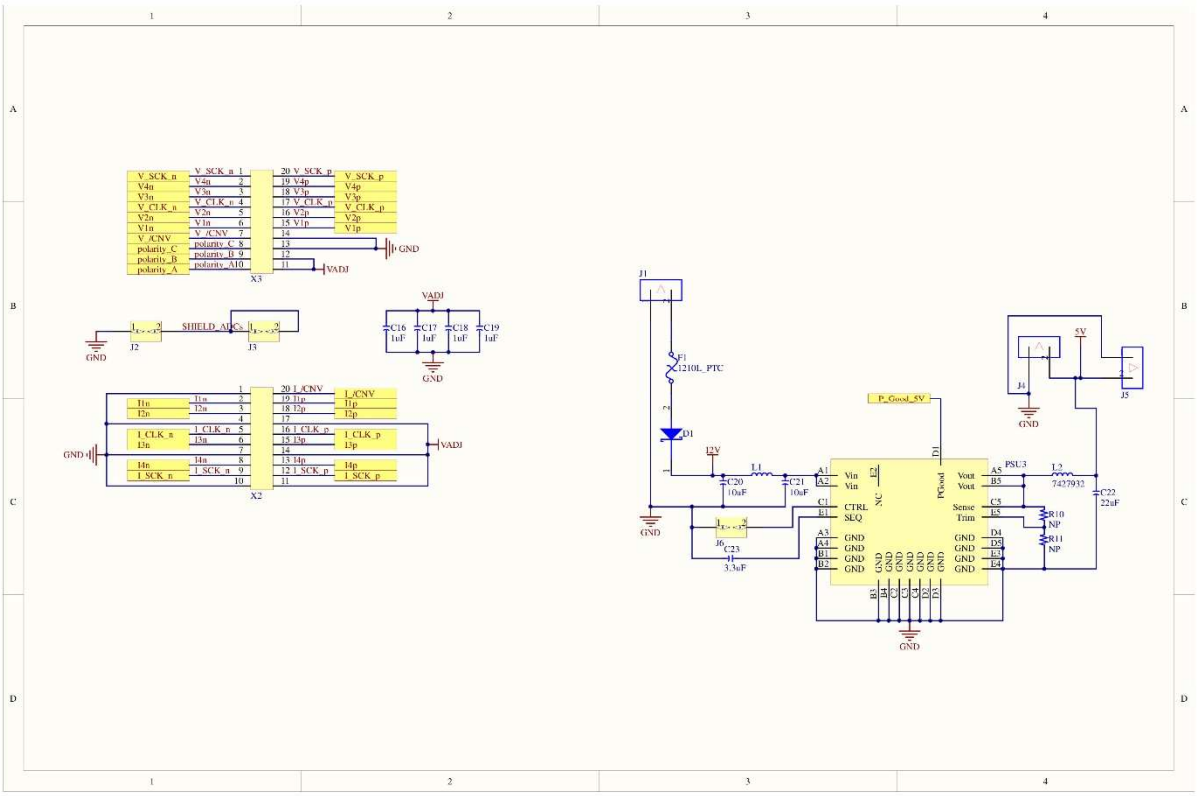


Fig E.3. FMC Board Power supply and Acquisition board I/O schematic.

E4. Level Conversion and DVSI I/O Schematic

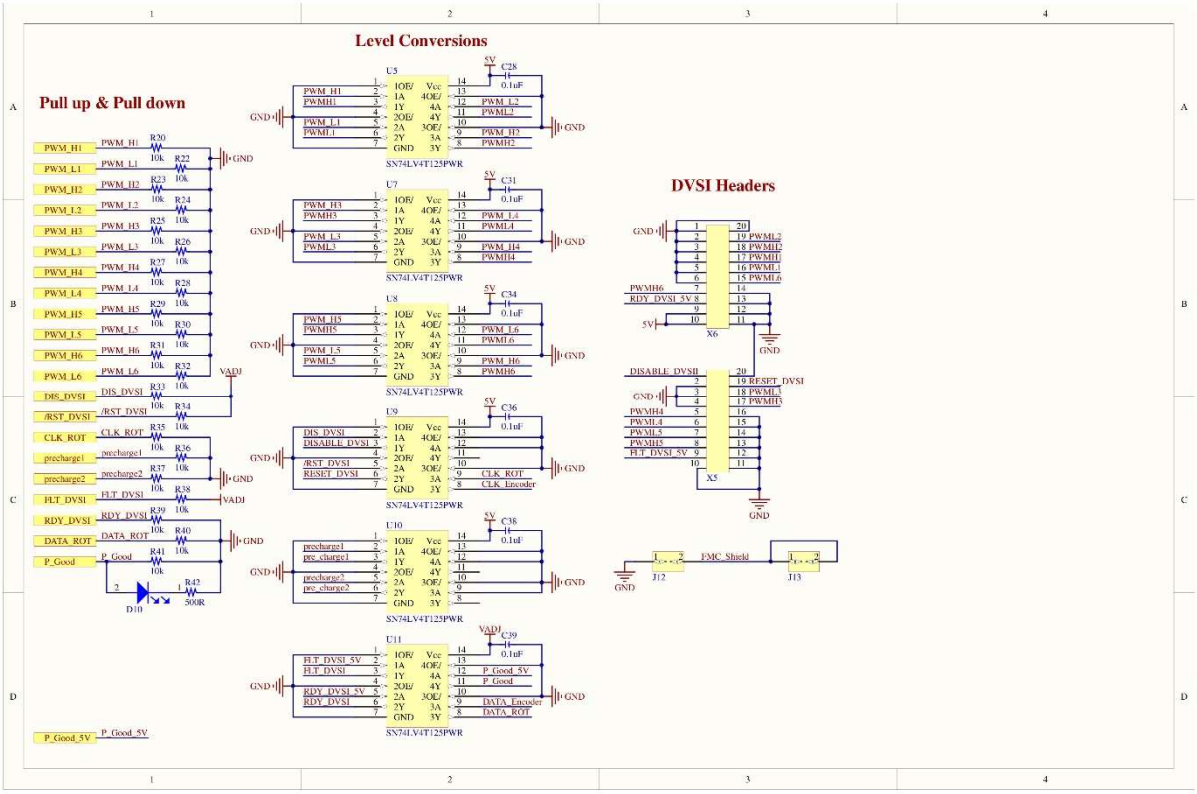


Fig E.4. FMC Board level conversion and DVSI I/O schematic.

E5. ADCs and DACs Schematic

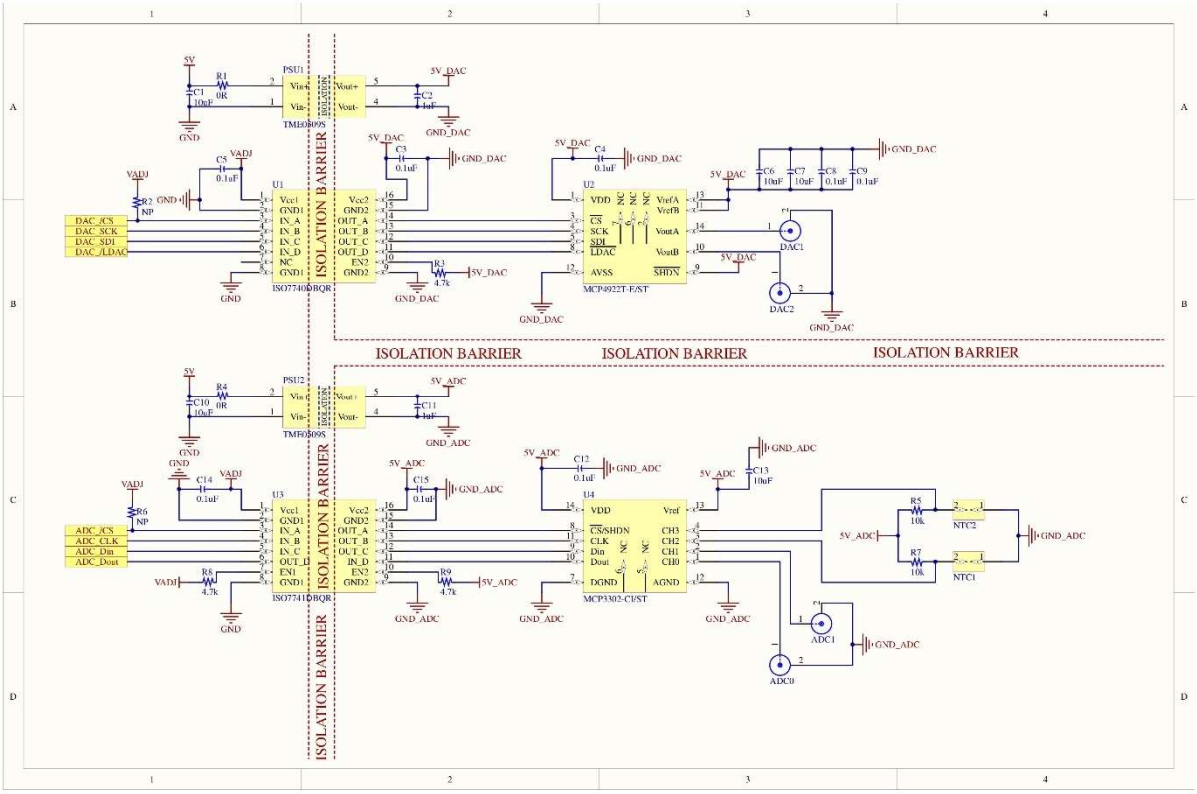


Fig E.5. FMC Board ADCs and DACs schematic.

E6. LEDs and Switches for User Interface Schematic

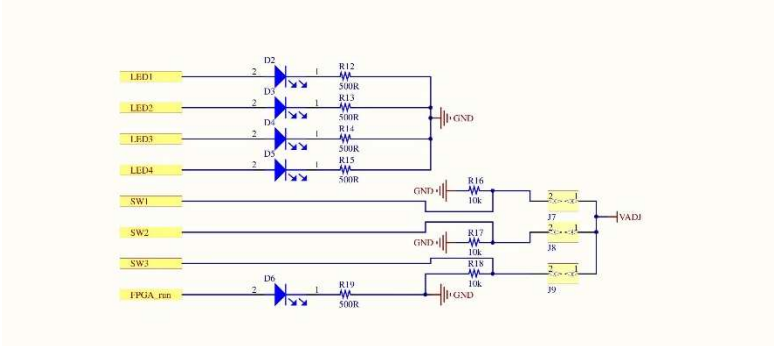
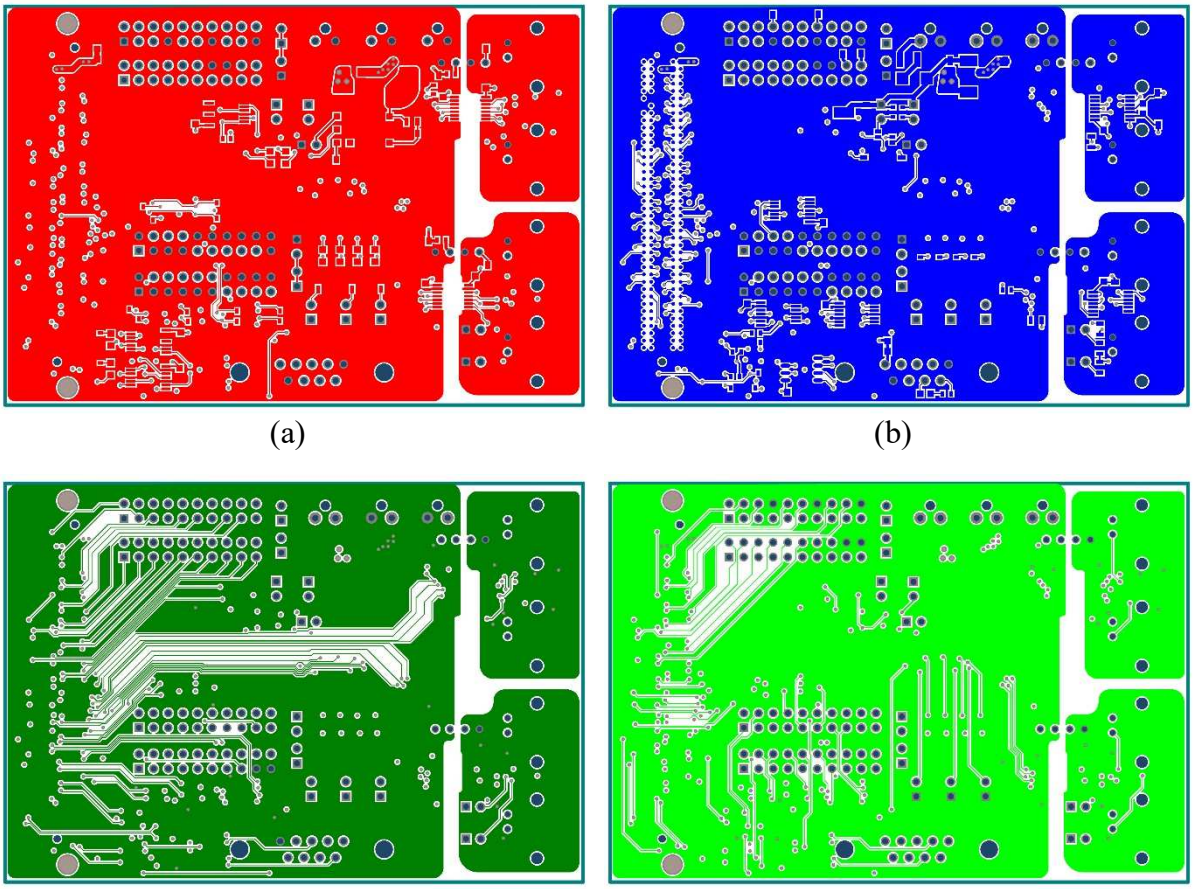


Fig E.6. FMC Board LEDs and switches for user interface schematic.

E7. Printed Circuit Board Copper Layers



(a) (b)

(c) (d)

Fig E.7. FMC Board copper layers. (a) Top external layer. (b) Bottom external layer. (c) Top inner layer. (d) Bottom inner layer.

APPENDIX F

RS422 ISOLATION BOARD

F1. Schematic

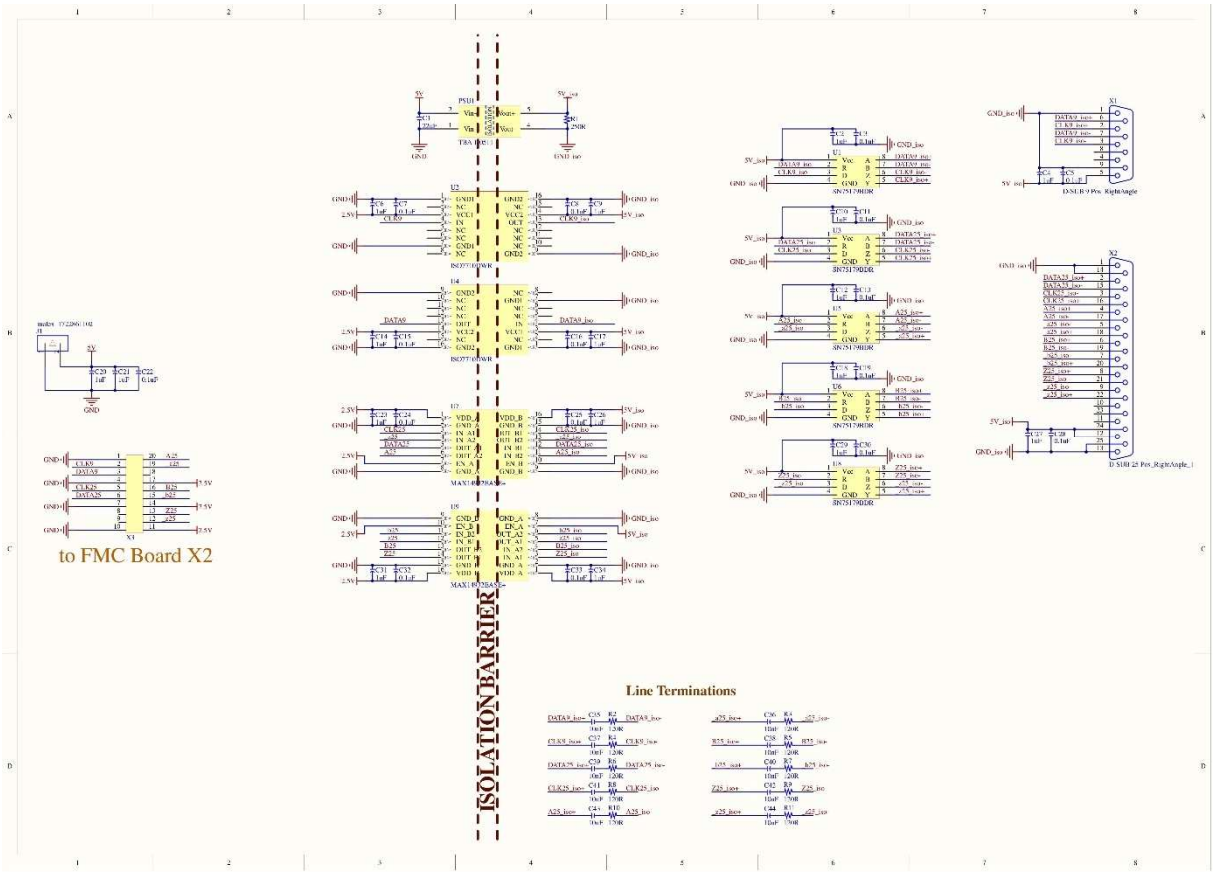
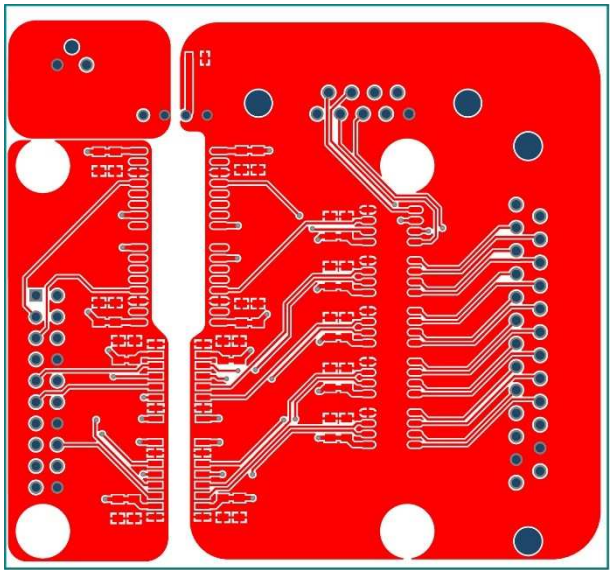
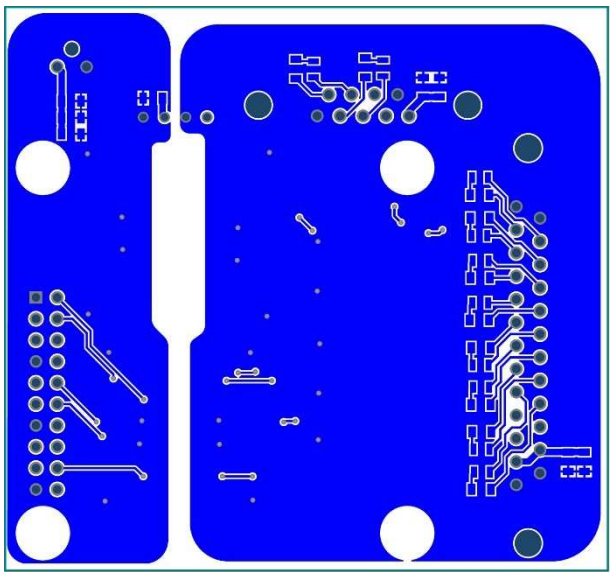


Fig F.1. RS422 isolation board schematic.

F2. Printed Circuit Board Copper Layers



(a)



(b)

Fig F.2. RS422 isolation board copper layers. (a) Top layer. (b) Bottom layer.