INSTITUTO SUPERIOR TÉCNICO
Universidade Técnica de Lisboa

LNA for a 2.4 GHz ISM Receiver

Amplificador de Baixo Ruído para a Banda ISM de 2.4 GHz em Tecnologia CMOS

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Dissertation submitted for obtaining the degree of
Master in Electrical and Computer Engineering

Jury

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July 2010

To my parents and sister

Acknowledgements

This MSc Thesis would not exist without the help from my supervisors, colleagues, friends and family.

First, I wish to acknowledge my thesis supervisors Professors Jorge Fernandes and Miguel Martins for their guidance, support and expertise. It was truly a privilege to work under their guidance and I sincerely hope this thesis will adequately reflect that.

I want to thank the colleagues with whom I worked at the group of *Circuitos analógicos e mistos* at INESC-ID for their help and fun work environment, specially, Ivanildo Gomes, Pedro Matos, Pedro Jesus and Rui Duarte.

This MsC Thesis is the culmination of a five-year journey, which would never be successful without the camaraderie and support from my IST friends. I would like to acknowledge my great friends André Esteves and David Correia, companions on countless project and study hours, who made these years much more enjoyable.

I want to thank all my close friends who never let me forget that life is primarily about having good times and creating lasting memories.

Finally, I want to thank my family for their unconditional support, and particularly my parents, José Alberto Dores and Maria Cristina Heitor and my sister, Ana Cristina Dores. I am where I am because of you. Thank you.

Abstract

This thesis presents a low cost and low power low noise amplifier (LNA) to be included in the analog frontend of a radio receiver operating in the 2.4 GHz ISM band.

The investigated LNAs are inductorless in order to reduce cost, as inductors substantially increase circuit area, and use feedback loops to achieve impedance matching with the antenna. These LNAs allow an almost independent design of the voltage gain and of the input matching, while benefitting from the advantages of feedback loops, such as, desensitization of the gain, lower nonlinear distortion and higher bandwidth.

During the LNA implementation, several aspects are taken in consideration to ensure the correct functioning of the LNA and of the radio receiver, such as the inclusion of protection from electrostatic discharges, the design of a buffer and an output stage for the LNA, and circuit simulations with bonding wire models and pads.

The LNA is implemented in a 0.13 μm CMOS technology and has an active area of 75x155 μm^2 including the buffer and the output stage. The LNA exhibits a voltage gain of 16.50 dB, a S_{11} of -11.77 dB, a noise figure of 2.66 dB and an IIP_3 of -4.97 dB, at 2.4 GHz, while having a power consumption of 3.22 mW for a voltage supply of 1.2 V.

The radio receiver where the LNA is included has an area of 0.39 mm^2, a voltage gain of 27.6 V, while having a power consumption of 16.26 mW for a voltage supply of 1.2 V.

Keywords

Radio Receiver, Low Noise Amplifier, Inductorless, Low Area, Low Cost, ISM bands.

Resumo

Nesta tese apresenta-se um amplificador de baixo ruído (LNA) com custo e consumo reduzidos. Este LNA é o primeiro andar de um receptor de rádio a operar na banda ISM de 2.4 GHz.

Os LNAs investigados nesta tese não requerem o uso de bobinas de modo a diminuir o seu custo, visto estas aumentarem significativamente a área do circuito, e usam malhas de realimentação para se conseguir adaptação da impedância de entrada com a antena. Estes LNAs permitem o dimensionamento praticamente independente do ganho de tensão e da impedância de entrada, e beneficiam das vantagens de um sistema com realimentação, tais como, dessensibilização do ganho, menor distorção não linear e maior largura de banda.

Durante a implementação do LNA foram tomados diversos cuidados, de modo a garantir o funcionamento correcto do LNA e do receptor de rádio, tais como a inclusão de protecção contra descargas electroestáticas, desenho de um andar de isolamento e de um andar de saída para o LNA. Foram também realizadas simulações do circuito com *pads* e com modelos dos fios de ligação.

O LNA foi implementado em tecnologia 0.13 μm CMOS e tem uma área activa final de 75x155 μm2, incluindo o buffer e o andar de saída. O LNA apresenta a 2.4 GHz, um ganho de tensão de 16.50 dB, um S11 de -11.77 dB, um factor de ruído de 2.66 dB e um IIP3 de -4.97 dB. O seu consumo de energia é 3.22 mW para uma fonte de tensão de 1.2 V.

O receptor de rádio onde se insere o LNA tem uma área de 0.39 mm^2 e um ganho de tensão de 27.6 V. O seu consumo de energia é 16.26 mW para uma fonte de tensão de 1.2 V.

Palavras-chave

Receptor de rádio, Amplificador de baixo ruído, Sem bobinas, Área reduzida, Baixo custo, bandas ISM.

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List of Acronyms

ADC	Analog to digital converter
AM	Amplitude modulation
FM	Frequency modulation
FoM	Figure of merit
IF	Intermediate frequency
ISM	Industrial, scientific and medical
LAN	Local area network
LNA	Low noise amplifier
LO	Local oscillator
MOS(FET)	Metal-oxide-semiconductor field-effect transistor
PM	Phase modulation
RF	Radio frequency
SNR	Signal to noise ratio
UMC	United Microelectronics Corporation

List of Symbols

Γ	Reflection coefficient
γ	Bias dependent factor
β	Feedback factor
Φ_M	Phase margin
A	Open loop gain
A_M	Amplitude margin
A_v	Voltage gain
C_{gd}	Gate-drain capacitance
C_{gs}	Gate-source capacitance
F	Noise factor
G_A	Available power gain
g_{d0}	Channel admittance
G_L	Load transconductance
g_m	Transistor transconductance
IIP_3	Third order intercept point
i_n	Noise current
k_B	Boltzmann constant
N	Noise power spectral density
NF	Noise figure
P_{-1dB}	-1 dB compression point
R_g	Gate resistance
R_S	Source resistance
S_{xy}	Scattering parameters
T	Absolute temperature
v_n	Noise voltage
y_{xy}	Admittance parameters
Z_{in}	Input impedance
Z_o	Characteristic impedance

Chapter 1

Introduction

1.1 Background and motivation

The industrial, scientific and medical (ISM) radio bands were originally reserved for the use of RF electromagnetic fields for industrial, scientific and medical purposes other than communications. However, in recent years these bands have also been shared with licence-free error-tolerant communications applications such as wireless LANs, Bluetooth devices, cordless phones or other protocol-specific devices operating in the 915 MHz, 2.450 GHz and 5.800 GHz bands. Because unlicensed devices are already required to be tolerant of ISM emissions in these bands, unlicensed low power uses are generally able to operate in these bands without causing problems for ISM users [1].

This thesis is part of an effort to implement the analog frontend of a wideband radio receiver operating in the 2.4 GHz ISM band using 0.13 μm CMOS technology to be used in several ongoing projects at INESC-ID. As this frontend will be used for portable non-critical applications, its key features are low cost and low power.

The objective of this thesis is to design a low noise amplifier (LNA), typically, the first block of a radio receiver. This block is responsible for amplifying the usually weak RF signals received at the antenna without significantly degrading the signal to noise ratio (SNR). Being low-cost a desired feature for this LNA, this thesis explores inductorless circuits since they provide large savings in area size. These circuits have the added advantage of being wideband and therefore are able to operate in multi-ISM bands if required.

1.2 Organization of the thesis

This thesis is divided into seven chapters plus annexes.

Chapter 2 describes the most important topics on RF design relevant to this thesis. It describes basic concepts of radio receivers, including its building blocks with an emphasis in the LNA block and its most important specifications. The chapter also presents important RF microelectronic concepts, such as, impedance matching, bandwidth, linearity, noise, negative feedback and circuit stability.

Chapter 3 discusses several LNA implementations, their virtues and weaknesses and the reasoning for choosing LNAs with negative feedback.

Chapter 4 presents a theoretical analysis of two LNA candidates to be implemented in the radio receiver. Their Y-matrix, gain and input impedance equations are calculated and a preliminary circuit dimensioning is done. The remaining part of the chapter consists of numerical simulations to analyze

important circuit parameters, namely, gain, input matching, noise and stability.

Chapter 5 presents circuit simulations results of the LNAs presented in chapter 4 and some variations of them. A decision is reached about which LNA to be implemented and more in depth simulations are performed including corner simulation results are presented for the chosen LNA.

Chapter 6 deals with the necessary steps taken to reach the final layout design, such as analyzing the performance degradation of the LNA when connected to other receiver blocks; the design of an output stage for testing purposes; adding circuitry to shield the LNA from electrostatic discharges; bonding wires and pads influence on the LNA performance and finally, designing the layout. The radio receiver where the LNA is included is also presented.

Chapter 7 gives the overall conclusion of the thesis and whether its objectives were achieved. Some future work is also proposed.

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Chapter 2

Fundamentals of RF Microelectronic Design

2.1 Introduction

In this chapter an overview of concepts of RF microelectronics needed to understand the following chapters of this thesis is presented. Therefore, in this chapter the structure of a wireless transceiver (2.2), some basic wireless receiver architectures and its building blocks (2.3) and several concepts of RF microelectronics important for this thesis, such as impedance matching (2.4.1), bandwidth (2.4.2), non-linear effects (2.4.3) and noise (2.4.4) are discussed. In the last section (2.5) some concepts regarding feedback systems are also discussed.

2.2 Overview of wireless transceivers

In Figure 2-1, a simple architecture of a wireless transceiver (transmitter and receiver) is shown. The purpose of a transmitter is to transmit information through a channel. The information to be transmitted is base band, which is impractical to transmit without processing due to interference (all applications would be in the same band) and to the long size of the antennas required to transmit base band signals [2]. So, in order to transmit the information, signal processing is required.

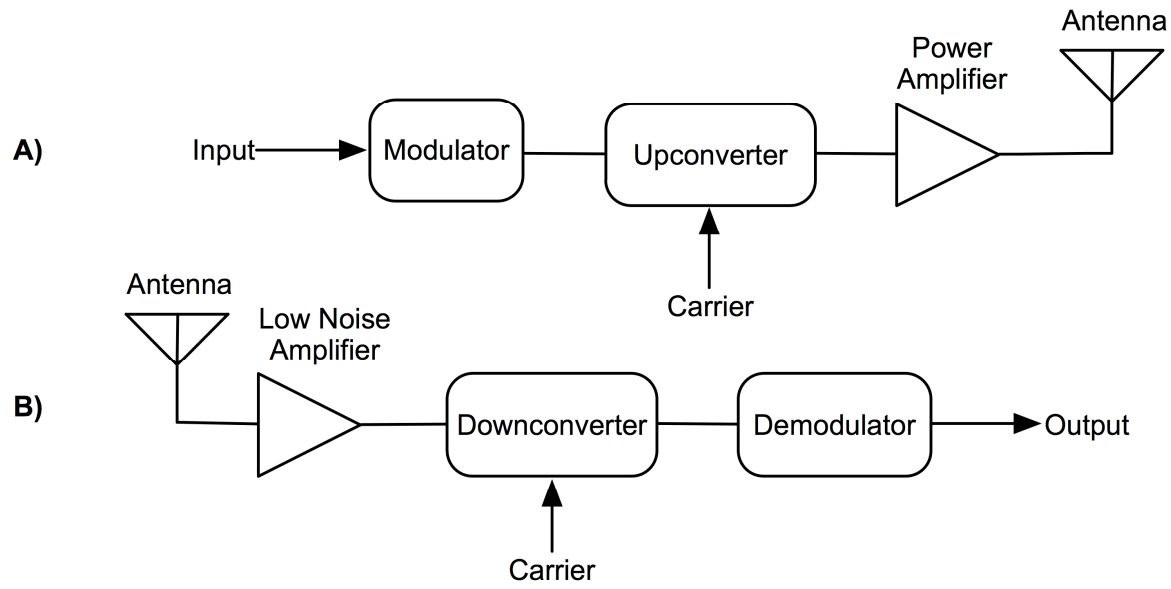


Figure 2-1. Block diagram of a generic analog RF system: A) Transmitter B) Receiver.

In the transmitter, the input signal is shifted to a higher frequency by convolution with a carrier signal. The modulator block defines the way the wanted signal varies the carrier in order to convey the

information (modulation). In the analog domain there are three basic types of modulation: amplitude modulation (AM), frequency modulation (FM) and phase modulation (PM). Further information about modulation techniques can be found in [3]. The RF signal is then amplified and transmitted through the antenna.

In the receiver, the typically weak RF signals are amplified by a LNA, downconverted back to base band or to a lower frequency (by a mixer) to facilitate the subsequent demodulation.

In Figure 2-2, an example of upconversion and downconversion is shown, where the downconversion is done directly to base band which is characteristic of homodyne systems (see 2.3).

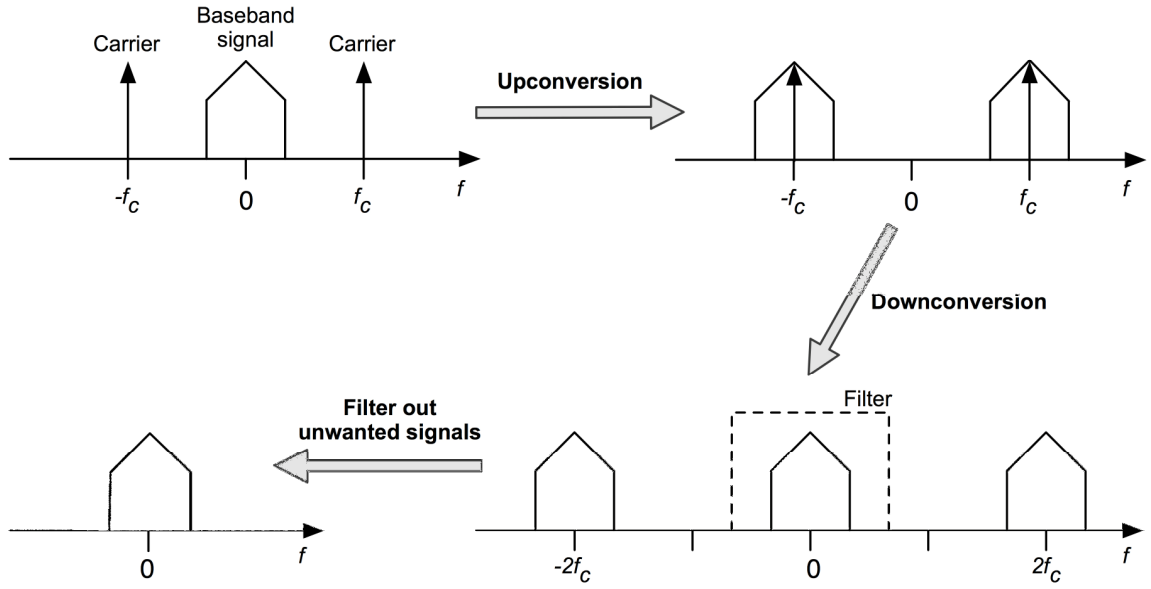


Figure 2-2. Upconversion and downconversion exemplified (homodyne system).

As explained above, it is impractical to transmit low-frequency signals. On the other hand, it is also difficult to transmit very high frequencies due to the severe attenuation these signals suffer from propagating in open-space. Therefore, the frequency range of portable wireless transceivers is typically from hundreds of MHz up to a few GHz [4].

2.3 Basic Wireless Receiver Architectures

A receiver can be divided into an analog and a digital part. The analog part is responsible for processing the RF signal, from the antenna till it is converted into binary code by an analog-to-digital converter (ADC). Further processing is done in the digital domain in the digital part of the receiver (Figure 2-3).

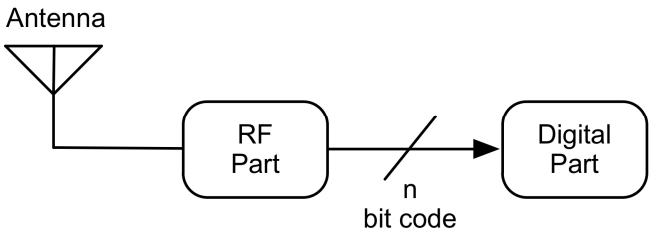


Figure 2-3. Possible block diagram of a wireless receiver.

A receiver can be catalogued in three groups regarding its bandwidth: narrowband, multi-band or wideband. In a narrowband receiver the signal bandwidth is small when compared to the frequency of the carrier [5]. A multi-band receiver can operate at several narrowbands, either one at the time or simultaneously. Finally, in a wideband receiver the signal bandwidth is of the same order of magnitude of the carrier.

Nowadays most wireless receivers are narrowband and are divided in three basic types: homodyne (or zero-IF), heterodyne (or IF) and low-IF receivers [6]. The block diagram of a receiver can be seen in Figure 2-4. The LNA is responsible for the amplification of the RF signal received by the antenna, which is then multiplied by a sinusoid (generated by the LO) at the mixer. In a homodyne receiver, the LO sinusoid and the carrier frequency are equal, resulting in a baseband signal at the mixer output. The unwanted results of the mixing are finally filtered out. In a heterodyne receiver, the LO frequency is different from the carrier frequency, resulting in an intermediate frequency at the mixer. There can be several mixing/filtering stages, each having a different LO frequency. Finally, the low-IF is a special case of heterodyne receiver where the signal is converted to a low (near zero) intermediate frequency. Low-IF receivers combine some of the advantages of the homodyne and heterodyne receivers.

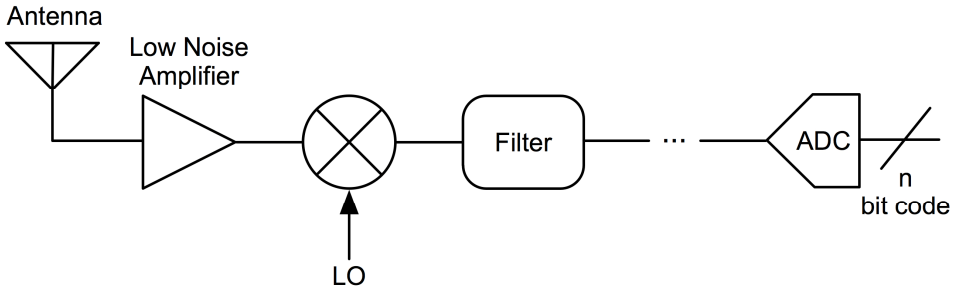


Figure 2-4. Block diagram of a wireless receiver.

Although the focus of this thesis is solely the design of a LNA, a brief description of the building blocks of a wireless receiver follows.

Low Noise Amplifier (LNA)

The LNA is the first block of the receiver and is usually connected to an antenna. Its function is to amplify the weak RF signals received by the antenna. The main considerations when designing an

LNA are:

- Input matching: the distance between the LNA and the antenna is usually of the same order of magnitude of the signal wavelength, which means that the propagation effects require that connections are made using standard impedance transmission lines [2][7]. To maximize power transfer, the LNA and the antenna should be impedance matched.

- Low noise: Friis' Law shows (see 2.4.4) that the first block of an amplifying chain has a greater contribution to the overall cascade noise factor, which means that the LNA noise contribution should be as low as possible to prevent the degradation of the SNR.

- Linearity: the LNA linearity is not a major cause of concern because the overall wireless receiver linearity is typically dominated by the last blocks of the receiver chain (see 2.4.3).

- Feedback isolation: the LNA should have a good feedback isolation to prevent instability and signal leakage from the subsequent blocks that might be reradiated by the antenna [8].

- Output matching: the LNA output impedance does not have to be impedance matched because the mixer is also integrated and the interconnection can be made short.

- Power efficiency: the wanted LNAs are usually used in portable receivers and therefore must be efficient in terms of power use.

Mixer

After the LNA, the signal is usually downconverted to a lower frequency by a mixer [7]. The mixer inputs are two signals of different frequencies: the high frequency RF signal and the local oscillator signal (LO) and presents at its output a mixture of signals at several frequencies. Of the different signals at the output, the desired one corresponds to the signal whose frequency is equal to the difference between the frequencies of the input signals. The other frequency components at the output of the mixer should be filtered out.

Local oscillator (LO)

An oscillator generates a periodic signal of a determined frequency. The periodic signal generated by a LO is used by the mixer to downconvert the high frequency RF signal to an IF or baseband signal.

Analog-to-Digital Converter (ADC)

The analog-to-digital converter converts the IF or baseband analog signal into a digital signal. The main ADC specifications are the sampling frequency and the resolution; i.e., the number of bits of the output code [9].

2.4 Concepts of RF Design

Linear circuits with multiple ports can be represented by linear combinations of voltages and currents at these ports. For circuits having only one input and one output, a matrix description of linear circuits with two-ports is used. For the general 2-port block represented in Figure 2-5, different matrices can be obtained, their choice being dependent on the circuit at hand. These matrices can be consulted at ANNEX I, however, in this thesis, only the Admittance Matrix and Chain Matrix are relevant.

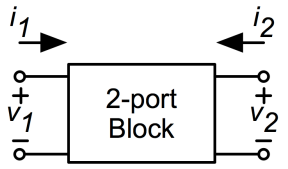


Figure 2-5. 2-port block.

2.4.1 Impedance Matching, Reflection Coefficient and Scattering Parameters

Although, from an analog point of view, an LNA is a voltage amplifier and its ideal input impedance would be infinity, it is designed to have 50 Ω resistive input impedance. This is because there is a need for input matching: the LNA is typically connected to an antenna and the distance between these circuits is of the order of the carrier wavelength, which means that the propagating effects require that the connections are made using standard impedance transmission lines. So, there is the need for input matching, in order to maximize power transfer. The 50 Ω is a standard termination impedance value that goes back to the development of coaxial cables, where 50 Ω represents a compromise between power handling and low loss [23].

Reflection Coefficient

The quality of the input matching is expressed by the input "return loss" defined as 20log|*Γ*|, where *Γ* is the reflection coefficient with respect to a source impedance Z_0 (50 Ω, in this case):

$$\Gamma = \frac{Z_{in} - Z_0^*}{Z_{in} + Z_0^*} \tag{2.1}$$

The LNA output impedance does not have to be impedance matched because the following receiver block, the mixer, is also integrated and the connection is made shorter than the signal wavelength.

S-parameters

The scattering parameters or S-parameters allow a 2-port description in terms of incident and reflected

power waves. In Figure 2-6, the 2-port block is represented by impedances Z_1 and Z_2 at ports 1 and 2, respectively. Port 1 is connected to a transmission line of characteristic impedance Z_0, and Port 2 is connected to impedance Z_{OUT}.

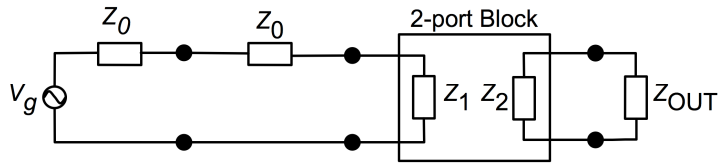


Figure 2-6. 2-port block connected to a transmission line and Z_{OUT}.

It can be shown that S_{11} is equal to (2.1), with $Z_{in}=Z_1$ and $Z_0=50\ \Omega$ [4]. An LNA is typically considered impedance matched when S_{11} is lower than -10 dB.

2.4.2 Bandwidth

The most common definition of a system bandwidth is the range of the input signal frequencies for which the gain is no more than 3 dB lower than its passing band value. Nevertheless, for this thesis it will be defined as the range of input signal frequencies for which the following conditions are met:

- Gain is no more than 3 dB lower than its passing band value;
- Noise Figure below 3 dB;
- S_{11} below -10 dB.

2.4.3 Linearity

Consider the system represented in Figure 2-7 and two input signals: $x_1(t)$ and $x_2(t)$.

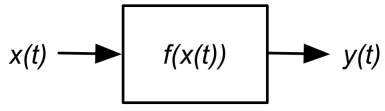


Figure 2-7. System $f(x(t))$ with input $x(t)$ and output $y(t)$.

The system is linear if its output can be expressed as a linear combination of responses to individual inputs. More accurately, if for inputs $x_1(t)$ and $x_2(t)$, the following transformations occur:

$$\begin{aligned} x_1(t) &\rightarrow y_1(t) \\ x_2(t) &\rightarrow y_2(t) \end{aligned} \tag{2.2}$$

where the arrow denotes the operation of the system, then:

$$ax_1(t)+bx_2(t)\rightarrow ay_1(t)+by_2(t) \tag{2.3}$$

for all values of *a* and *b*. Any system that does not satisfy this condition is nonlinear.

The system is time-invariant if a time shift in its input results in the same time shift in its output. That is, if $x(t)\rightarrow y(t)$, then $x(t-\tau)\rightarrow y(t-\tau)$, for all values of τ.

Finally, the system is memoryless if its output does not depend on the past values of its input.

While many analog and RF circuits can be approximated with a linear model to obtain their response to small signals, nonlinearities lead to important phenomena. For simplicity, it will be considered that the system is memoryless, time-invariant, nonlinear and assume:

$$y(t)\approx a_1x(t)+a_2x^2(t)+a_3x^3(t) \tag{2.4}$$

From this system description two different metrics are defined to measure the linearity of a circuit: the -1 dB compression point (P_{-1dB}) and the third order intercept point (IIP_3).

-1 dB Compression Point

If $x(t)=A\cos(\omega t)$, then (2.4) becomes:

$$y(t)=\frac{a_2A^2}{2}+\left(a_1A+\frac{3a_3A^3}{4}\right)\cos(\omega t)+\frac{a_2A^2}{2}\cos(2\omega t)+\frac{a_3A^3}{4}\cos(3\omega t) \tag{2.5}$$

In equation (2.5), the term with the input frequency is called “fundamental” and the high-order terms the “harmonics”.

The small-signal gain of a circuit is usually obtained with the assumption that the harmonics are negligible. If a_1A in (2.5) is much larger than all the other factors, then the small-signal gain is approximately a_1. However, in most circuits of interest, the output is a saturating function of the input, i.e, the gain approaches zero for sufficiently high input levels. In (2.5) this occurs if $a_3<0$.

P_{-1dB} is then defined as the input signal level that causes the signal gain to drop by 1 dB:

$$20\log\left|a_1A+\frac{3a_3A^3}{4}\right|=20\log|a_1A|-1\text{dB}\Leftrightarrow A_{-1dB}=\sqrt{0.145\left|\frac{a_1}{a_3}\right|} \tag{2.6}$$

The -1 dB compression point can be visualized graphically in Figure 2-8.

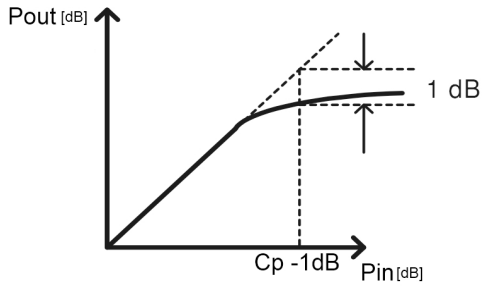


Figure 2-8. -1dB Compression Point.

Third-order Intercept Point

The third-order intercept point (IIP_3) is a practical measure of linearity. To determine it, a double tone input signal is considered:

$$x(t) = A\cos(\omega_1 t) + A\cos(\omega_2 t) \tag{2.7}$$

where ω_1 and ω_2 are two frequencies inside the bandwidth of operation. (2.8) is obtained by replacing (2.7) in (2.4).

$$\begin{aligned} y(t) = &\left(a_1 + \frac{9a_3A^2}{4}\right)A\cos(\omega_1 t) + \left(a_1 + \frac{9a_3A^2}{4}\right)A\cos(\omega_2 t) \\ &+ \frac{3a_3A^3}{4}\cos(2\omega_1 - \omega_2)t + \frac{3a_3A^3}{4}\cos(2\omega_2 - \omega_1)t \end{aligned} \tag{2.8}$$

Assuming weak distortion ($a_1 >> 9a_3A^2/4$), the amplitude A for which the output components at ω_1 (and ω_2) equal the components at $2\omega_1-\omega_2$ (and $2\omega_2-\omega_1$) is the third-order intercept point IIP_3:

$$a_1 A = \frac{3a_3A^3}{4} \Leftrightarrow A = \sqrt{\frac{4a_1}{3a_3}} = \mathrm{IIP}_3 \tag{2.9}$$

The reason the IIP_3 is the most common measure of linearity is because the third-order intermodulation products at $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$ reveal nonlinearities in almost all cases: if the difference between ω_1 and ω_2 is small, the components at $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$ appear in the vicinity of ω_1 and ω_2.

The IIP_3 point can be visualized graphically in Figure 2-9.

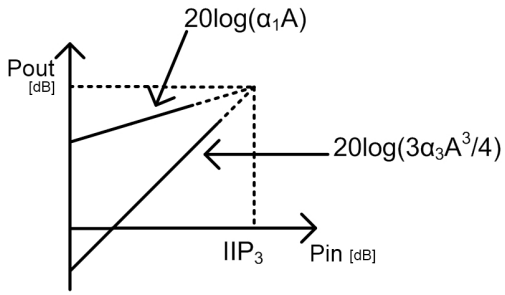


Figure 2-9. Third-order intercept point (IIP_3).

IIP_3 in cascade systems

A wireless system can be analyzed as a cascade of 2-ports, as can be seen in Figure 2-10.

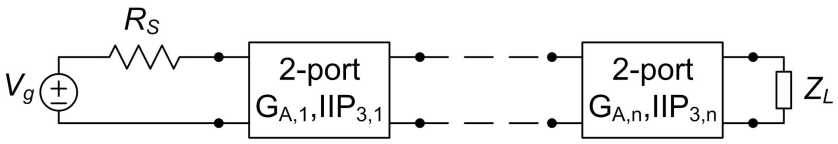


Figure 2-10. Cascade of 2-port blocks.

The IIP3 equation for the cascade is [7]:

$$\frac{1}{\mathrm{IIP}_3} = \frac{1}{\mathrm{IIP}_{3,1}} + \frac{G_{A1}}{\mathrm{IIP}_{3,2}} + \frac{G_{A1}G_{A2}}{\mathrm{IIP}_{3,3}} + \ldots + \frac{\Pi_{i=1}^{n} G_{Ai}}{\mathrm{IIP}_{3,n}} \tag{2.10}$$

where G_A is the available power gain of the 2-port block. The equation shows that the last blocks in the cascade have more influence on IIP_3 than the first ones. This is the reason why linearity is of smaller concern in an LNA.

2.4.4 Noise

Noise can be defined as any random interference unrelated to the signal of interest. It has different sources with different physical explanations and most of these sources can be characterized statistically.

In wireless receivers, noise can be divided into external and fundamental noise [12]. External noise is generated outside the receiver and can be minimized with good electromagnetic shielding and adequate system architecture. Fundamental noise results from physical phenomena in the electronic devices. Some examples are thermal noise and flicker noise.

Noise and the Wiener-Khintchine Theorem

The definition of the noise power distribution in the frequency domain is [7]:

$$N(f) = \lim_{T \to \infty} \frac{\overline{|X_T(f)|^2}}{T} \tag{2.11}$$

where $X_T(f)$ is:

$$X_T(f) = \int_0^T x_n(t) e^{-j2\pi ft} dt \tag{2.12}$$

Consider now the 2-port represented in Figure 2-11, which has a network function $H(f)$ and is excited by a noise source with a power spectral density (PSD) $N_x(f)$. The output power spectral density $N_y(f)$ is given by the Wiener-Khintchine theorem [7]:

$$N_y(f) = |H(f)|^2 N_x(f) \tag{2.13}$$

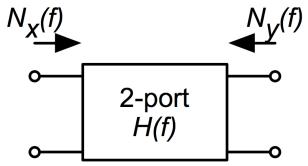


Figure 2-11. 2-port with transfer function $H(f)$ excited by noise source with power density $N_x(f)$.

Noise Factor and Noise Figure

The most common noise performance measure used in RF for a 2-port is the noise factor (F), or noise figure (NF), when expressed in dB. It is defined as the ratio between the 2-port total available output noise power and the 2-port available output noise power due only to the 2-port input noise:

$$F = \frac{\text{Total Available Output Noise Power}}{\text{Available Output Noise Power due to the Source}} \tag{2.14}$$

The noise factor can also be expressed as the ratio between the input and output signal-to-noise ratio, generated at 290 K:

$$F = \frac{\text{SNR}_{in}}{\text{SNR}_{out}} \tag{2.15}$$

The SNR is defined as the ratio of the average signal power S and the average noise power N and is independent of frequency. Thus the noise factor as defined above does not give information about the circuit noise performance along the frequency.

To express the noise performance as a function of frequency, the spot noise factor is commonly used. Consider the noisy 2-port block of Figure 2-12, where $S_i(f)$ is the input signal power, $N_i(f)$ is the input noise power, $G_A(f)$ is the available power gain of the 2-port block and $N_{p,o}(f)$ is the noise power

generated by the 2-port block reported to the output.

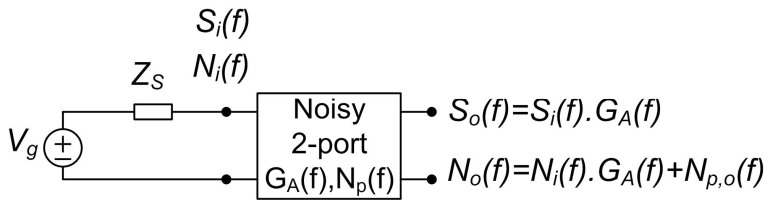


Figure 2-12. Noisy 2-port excited by signal and noise source.

The spot noise factor is then defined as:

$$F = \frac{\frac{S_i(f)}{N_i(f)}}{\frac{G_A(f)S_i(f)}{G_A(f)N_i(f)+N_{p,o}(f)}} \tag{2.16}$$

The numerator of (2.16) is the ratio of the spectral densities of the signal and noise powers at the input, while the denominator corresponds to the same ratio but at the output. (2.16) can be simplified to:

$$F = 1+\frac{N_{p,o}(f)}{G_A(f)N_i(f)} = 1+\frac{N_{p,i}(f)}{N_i(f)} \tag{2.17}$$

$N_{p,i}$ is the power generated by the 2-port block and reported to the input. As can be seen from (2.16) and (2.17), if the 2-port block is noiseless, then the noise factor equals 1.

The noise generated inside a 2-port block can be represented by the equivalent input noise voltage $v_{n,I}$ and the equivalent input noise current $i_{n,I}$, as shown in Figure 2-13. The source has a resistance R_S that generates a noise voltage $v_{n,S}$.

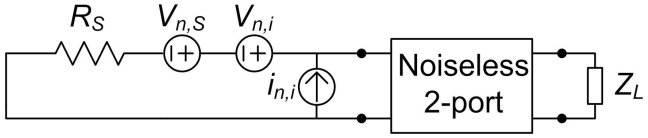


Figure 2-13. Noisy 2-port excited by signal and noise source.

The noise current source can be transformed into a voltage by multiplying it by the source impedance and considering the Norton-Thevenin transformation (ANNEX II). The equivalent input noise voltage is then:

$$v'_{n,i} = v_{n,i} + R_S i_{n,i} \tag{2.18}$$

The input noise power spectral density due to the 2-port is determined by the Wiener-Khintchine theorem (2.13):

$$N_i(f) = N_{v_{n,i}}(f) + R_S^2 N_{i_{n,i}}(f) \tag{2.19}$$

The noise factor is finally:

$$F = 1 + \frac{N_i(f)}{N_S(f)} \tag{2.20}$$

where $N_S(f)$ is the power spectral density of the noise generated by the source resistance R_S.

Friis Law

A wireless system can be analyzed as a cascade of 2-ports, as can be seen in Figure 2-14.

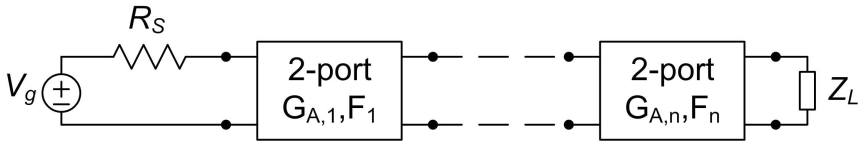


Figure 2-14. Cascade of 2-port blocks.

The noise factor referred to the input of the first block is equal to [7]:

$$F = F_1 + \frac{F_2 - 1}{G_{A1}} + \frac{F_3 - 1}{G_{A2} G_{A1}} + ... + \frac{F_n - 1}{\Pi_{i=1}^{n} G_{Ai}} \tag{2.21}$$

Equation (2.21) is known as Friis Law and it indicates that the noise contributed by each stage decreases as the gain preceding each stage increases, implying that the first few stages in a cascade are the most critical. This is the reason why the LNA noise contribution should be as low as possible.

Noise Sources

There are several noise sources in electronic devices. The most important in RF design using MOS transistors are thermal noise and flicker noise.

- Thermal Noise

  Thermal noise is the electronic noise generated by the thermal agitation of the excited electrons inside the conducting material at equilibrium and depends only on its temperature and resistance [13]. Thermal noise is approximately white, meaning that the power spectral density is nearly equal throughout the frequency spectrum and its expression is:

  $$N(f) = 4 k_B T R \tag{2.22}$$

  where k_B is the Boltzmann constant (k_B=1.380x10^{-23}JK^{-1}), R is the resistance and T is the absolute temperature in Kelvin [K].

- Flicker Noise

  Flicker noise, also known as 1/f noise or pink noise, is the least understood type of noise known [4]. No universal mechanism for flicker noise has been identified, yet it is ubiquitous. It is characterized by a spectral density that increases as frequency decreases.

  This type of noise is more relevant for mixers that perform down-conversions. As the LNA works at high frequencies, flicker noise is negligible in comparison with other noise sources [12].

Noise in MOS Transistors

For LNA design, only two noise sources will be considered in MOS transistors: thermal noise in the gate resistance R_g and represented by a voltage source $v_{n,Rg}$, and the thermal noise generated by the channel admittance g_{d0} and represented by a current source $i_{n,d}$. The noise power spectral densities of these noise sources are:

$$\begin{cases} N_{R_g}(f) = 4k_B T R_g \\ N_{i_d}(f) = 4k_B T \gamma g_{d0} \end{cases} \tag{2.23}$$

where g_{d0} is the zero-bias drain conductance and is related with the transistor transconductance g_m by the relation $g_m = \alpha\, g_{d0}$ and γ is a dimensionless bias dependent factor. For long channel transistors $\alpha = 1$ and $\gamma = 2/3$ [14]. A MOS transistor with both noise sources represented is represented in Figure 2-15.

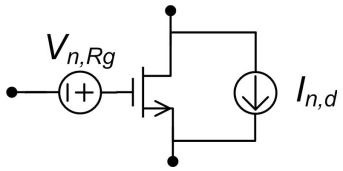


Figure 2-15. MOS transistor noise sources for RF design.

Finally, the equivalent input sources v_n and i_n are [14]:

$$\begin{cases} v_n = v_{n,R_g} + \dfrac{1}{g_m}\left(1 + \dfrac{R_g}{Z_{gs}}\right) i_{n,d} \\ i_n = 0 \end{cases} \tag{2.24}$$

where Z_{gs} is the impedance due to the gate-source capacitance.

2.5 Other Concepts

The following concepts surpass the topics of RF design but are important in order to understand the next chapters.

2.5.1 Negative Feedback

Negative feedback occurs when the output of a system acts to oppose changes to the input of the system, with the result that the changes are attenuated. If the overall feedback of the system is negative, then the system will tend to be stable.

In electronic systems, negative feedback is used in amplifiers and in a lot of other circuits, for the advantages it brings, such as:

- desensitization of the gain, which means that the gain is less sensitive to the variation of the amplifying block parameters;
- higher bandwidth;
- lower nonlinear distortion;
- lower noise figure;
- control of input and output impedances.

Negative feedback lowers the gain, which is not necessarily a disadvantage because it is easy to obtain high gains. A generic system with feedback can be represented as in Figure 2-16.

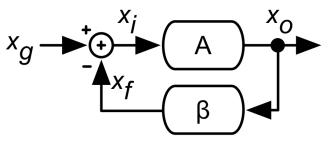


Figure 2-16. Generic system with feedback.

The variables X_g, X_i and X_f have the same dimensions, which can be different from X_o. Considering that the blocks are linear and are represented by their Laplace transformation then, for null initial conditions, we have:

$$\begin{cases} X_o = AX_i \\ X_f = \beta X_o \\ X_i = X_g - X_f \end{cases} \tag{2.25}$$

where A is the open-loop gain and β is the feedback factor. By manipulating equations (2.25), the closed loop gain A_v can be obtained:

$$A_v = \frac{X_o}{X_g} = \frac{A}{1 + A\beta} \tag{2.26}$$

$A\beta$ is usually called loop gain and $1+A\beta$ amount of feedback.

Amplifiers are 2-port blocks, which use current or voltage as input and output, so four types of feedback amplifiers are possible. They are represented in Table 2.1.

Table 2.1. Types of feedback amplifiers.

Feedback amplifier type	Input connection	Output connection	2-port matrix
Current	Shunt	Series	H'
Transimpedance	Shunt	Shunt	Y
Transconductance	Series	Series	Z
Voltage	Series	Shunt	H

A description of the 2-port matrices can be seen in ANNEX I. For this thesis the only relevant feedback amplifier type is the transimpedance amplifier, which is represented in Figure 2-17.

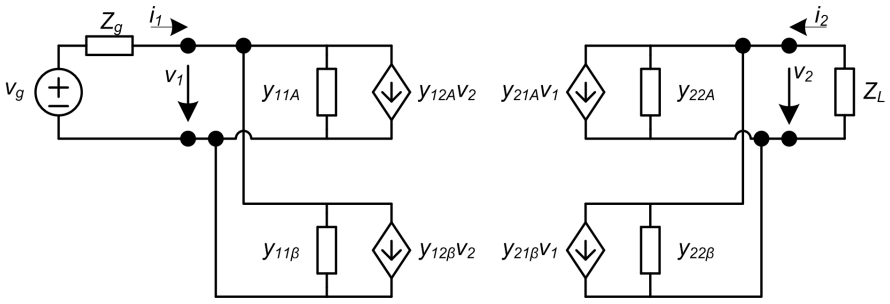


Figure 2-17. Transresistance amplifier.

It is possible to rearrange the components in Figure 2-17, resulting in Figure 2-18:

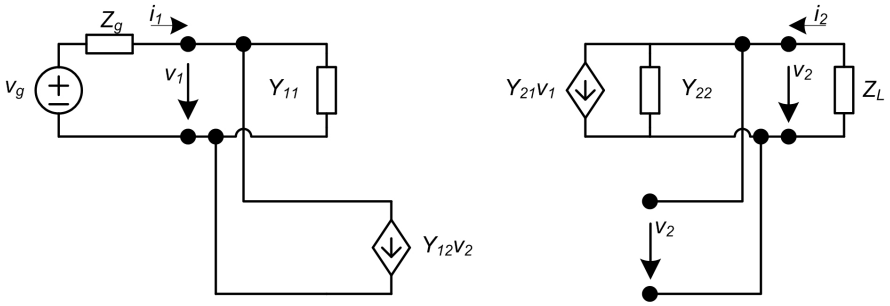


Figure 2-18. Transresistance amplifier rearranged.

with:

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} y_{11A} + y_{11\beta} & y_{12A} + y_{12\beta} \\ y_{21A} + y_{21\beta} & y_{22A} + y_{22\beta} \end{bmatrix} \tag{2.27}$$

From Figure 2-18 it can be concluded that:

$$A_v = -\frac{Y_{21}}{Y_{22} + G_L} \tag{2.28}$$

and:

$$Z_{in} = \left(Y_{11} - \frac{Y_{12} \cdot Y_{21}}{Y_{22} + G_L} \right)^{-1} (1 + A\beta) \tag{2.29}$$

Finally, the loaded *A* and the ideal β are defined as:

$$\begin{cases} A' = -\dfrac{Y_{21}}{\left(Y_{22} + \dfrac{1}{R_L} \right)\left(Y_{11} + \dfrac{1}{R_g} \right)} \\ \beta_{ideal} = Y_{12} \end{cases} \tag{2.30}$$

2.5.2 Stability

A feedback system can be unstable. This situation arises if A_f (2.26) has poles with a positive real part. So, in order to determine the stability of a feedback system, one should find the poles of A_f. But, for complex systems such calculations are difficult to do. However it is easy to evaluate the stability of a system by measuring the frequency response of $A(j\omega)$ and $\beta(j\omega)$.

In the threshold of instability the poles of A_f are in the imaginary axis, and therefore in the form $\pm j\omega$. As $A(s)$ is stable, it follows that:

$$1 + A(j\omega_p)\beta(j\omega_p) = 0 \Leftrightarrow A(j\omega_p)\beta(j\omega_p) = -1 \tag{2.31}$$

$$\Leftrightarrow \begin{cases} \left| A(j\omega_p)\beta(j\omega_p) \right| = 1 & (2.31a) \\ \arg\left[A(j\omega_p)\beta(j\omega_p) \right] = \pi & (2.31b) \end{cases}$$

It is undesirable to operate a system near the threshold of instability. So, the stability margins are usually defined to constitute a measure of stability and distance from the threshold of instability.

Consider the frequency ω_π for which $\arg\left[A(j\omega_\pi)\beta(j\omega_\pi) \right] = \pi$ and that there is only one frequency

in this condition. In this case:

- If $\left|A(j\omega_\pi)\beta(j\omega_\pi)\right| = 1$, the system is in the threshold of instability;
- If $\left|A(j\omega_\pi)\beta(j\omega_\pi)\right| < 1$, the system is stable (considering that *A* and β are stable);
- If $\left|A(j\omega_\pi)\beta(j\omega_\pi)\right| > 1$, the system is unstable.

The amplitude margin A_M is then defined in the Bode diagrams (see Figure 2-19). If A_M>0 dB, the system is stable and a higher A_M reflects a bigger distance from the threshold of instability.

Consider the frequency ω_o for which $\left|A(j\omega_o)\beta(j\omega_o)\right| = 0 \text{ dB}$ and that there is only one frequency in this condition. In this case:

- If $\arg\left[A(j\omega_o)\beta(j\omega_o)\right] = \pi$, the system is in the threshold of instability;
- If $\arg\left[A(j\omega_o)\beta(j\omega_o)\right] > -\pi$, the system is stable (considering that *A* and β are stable);
- If $\arg\left[A(j\omega_o)\beta(j\omega_o)\right] < -\pi$, the system is unstable.

The phase margin ϕ_M is then defined in the Bode diagrams (see Figure 2-19). If ϕ_M >0, the system is stable and a higher ϕ_M >0 reflects a bigger distance from the threshold of instability.

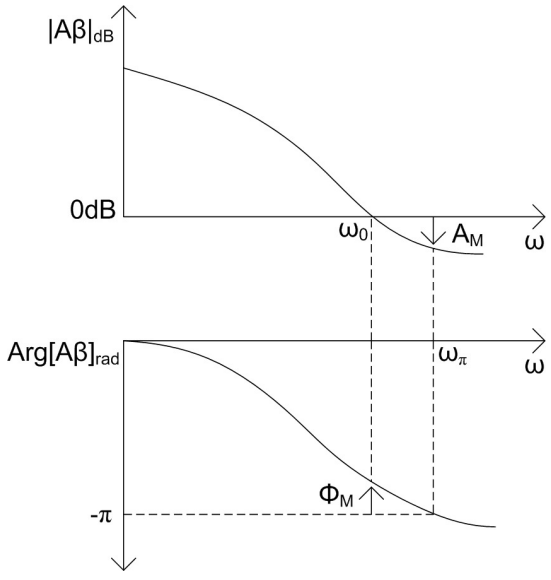


Figure 2-19. Stability margins.

The hypothesis that there is only one frequency ω_o and one frequency ω_π, so that the amplitude and phase margins can be defined without ambiguity is guaranteed when the *|Aβ|* and *arg[Aβ]* curves decrease monotonically when ω increases. This only happens if there are real poles in the critical

range of frequencies, i.e, where $|A\beta|$ has values near 0 dB and $arg[A\beta]$ has values near π.

If the loop gain $A(s)\beta(s)$ has only one pole the Bode diagrams look like Figure 2-20. In that case, the system is always stable with phase margin higher than 90º.

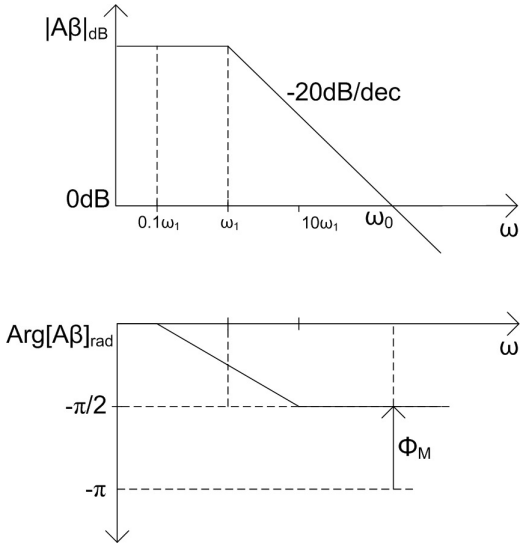


Figure 2-20. Asymptotic Bode diagrams for loop gain with only one pole.

If the loop gain $A(s)\beta(s)$ has two poles the Bode diagrams look like Figure 2-21. In that case, the system continues to be stable but has a very small phase margin (in Figure 2-21, as it is a Bode diagram, the stability margins appear to be zero, but in reality they would be positive, even if only slightly so).

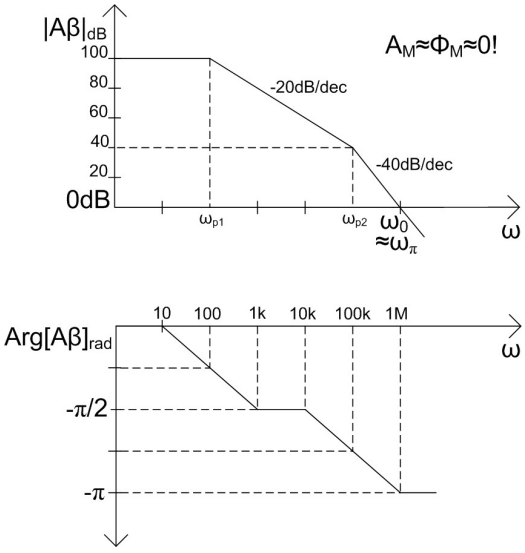


Figure 2-21. Example of asymptotic Bode diagrams for loop gain with two poles.

If the loop gain $A(s)\beta(s)$ has three or more poles, which is the case in any RF circuit, the Bode diagrams can be stable or unstable, depending on the poles location. Therefore, it is important to define a dominant pole and ensure stability.

Chapter 3

LNA Basic Topologies

3.1 Introduction

The LNAs' main parameters are input impedance, gain and noise figure. The ideal LNA has finite input impedance matched to the output impedance of the preceding block, to maximize power transfer of the received high frequency signal (usually 50 Ω - see 2.4.1), and it should amplify the typically weak received signals without noise addition (Friis Law - see 2.4.4). Linearity has a lower priority in comparison with other parameters (linearity is more important for the last blocks in the receiver chain - see 2.4.3). Concerning bandwidth, LNAs can be narrowband, multi-band or wideband.

According to [7] a typical LNA in heterodyne systems should have the following general characteristics:

Table 3.1. Typical LNA characteristics in heterodyne systems.

Noise Figure (NF)	2dB
Third-order intercept (IIP_3)	-10dBm
Gain	15dB
Input Impedance	50 Ω

For the specific LNA to be designed in the thesis there are two other important parameters: low power and low cost. The first parameter is consequence of the portable nature of the receiver in which the LNA is to be included. The second parameter leads to minimizing the area of the circuit as cost and area are intrinsically related.

Few circuits can satisfy these specifications simultaneously at the required frequency band. In the following sections, an overview of the most used LNA topologies is presented.

3.2 LNA Topologies

LNAs can be implemented in several technologies but in this thesis only MOS transistors are considered. For the analysis of the different topologies a simple incremental model shown in Figure 3-1 is used. It only includes the transconductance g_m and the gate-source capacitance C_{gs}. Other elements, like the gate resistance R_g and the gate-drain capacitance C_{gd} will be neglected for simplicity.

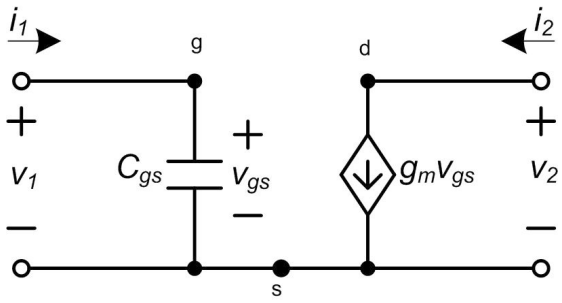


Figure 3-1. MOS incremental π model.

Of the three most important LNA characteristics (input impedance, noise factor and gain), only the input impedance should have a precise value and the following topologies show the most common approaches to obtain the 50 Ω at the input.

3.2.1 LNA using an Input Resistor

The simplest and easiest way to obtain input matching is to put a resistance in parallel with the amplifying block, as shown in Figure 3-2.

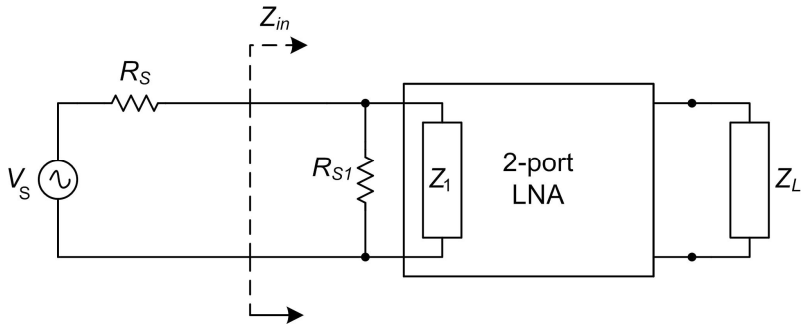


Figure 3-2. LNA using Input Resistor.

For the circuit represented in Figure 3-2 the input impedance Z_{in} is $R_{s1}//Z_1$. If Z_1 is much higher than R_{S1} then Z_{in} is approximately equal to R_{S1}, and there is input matching if $R_{S1} = R_S$.

Assuming that the 2-port is noiseless, the only noise contribution is the thermal noise generated by R_{S1}. The noise factor is then:

$$\begin{cases} F = 1 + \dfrac{N_i(f)}{N_S(f)} = 1 + \dfrac{N_{S1}}{N_S} = \dfrac{N_S + N_{S1}}{N_S} = \dfrac{R_S + R_{S1}}{R_S} = 2 \\ N_x = 4k_B T R_x \end{cases} \tag{3.1}$$

where N_S and N_{S1} are the noise power spectral densities due to the source resistance R_S and the input matching resistance R_{S1}, respectively. (3.1) shows that there is a 3 dB penalty (10log(2)) in the noise figure by using a resistor in parallel with the LNA input impedance. To this penalty it is still necessary to add the noise due to the other non-ideal components.

3.2.2 Common-Gate LNA

In the common-gate LNA the input matching is done through the transistor transconductance as shown in Figure 3-3[15].

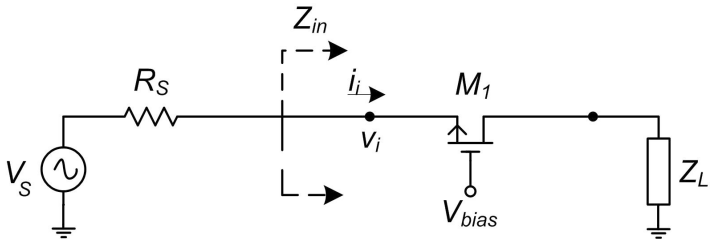


Figure 3-3. Common-gate LNA (biasing not represented).

Replacing the common-gate transistor by the incremental model of Figure 3-1, leads to:

$$Z_{in} \approx \frac{1}{g_m} \tag{3.2}$$

and there is input matching if $g_m = 1/R_S$. This topology has the clear disadvantage of not having the voltage gain independent of the input matching.

Regarding noise analysis and considering the MOS transistor noise sources (see 2.44 – Noise sources), the noise power spectral density due to the common-gate transistor referred at its input can be determined as:

$$N_i(f) = 4k_B T\left(R_g + R_S^2 \gamma g_m\right) \tag{3.3}$$

where R_g is the gate resistance of the transistor and γ is a bias dependent factor (for long channel transistors $\gamma = 2/3$). The noise factor is then:

$$F = 1 + \frac{N_i}{N_S} = 1 + \frac{R_g}{R_S} + R_S \gamma g_m \tag{3.4}$$

Assuming that $R_g = 0$ and $\gamma = 2/3$, this LNA topology has a minimum noise factor of 5/3 which is approximately 2.2 dB.

3.2.3 Common-Source LNA with Inductive Degeneration

The topology shown in Figure 3-4 was first proposed in [16].

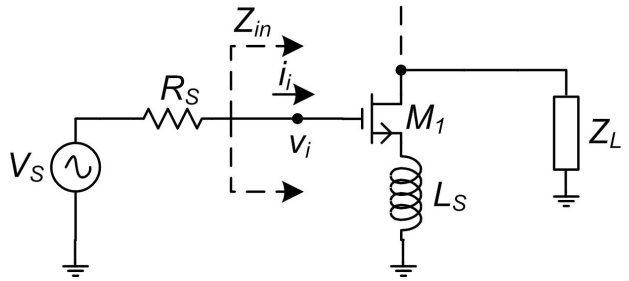


Figure 3-4. Common-Source LNA with inductive degeneration (biasing not represented).

Replacing the common-source transistor by the incremental model of Figure 3-1, leads to:

$$Z_{in} = \frac{g_m L_S}{C_{gs}} + \frac{1}{sC_{gs}} + sL_S \tag{3.5}$$

Z_{in} is real at the resonant frequency:

$$Z_{in} = \frac{g_m L_S}{C_{gs}} \quad \text{at} \quad \omega_0 = \frac{1}{\sqrt{L_S C_{gs}}} \tag{3.6}$$

Assuming that g_m, C_{gs} and L_S are ideally noiseless, means that it is possible to achieve a real input impedance without addition of noise using this topology. Moreover voltage gain and input matching are independent: g_m can be maximized to improve gain, while the values of C_{gs} and L_S are used to obtain the required input matching. This topology also has the characteristic of being narrowband.

These qualities make this topology very popular. Its only drawback is the use of an inductor, which has a large circuit area when compared to other components, thus increasing its cost [4].

3.2.4 LNA with Resistive Feedback

The topology shown in Figure 3-5 uses a resistor connected in a shunt-shunt feedback topology [17].

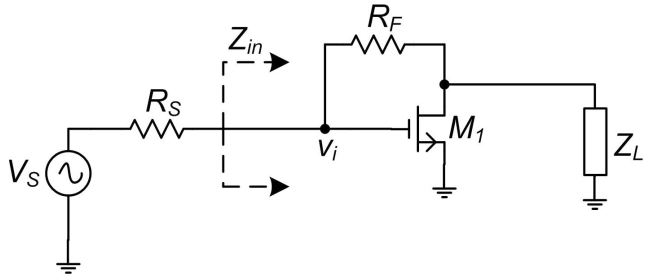


Figure 3-5. LNA with resistive feedback (biasing not represented).

Replacing the transistor by the incremental model of Figure 3-1, leads to:

$$Z_{in} = \frac{R_F + Z_L}{1 + g_m Z_L + (R_F + Z_L) s C_{gs}} \tag{3.7}$$

If the load impedance Z_L is high enough, Z_{in} simplifies to:

$$Z_{in} = \frac{1}{g_m + s C_{gs}} \tag{3.8}$$

For frequencies at which sC_{gs} is negligible in comparison with g_m, the input impedance is almost real and equal to $1/g_m$. Neglecting Z_L and C_{gs}, it can also be shown that the voltage gain is:

$$A_v = \frac{v_o}{v_s} = \frac{1 - R_F g_m}{1 + R_S g_m} \tag{3.9}$$

which can be simplified to:

$$A_v \approx -\frac{R_F}{R_S} \tag{3.10}$$

if g_m is high enough. This shows that it is possible to have the voltage gain and the input impedance dimensioned almost independently, although these variables are not independent.

Regarding the noise figure, the resistive feedback network generates thermal noise of its own. As a consequence, the overall amplifier's noise figure, while usually much better than that of the circuit in Figure 3-2, still generally exceeds that of the circuit in Figure 3-4. Nonetheless, it has smaller area due to the fact that this circuit does not use inductors, which is frequently an advantage to give it preference over other topologies.

3.2.5 Discussion

There are obviously countless other ways to design an LNA with MOS transistors, but they can be seen as variations of these four basic topologies. Therefore, it is advisable to look into these four topologies and see which is a better fit to the parameters of the LNA to be designed.

From the above analysis of the basic LNA topologies some conclusions can be made. The overall best topology is the common-source LNA with inductive degeneration due to its minimal noise figure and the independent dimensioning of its gain and input matching. But its high circuit area due to the use of an inductor makes it an inadvisable choice for a project where low cost is an important parameter. That leaves us to ponder the other possible topologies, where the LNA with resistive feedback clearly is the best candidate. It has a lower noise figure than the LNA using an input resistor and unlike a common-gate LNA it is possible to design the voltage gain and the input impedance almost independently. Moreover it has all the advantages that come along from using a feedback loop:

desensitization of the gain, lower nonlinear distortion and higher bandwidth.

Therefore it was decided to look into LNA topologies with feedback, in particular two circuits, which already proved to be successful with other technologies. These circuits are discussed in the next chapter.

Chapter 4

Theoretical Analysis of Two LNAs with Feedback

4.1 Introduction

In this chapter two circuits which were studied as possible implementations of the LNA for the wireless radio receiver are presented. Both circuits are inductorless in order to provide savings in area and cost and use a shunt-shunt feedback topology for impedance matching. In section 4.2 a circuit description is presented and in section 4.3 the Y-Matrix coefficients are calculated. A preliminary circuit dimensioning is done in section 4.5 based on the gain and input impedance equations found in section 4.4. Finally an analysis of several parameters of the circuits is presented in sections 4.6 to 4.9.

The wireless receiver is designed to work for the 2.4 GHz ISM band and the desired LNA specifications are as follows:

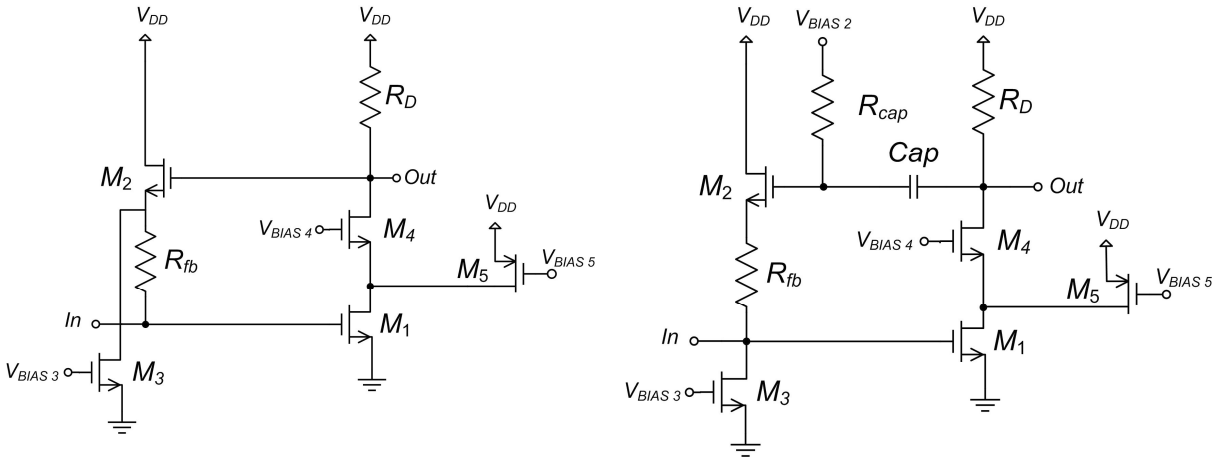
Current consumption	2 mA
Voltage gain	20 dB
S_{11} at 2.4GHz	< -10 dB
Noise figure at 2.4GHz	< 3 dB
IIP_3	0 dBm
P_{-1dB}	> -14 dBm

Table 4.1. Specifications of the LNA.

The technology to be used in the LNA is the CMOS UMC 0.13 µm with 8 metal layers and a V_{DD} of 1.2 V.

4.2 Circuit Description

The analyzed circuits are shown in Figure 4-1. LNA_A was first presented in [18] and LNA_B is discussed in [19].



LNA_A LNA_B

Figure 4-1. LNA_A and LNA_B.

LNA_A can be divided in two main blocks: the amplifying block (M_1, M_4 and R_D) and the feedback block (M_2 and R_{fb}). M_3 and M_5 are used for biasing and for circuit performance, respectively.

The amplifier block is a cascode stage with a resistance load, where both transistors M_1 and M_4 must operate in the saturation region. A cascode stage is used for its advantages such as higher gain and higher input-output isolation [15]. The gain of this stage depends mainly on g_{m1} and R_D. If necessary, M_5 is used for current steering, providing more current for M_1 without having a higher voltage drop in R_D, which could put M_4 out of the saturation region.

The feedback block is used to achieve the 50 Ω input matching. M_3 is used to permit adequate biasing of M_2 without voltage drop in R_{fb}.

LNA_B operates approximately in the same manner. The main difference between these circuits is regarding the dimensioning of the DC operating point: LNA_B allows a completely independent dimensioning of the amplifying and feedback blocks as the capacitor connected to the gate of M_2 disconnects the blocks at low frequencies, while in LNA_A there is always a feedback loop, which makes individual dimensioning of the blocks impossible. There is a clear trade-off between the size of the circuit and the difficulty of the dimensioning. To provide a deeper understanding of the circuits and their feasibility, the Y-matrix of the LNAs was obtained and a preliminary circuit dimensioning was done to allow numerical simulations of the parameters of the circuits (noise figure, input matching and stability).

4.3 Y-Matrix

As the LNAs have a shunt-shunt feedback topology (Figure 2-17), a Y-matrix is used to describe the amplifiers. This description of the circuits by its Y-parameters is useful for various calculations that provide insight about them, such as gain, input impedance, noise figure and stability. Each coefficient of the matrix is calculated through the following expressions:

$$Y = \begin{bmatrix} y_{11} = \left.\frac{i_1}{v_1}\right|_{v_2=0} & y_{12} = \left.\frac{i_1}{v_2}\right|_{v_1=0} \\ y_{21} = \left.\frac{i_2}{v_1}\right|_{v_2=0} & y_{22} = \left.\frac{i_2}{v_2}\right|_{v_1=0} \end{bmatrix} \tag{4.1}$$

The model of the transistor used in these calculations is shown in Figure 4-2. This model takes into account the 2-order effects of the capacitor C_{gd} in order to provide a deeper analysis.

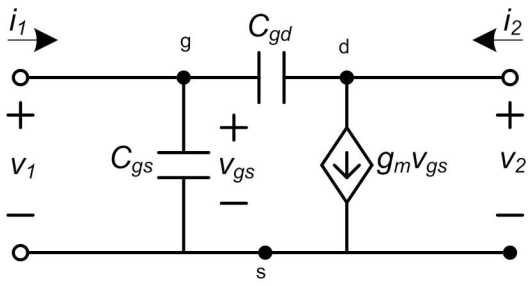


Figure 4-2. MOS incremental model used.

Both LNAs have the same small-signal circuit, which can be seen in Figure 4-3. The only difference is regarding the resistance $R_{T'}$, which is equal to R_D in LNA_A and equal to $R_D//R_{cap}$ in LNA_B. Nevertheless, R_{cap} is designed to have a much higher impedance value than R_D so that the approximation $R_{T'} \approx R_D$ can be made.

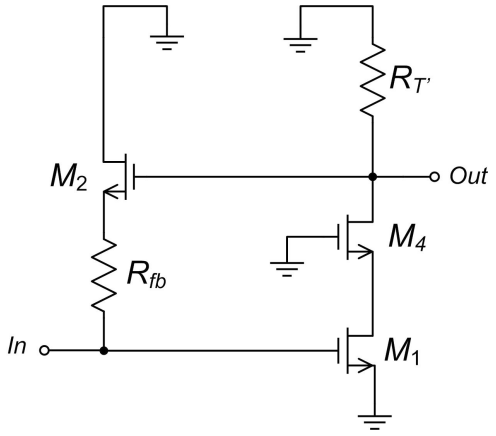


Figure 4-3. Small signal circuit of LNA_A and LNA_B.

Amplifying Block Y-Parameters

The amplifying block of the LNAs can be represented as seen in Figure 4-4.

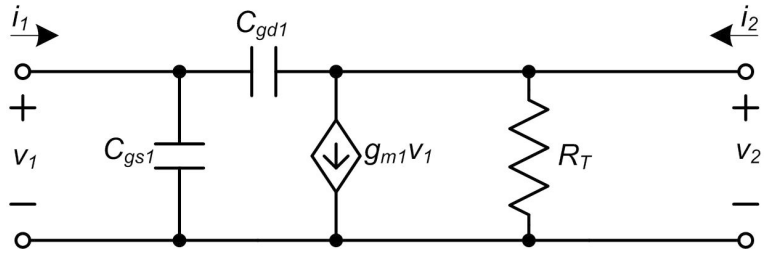


Figure 4-4. Small signal circuit of the amplifying block.

R_T is equal to the parallel of $R_{T'}$ with the output impedance of the cascode [9] (R_{o4} equation takes into account the incremental output impedance of a transistor):

$$\begin{cases} R_{o4} = r_{o1} + r_{o4}\left[1 + (g_{m4} + g_{mb4})r_{o1}\right] \\ R_T = R_{T'} // R_{o4} \approx R_{T'} \approx R_D \end{cases} \qquad \text{because } R_{o4} >> R_{T'} \tag{4.2}$$

The Y-parameters of the amplifying block are:

$$\begin{cases} y_{11A} = s(C_{gs1} + C_{gd1}) \\ y_{12A} = -sC_{gd1} \\ y_{21A} = g_{m1} - sC_{gd1} \\ y_{22A} = \left(\dfrac{1}{R_T} + sC_{gd1}\right) \end{cases} \tag{4.3}$$

The calculations performed to reach these results are in ANNEX III.

Feedback Block Y-Parameters

The feedback block of the LNAs can be represented as seen in Figure 4-5.

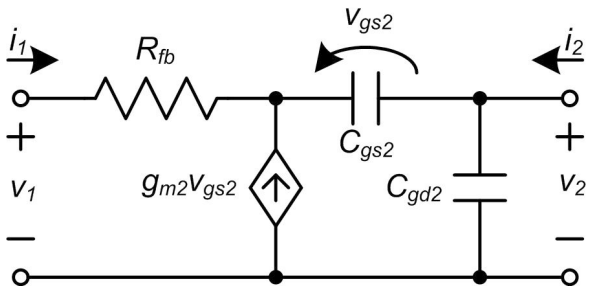


Figure 4-5. Small signal circuit of the feedback block.

The Y-parameters of the feedback block are:

$$\begin{cases} y_{11\beta} = \dfrac{gm_2 + sC_{gs2}}{1 + gm_2 R_{fb} + sC_{gs2} R_{fb}} \\ y_{12\beta} = -\dfrac{g_{m2} + sC_{gs2}}{1 + gm_2 R_{fb} + sC_{gs2} R_{fb}} \\ y_{21\beta} = -\dfrac{sC_{gs2}}{1 + gm_2 R_{fb} + sC_{gs2} R_{fb}} \\ y_{22\beta} = \dfrac{s\left(C_{gd2} + C_{gs2} + gm_2 C_{gd2} R_{fb} + sC_{gs2} C_{gd2} R_{fb}\right)}{1 + gm_2 R_{fb} + sC_{gs2} R_{fb}} \end{cases} \tag{4.4}$$

The calculations performed to reach these results are in ANNEX III.

Equivalent Y-Parameters

The equivalent Y-parameters that represent the matrix description of the full circuit are the result of the sum of the components from the amplifying and feedback blocks.

$$\begin{cases} Y_{11} = y_{11A} + y_{11\beta} \\ Y_{12} = y_{12A} + y_{12\beta} \\ Y_{21} = y_{21A} + y_{21\beta} \\ Y_{22} = y_{22A} + y_{22\beta} \end{cases} \tag{4.5}$$

4.4 Gain and Input Impedance

The gain and input impedance are obtained by substituting the Y-parameters in equations 2.28 and 2.29. The load impedance is modelled as a capacitance because the input impedance of the mixer is mostly capacitive ($Z_L \approx C_L$ - see ANNEX IV). The resulting equations (4.6 and 4.7) are too complex to be analyzed manually but are useful in numerical analysis, which are presented from sections 4.6 to 4.8.

$$\begin{aligned} A_v &= \frac{N}{D} \\ N &= R_T\left[-g_{m1}\left(1 + g_{m2} R_{fb} + sR_{fb} C_{gs2}\right) + s\left(C_{gd1} + C_{gs2} + g_{m2} R_{fb} C_{gd1} + sR_{fb} C_{gd1} C_{gs2}\right)\right] \\ D &= 1 + sR_T\left[C_{gd1} + C_{gd2} + C_l\right] + g_{m2} R_{fb}\left[1 + sR_T\left(C_{gd1} + C_{gd2} + C_l\right)\right] + sC_{gs2}\left[R_{fb} + R_T + sR_{fb} R_T\left(C_{gd1} + C_{gd2} + C_l\right)\right] \end{aligned} \tag{4.6}$$

$$
\begin{aligned}
&Z_{in} = \frac{N}{D} \\
&N = 1 + sR_T\left[C_{gd1} + C_{gd2} + C_l\right] + g_{m2}R_{fb}\left[1 + sR_T\left(C_{gd1} + C_{gd2} + C_l\right)\right] + sC_{gs2}\left[R_{fb} + R_T + sR_TR_{fb}\left(C_{gd1} + C_{gd2} + C_l\right)\right] \\
&D = g_{m2}\left[1 + sR_{fb}\left(C_{gd1} + C_{gs1}\right) + R_T\left(g_{m1} + sg_{m1}C_{gd1}R_{fb} + s\left[C_{gd2} + C_l + sR_{fb}\left(C_{gs1}\left[C_{gd2} + C_l\right] + C_{gd1}\left[C_{gd2} + C_{gs1} + C_l\right]\right)\right]\right)\right] \\
&+s\left[C_{gs1} + C_{gs2} + sC_{gs1}R_T\left(C_{gd2} + C_l\right) + C_{gd1}\left(1 + sC_{gs2}R_{fb}\right)\left(1 + g_{m1}R_T + sR_T\left[C_{gd2} + C_{gs1} + C_l\right]\right)\right] \\
&+C_{gs2}\left(sC_{gs1}R_{fb} + R_T\left[g_{m1} + s\left(C_{gd2} + C_{gs1} + C_l + sC_{gs1}R_{fb}\left[C_{gd2} + C_l\right]\right)\right]\right)
\end{aligned}
\tag{4.7}
$$

Some simpler equation can be obtained by neglecting C_{gs} and C_{gd} and considering the load impedance of the circuit to be infinite ($Z_L \to \infty$). The resulting equations are as follows:

$$A_v \approx -g_{m1}R_T \tag{4.8}$$

$$Z_{in} \approx \frac{1 + g_{m2}R_{fb}}{g_{m2}(1 + g_{m1}R_T)} \approx \frac{1 + g_{m2}R_{fb}}{g_{m2}\left(1 + \left|A_v\right|\right)} \tag{4.9}$$

These equations are used to obtain a first draft of the circuit dimensioning for the passing band as they neglect high frequency effects.

4.5 Circuit Dimensioning

4.5.1 LNA_A Circuit Dimensioning

In Figure 4-6, the critical paths regarding the circuit biasing for the LNA_A circuit are represented.

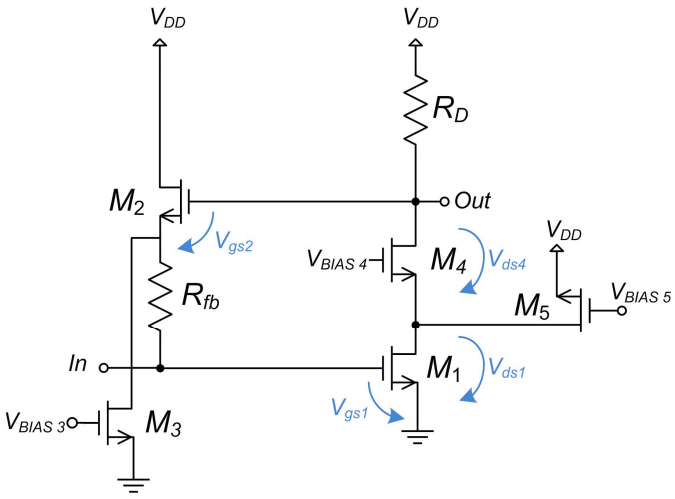


Figure 4-6. Critical path for the LNA_A.

The equations representing those paths are:

$$V_{OUT} = V_{GS2} + V_{GS1} \tag{4.10}$$

$$V_{OUT} = V_{DS4} + V_{DS1} \tag{4.11}$$

The transistors have to be in the saturation region. Thus, the lower bound of V_{OUT} that allows a correct biasing is expressed by the following equation:

$$V_{OUT\,MIN} = \max\left\{\left(V_{TH2} + V_{TH1}\right), \left(V_{DSAT4} + V_{DSAT1}\right)\right\} \tag{4.12}$$

where V_{TH1} and V_{TH2} are the threshold voltages of transistors M_1 and M_2, respectively, and V_{DSAT1} and V_{DSAT4} are the minimum values of the drain source voltage needed for the transistors M_1 and M_4 to be in the saturation region. From simulations done with transistors of the chosen technology, it was found that 400 mV and 100 mV are reasonable values for V_{TH} and V_{DSAT}, respectively. Therefore, the minimum value of V_{OUT} is 800 mV. To increase reliability it was chosen to dimension the circuit with a V_{OUT_MIN} of 900 mV.

The maximum value for V_{OUT} is the supply voltage, 1.2V. V_{OUT} is then restricted from 0.9 V to 1.2 V and a correct dimensioning of the circuit leads to choosing a DC voltage for this node in the middle of this gap to increase linearity:

$$V_{OUT\,DC} = \frac{1.2 + 0.9}{2} = 1.05V$$

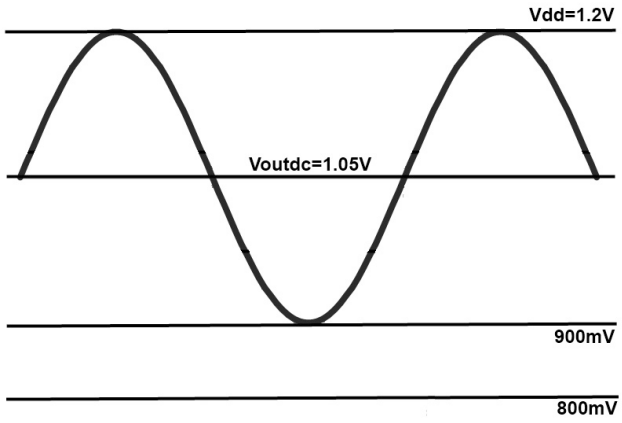


Figure 4-7. Sine wave at V_{OUT}.

Looking at the amplifying block of LNA_A, V_{OUTDC} can also be expressed as:

$$V_{OUTDC} = V_{DD} - R_D I_{DC} \tag{4.13}$$

Considering the current consumption to be 2 mA and attributing 75% of this consumption to the amplifying block (I_{DC} =1.5 mA), results in a value of 100 Ω for R_D.

Considering that $R_T \approx R_D$ and that the desired gain is 20 dB, from equation 4.8 results that g_{m1} is equal to 100 mS. As a trade-off to lower the power consumption and the transistor size, and still having an effective feedback factor, leaded to consider g_{m2} five times smaller than g_{m1}, i.e., g_{m2} equal to 20 mS. Finally, from equation 4.9, and considering Z_{in} to be 50Ω results in a value of 500 Ω for R_{fb}.

Regarding the capacitances, it was found that 20 fF and 40 fF are reasonable values for C_{gd} and C_{gs}, respectively. These values were found through simulations done with transistors of the chosen technology. As a summary, the circuit dimensioning of LNA_A can be seen in Table 4.2.

Table 4.2. Circuit dimensioning of LNA_A.

g_{m1}	100 mS
g_{m2}	20 mS
R_T	100 Ω
R_{fb}	500 Ω
C_{gs}	40 fF
C_{gd}	20 fF

4.5.2 LNA_B Circuit Dimensioning

Contrary to LNA_A, LNA_B does not have a feedback loop when considering the DC operating point due to the capacitor, which for low frequencies 'disconnects' the feedback loop. Although the beneficial effects of feedback loops are lost for small frequencies and there is no stabilized biasing, the dimensioning of the DC operating point is more flexible (amplifying block and feedback block are dimensioned separately).

So, for LNA_B there is only one critical path, which is equal to equation 4.11, which in turn defines the lower bound of V_{OUT} at 200 mV. Again, to increase reliability it was chosen to size the circuit with a V_{OUT_MIN} of 300 mV. Considering V_{OUTMAX}=1.2 V, leads to V_{OUTDC}=0.75 V.

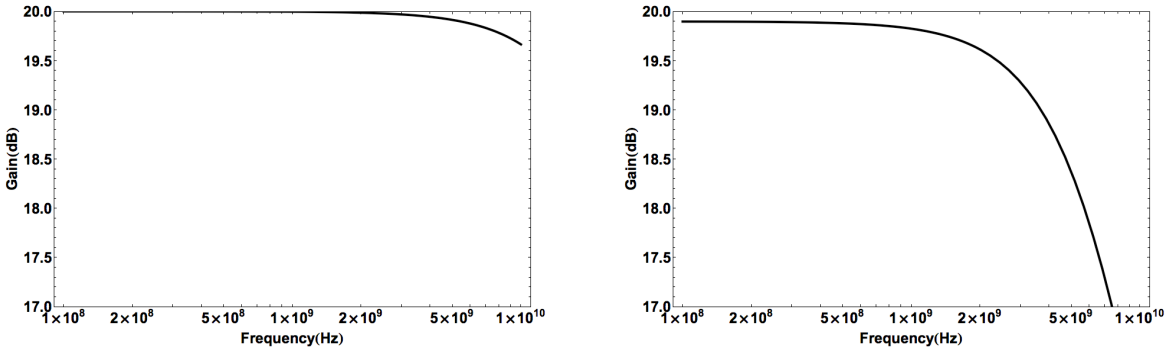
The rest of the dimensioning was done using the same criteria as in section 4.5.1 leading to the circuit dimensioning presented in Table 4.3.

Table 4.3. Circuit dimensioning of LNA_B.

g_{m1}	27 mS
g_{m2}	5.5 mS
R_T	366 Ω
R_{fb}	367 Ω
C_{gs}	40 fF
C_{gd}	20 fF

4.6 Gain Analysis

In Figure 4-8, plots of the gain magnitude as a function of frequency for the LNA_A and LNA_B are shown. To obtain these plots, the values of the circuit dimensioning were substituted in equation 4.6 and the substitution $s=2j\pi f$ was applied. The absolute value of the resulting equation is then plotted using the program *Mathematica* (the source code is in ANNEX VI). In these plots the load impedance is considered to be infinite, therefore they show the effects of the capacitances C_{gs} and C_{gd} of the transistors.

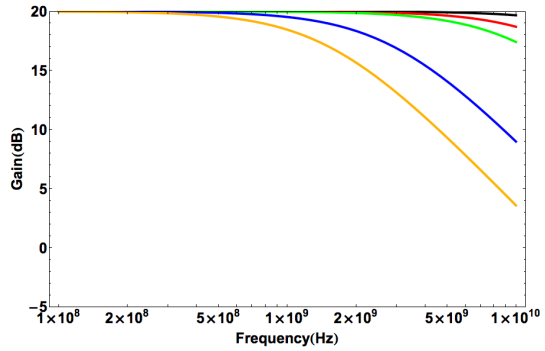


LNA_A Gain ($Z_L \to \infty \leftrightarrow C_L$=0 F) LNA_B Gain ($Z_L \to \infty \leftrightarrow C_L$=0 F)

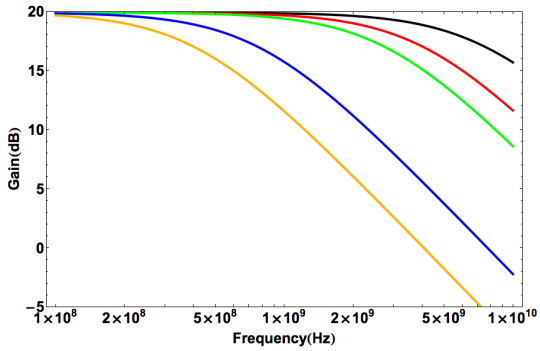
Figure 4-8. Gain of LNA_A and LNA_B with infinite load impedance.

As can be seen from the plots, the effects of the capacitances C_{gs} and C_{gd} are minimal. At 2.4 GHz, the gain of LNA_A is 20.0 dB and of LNA_B is 19.5 dB. The reason for a lower gain decrease in LNA_A is due to a higher $g_{m1}R_T$, which mitigates more the effect of the capacitances.

In Figure 4-9, plots of the gain magnitude as a function of frequency for different values of the load capacitance are presented. As expected, the plots show that both circuits are sensitive to the value of the output impedance with a significant decrease in bandwidth as the output impedance increases. A possible solution to this problem is to use a buffer with high input impedance between the LNA and the mixer.



LNA_A Gain (varying C_L)

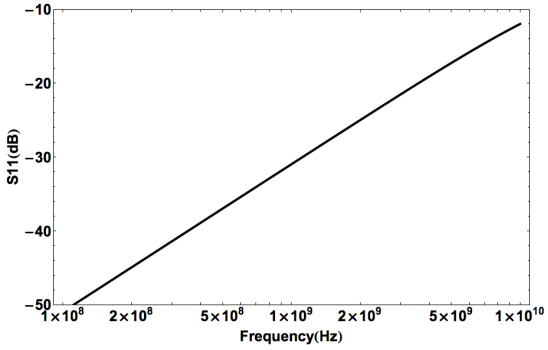


LNA_B Gain (varying C_L)

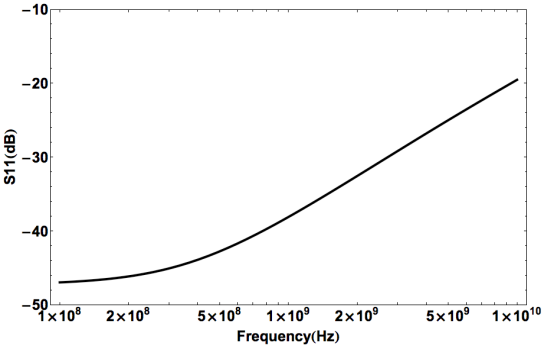
Figure 4-9. Gain of LNA_A and LNA_B for different values of load capacitance. C_f=0F (Black); C_f=50 fF (Red); C_f=100 fF (Green); C_f=500 fF (Blue); C_f=1 pF (Orange).

4.7 Input Matching Analysis

In Figure 4-10, plots of the input matching as a function of frequency for the LNA_A and LNA_B are shown. To obtain these plots, the values of the circuit dimensioning were substituted in equation 4.7 and the resulting equation was then used in equation 2.1 with R_o=50 Ω. Finally, the substitution $s=2j\pi f$ was applied. The absolute value of the result was then plotted using the program *Mathematica* (source code: ANNEX VI). In these plots the load impedance is considered to be infinite, therefore they show the effects of the capacitances C_{gs} and C_{gd} of the transistors.



LNA_A S_{11} ($Z_L \to \infty \leftrightarrow C_L$=0 F)

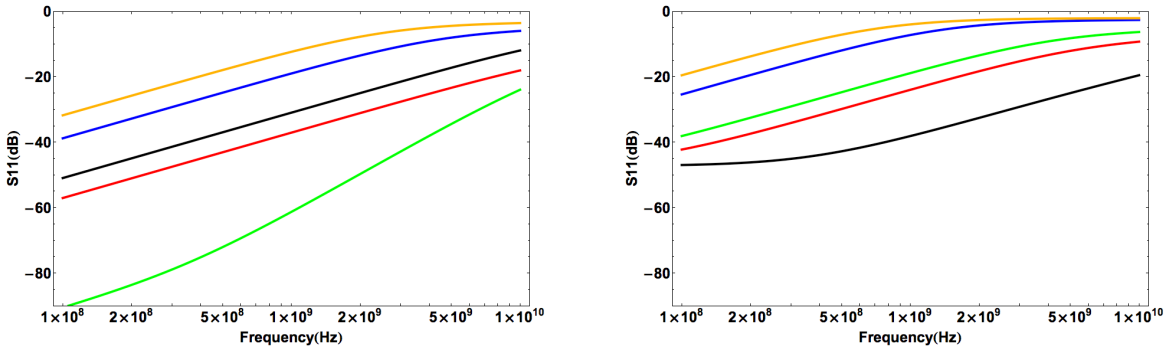


LNA_B S_{11} ($Z_L \to \infty \leftrightarrow C_L$=0 F)

Figure 4-10. S_{11} of LNA_A and LNA_B with infinite load impedance.

A circuit is considered to be input matched if S_{11} is lower than -10 dB. As can be seen from the plots, the effects of the capacitances C_{gs} and C_{gd} of the transistors are not enough to disrupt the input matching of the circuits.

In Figure 4-11, plots of the input matching as a function of frequency for different values of the load capacitance are presented. The plots show that C_L has a significant effect in the input matching of the circuit. For LNA_A the maximum accepted value for the load capacitance is 640 fF (S_{11}=-10.03 dB at 2.4 GHz) while for LNA_B is 140 fF (S_{11}=-9.98 dB at 2.4 GHz). Again, depending in the input impedance of the mixer, a buffer might be required to solve this problem.



LNA_A S_{11} (varying C_L) LNA_B S_{11} (varying C_L)

Figure 4-11. S_{11} of LNA_A and LNA_B for different values of load capacitance. C_L=0 F (Black); C_L=50 fF (Red); C_L=100 fF (Green); C_L=500 fF (Blue); C_L=1 pF (Orange).

4.8 Noise Analysis

For the noise analysis the transistors M_1 and M_3 and the resistances R_1 and R_T were considered to be the main noise sources, being the other noise sources considered negligible.

In equations (4.14) and (4.15), the input noise power spectral density equations are presented. The demonstration of how these equations are obtained can be seen ANNEX V.

$$N_i(f) = \left|1 + g_{m1}\alpha\right|^2 N_{v_{n,R_{fb}}} + \left|\frac{\alpha}{R_T}\right|^2 N_{v_{n,R_T}} + \left|\alpha\right|^2 N_{i_{n,d1}} + \left|g_{m1}\alpha\right|^2 N_{v_{n,R_{g1}}} \quad (4.14)$$

$$+\left|R_{fb} + R_S + g_{m1}R_{fb}\alpha\right|^2 N_{i_{n,d3}} + \left|g_{m3}R_{fb} + g_{m3}R_S + g_{m1}g_{m3}R_{fb}\alpha\right|^2 N_{v_{n,R_{g3}}} \quad \text{LNA\_A}$$

$$N_i(f) = \left|1 + g_{m1}\alpha\right|^2 N_{v_{n,R_{fb}}} + \left|\frac{\alpha}{R_T}\right|^2 N_{v_{n,R_T}} + \left|\alpha\right|^2 N_{i_{n,d1}} + \left|g_{m1}\alpha\right|^2 N_{v_{n,R_{g1}}} + \left|R_S\right|^2 N_{i_{n,d3}} + \left|g_{m3}R_S\right|^2 N_{v_{n,R_{g3}}} \quad (4.15)$$

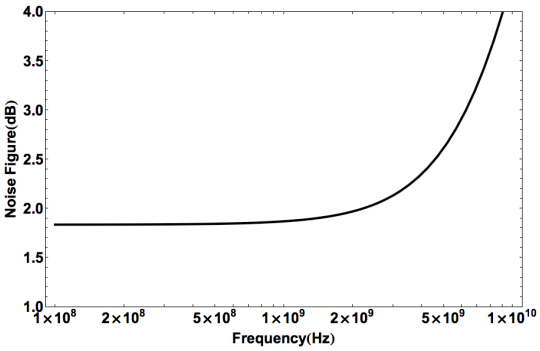
LNA_B

where

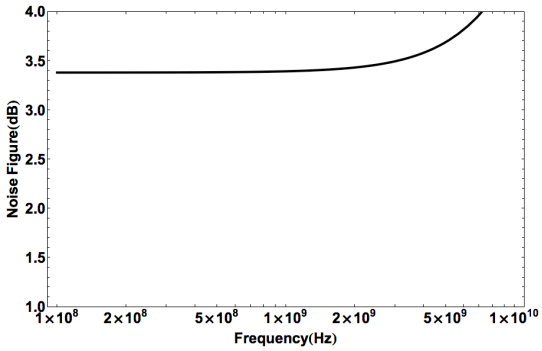
$$N_{v_{n,Rfb}}(f)=4k_BTR_{fb} \quad N_{i_{n,d1}}(f)=4k_BT\gamma g_{m1} \quad N_{v_{n,Rg1}}(f)=4k_BTR_{g1}$$
$$N_{v_{n,RT}}(f)=4k_BTR_T \quad N_{i_{n,d3}}(f)=4k_BT\gamma g_{m3} \quad N_{v_{n,Rg3}}(f)=4k_BTR_{g3} \tag{4.16}$$

The noise figure is then calculated using equation (2.20).

Plots of the noise figure of the LNA_A and LNA_B are shown in Figure 4-12. To obtain these plots, the values of the circuit dimensioning are applied to the equations above, the substitution $s=2j\pi f$ was applied and the absolute value of the result was then plotted using the program *Mathematica* (source code: ANNEX VI). In these plots the load impedance is considered to be infinite, therefore they show solely the effects of the transistor capacitances C_{gs} and C_{gd}.



LNA_A NF ($Z_L \to \infty \leftrightarrow C_L$=0 F)



LNA_B NF ($Z_L \to \infty \leftrightarrow C_L$=0 F)

Figure 4-12. Noise Figure of LNA_A and LNA_B with infinite load impedance.

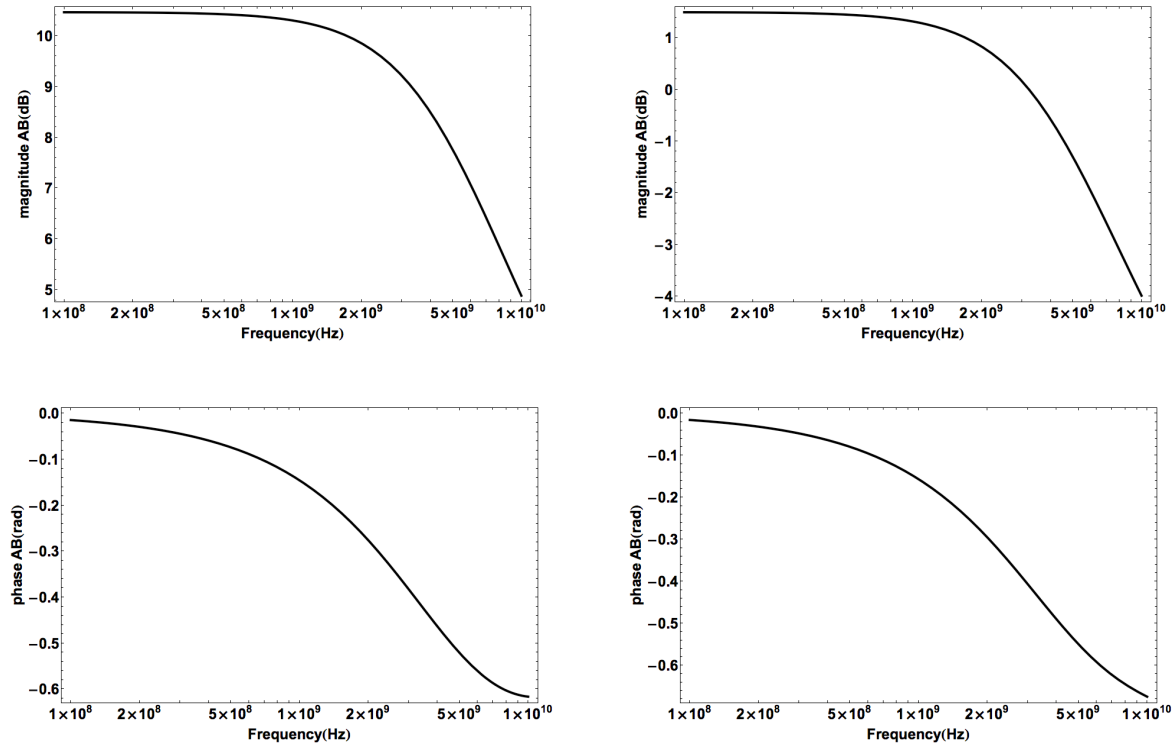
At 2.4 GHz, the noise figure of LNA_A is equal to 2.38 dB while the noise figure of LNA_B is equal to 3.45 dB. The specifications for the LNA require a NF lower than 3 dB, which might be a problem for LNA_B.

There is no need to simulate the noise figure for a varying C_L, as the noise figure equations do not take into account the load impedance and capacitors are noiseless components, theoretically.

4.9 Stability Analysis

To see if the circuits are stable, the frequency response of $A'\beta_{ideal}$ was plotted to measure the amplitude and phase margins. First of all, the values of the circuit dimensioning were substituted in equations (2.30) and the substitution $s=2j\pi f$ was applied. Then, the magnitude and phase of the product of $A'\beta_{ideal}$ was plotted using the program *Mathematica* (source code: ANNEX VI). These plots can be seen in Figure 4-13, where the load impedance is considered to be infinite and therefore they

show the effects of the capacitances C_{gs} and C_{gd} of the transistors.

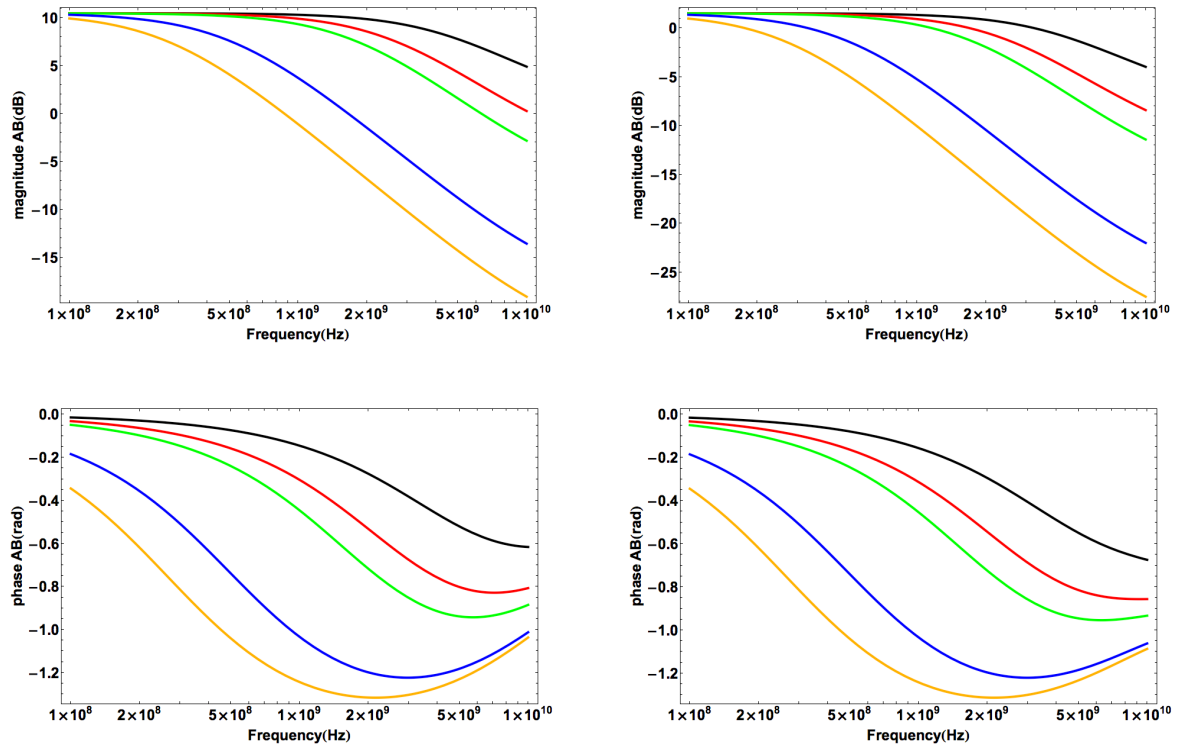


LNA_A ($Z_L \to \infty \leftrightarrow C_L$=0 F) LNA_B ($Z_L \to \infty \leftrightarrow C_L$=0 F)

Figure 4-13. $|A'\beta_{ideal}|$ and $\phi(A'\beta_{ideal})$ of LNA_A and LNA_B with infinite load impedance.

The plots show that the circuits are stable for their operating ranges: for LNA_A the frequencies ω_0 and ω_π do not even appear in the relevant frequency range and for LNA_B ω_0 is equal to 3.20 GHz and the corresponding phase margin is a 2.72 rad or 155.84º.

In Figure 4-14, plots of the product $A'\beta_{ideal}$ as a function of frequency, for different values of the load capacitance, are presented. The plots show that C_L does not create instability in the circuits as the phase margins are, for all values of C_L, positive and large enough.



LNA_A (varying C_L) LNA_B (varying C_L)

Figure 4-14. $|A'\beta_{ideal}|$ and $\phi(A'\beta_{ideal})$ of LNA_A and LNA_B for different values of output capacitance. C_L=0 F (Black) ; C_L=50 fF (Red) ; C_L=100 fF (Green) ; C_L=500 fF (Blue) ; C_L=1 pF (Orange).

4.10 Conclusions

Both circuits appear to be able to satisfy the specifications of the LNA by looking at the results of the theoretical and numerical analysis, exception being the noise figure for LNA_B. Nevertheless, it is also clear that the load impedance has high influence in the circuits, which may lead to the need of using a buffer to separate the LNA and the mixer.

Chapter 5

Choosing the LNA

5.1 Introduction

This chapter details the simulations performed with LNA_A, LNA_B and some variations of those circuits and the reasoning behind the decision to choose LNA_B for the radio. Finally this chapter presents the results of the corner simulations done with the chosen LNA.

5.2 Simulations

5.2.1 LNA_A simulation results

The schematic of the simulated LNA_A is shown in Figure 5-1. From the LNA_A presented in Figure 4-1, some differences are visible. The biasing transistor M_5 is eliminated because from early stages of the dimensioning it became apparent that the feedback loop already stabilized the output node so that there was not a high voltage drop in R_D. Also, increasing the current in M_1 through M_5 to increase the gain of the circuit proved to be a bad trade-off. The other difference between Figure 4-1 and Figure 5-1 is the biasing transistor M_3, which was substituted by a current mirror.

The components used in the circuit are from the UMC 0.13µm library. The NMOS transistors are the N_12_RF component and the resistances are the RNNOP_RF component.

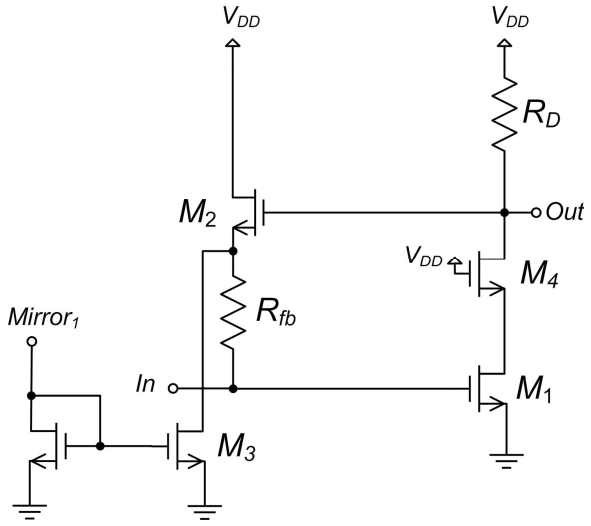


Figure 5-1. Schematic of the simulated LNA_A.

After several iterations, the dimensioning which produces the most balanced result regarding the

specifications was achieved and is presented in Table 5.1, while the results are shown in Table 5.2. It should be noted that the bandwidth parameter in Table 5.2 was calculated as defined in section 2.4.2. In ANNEX VII, plots of the gain, S_{11} and noise figure are presented.

Table 5.1. LNA_A dimensioning.

	W(μm)	L(nm)	Gate Finger	Multiplier
M_1	1.8	120	16	5
M_2	1.8	120	16	1
M_4	1.8	120	16	1
Mirror 1 (M_3 - 1:1)	7.2	130	16	1
R_D = 345.52 Ω		R_{fb} = 154.80 Ω		
I_{ref} of mirror 1 = 0.327 mA				

Table 5.2. LNA_A results.

Current consumption	1.48 mA
Voltage gain at 2.4GHz	15.00 dB
S_{11} at 2.4GHz	-13.32 dB
Noise figure at 2.4GHz	2.52 dB
IIP_3	-16.54 dBm
P_{-1dB}	-12.51 dBm
Bandwidth	5.28-0.09 = 5.19GHz

From the results it is apparent that the circuit while satisfying most of the specifications, fails at providing a higher gain and is very non linear. While a gain of 15 dB is acceptable for a LNA, the value of the IIP_3 is far from the objective of 0 dBm.

5.2.2 MOSFET Only LNA_A simulation results

In an effort to improve the gain of the circuit and also to reduce the circuit area a MOSFET only version of the LNA_A was simulated, where R_D was substituted by a PMOS transistor in the triode zone and R_{fb} was substituted for a NMOS transistor, also in the triode zone. The schematic of the circuit is represented in Figure 5-2.

The components used in the circuit were the same as the ones used in the LNA_A. The PMOS transistor corresponds to the component P_12_RF of the same library.

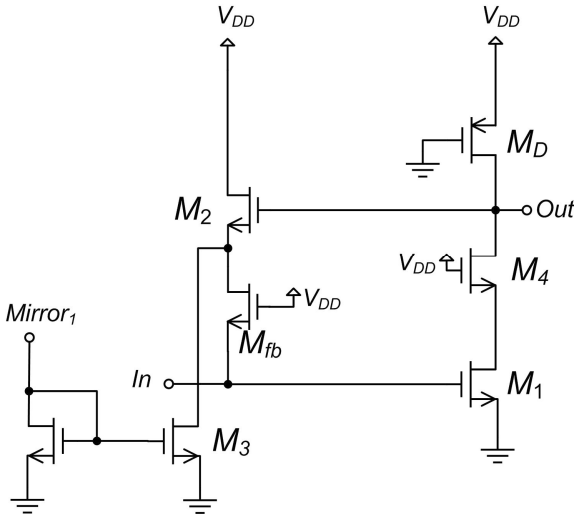


Figure 5-2. Schematic of the simulated MOSFET only LNA_A.

The dimensioning of the circuit is presented in Table 5.3 and the simulation results in Table 5.4, while the plots of the gain, S_{11} and noise figure can be consulted in ANNEX VII.

Table 5.3. Dimensioning of the MOSFET only LNA_A.

	W(μm)	**L(nm)**	**Gate Finger**	**Multiplier**
M_1	1.8	120	16	5
M_2	1.8	120	16	1
M_4	1.8	120	16	1
M_D	2.0	120	2	2
M_{fb}	0.9	120	7	1
Mirror 1 (M_3 - 1:1)	7.2	130	16	1
I_{ref} of mirror 1 = 0.33 mA				

Table 5.4. MOSFET only LNA_A results.

Current consumption	1.66 mA
Voltage gain at 2.4GHz	17.16 dB
S_{11} at 2.4GHz	-11.83 dB
Noise figure at 2.4GHz	2.16 dB
IIP_3	-15.81 dBm
P_{-1dB}	-17.18 dBm
Bandwidth	3.17-0 = 3.17 GHz

The results show that while it is possible to improve the gain of the circuit using the PMOS transistors instead of the resistances, the linearity problem remains and is aggravated by a worse P_{-1dB} as a consequence of the use of non-linear components instead of resistors.

5.2.3 LNA_B simulation results

The schematic of the simulated LNA_B is shown in Figure 5-3. From the LNA_B represented in Figure 4-1, the biasing transistors M_3 and M_5 are substituted by current mirrors, while the rest of the circuit remains identical.

The components used in the circuit are from the UMC 0.13µm library. The NMOS transistors are the N_12_RF component, the resistances are the RNNOP_RF component and the capacitor is the MOMCAPS_RF component.

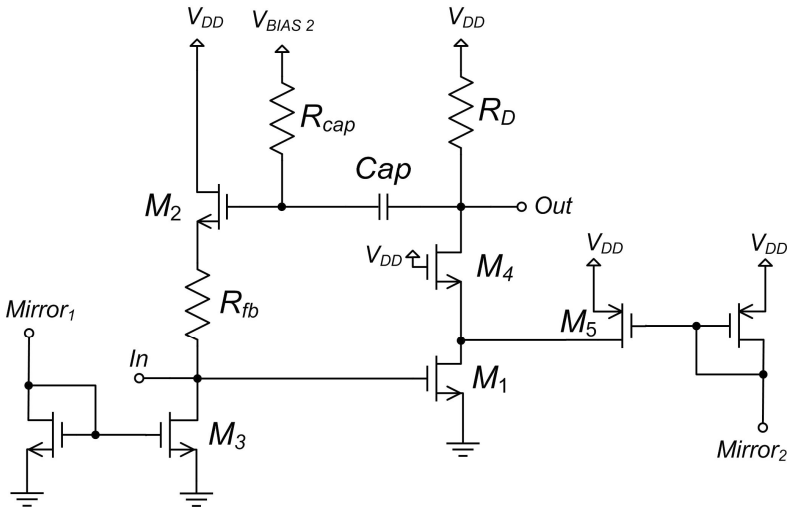


Figure 5-3. Schematic of the simulated LNA_B.

The dimensioning of the circuit is presented in Table 5.5 and the simulation results in Table 5.6, while the plots of the gain, S_{11} and noise figure can be consulted in ANNEX VII.

Table 5.5. Dimensioning of LNA_B.

	W(µm)	L(nm)	Gate Finger	Multiplier
M_1	1.8	120	16	5
M_2	3.0	130	4	2
M_4	1.8	120	16	1
Mirror 1 (M_3 - 1:1)	2.4	260	4	1
Mirror 2 (M_5 - 1:1)	4.0	130	6	1
R_D = 344.84 Ω	***R_{fb}*** = 403.57 Ω	***R_{cap}*** = 1.51 kΩ	***Cap*** = 142.25 fF	
I_{ref} of mirror 1 = 0.655 mA.		***I_{ref}*** of mirror 2 = 0.922 mA		

Table 5.6. LNA_B results.

Current consumption	2.68 mA
Voltage gain at 2.4GHz	16.50 dB
S_{11} at 2.4GHz	-11.77 dB
Noise figure at 2.4GHz	2.66 dB
IIP_3	-4.97 dBm
P_{-1dB}	-21.84 dBm
Bandwidth	3.95-1.01 = 2.94 GHz

The results show that regarding linearity, this circuit is superior to the LNA_A, while having similar results in most of the other parameters. The disadvantages are a higher current consumption and higher area due to the increase of the number of components.

5.2.4 LNA_C simulation results

In Figure 5-4, a variation of the studied circuits is presented. In this circuit a capacitor is included at the gate of M_1, so that the feedback loop is disconnected at low frequencies and therefore allowing an independent dimensioning of the amplifying and feedback blocks. The biasing of the M_1 transistor is done by the current mirror, which defines the current in the amplifying block.

The components used in the circuit are from the UMC 0.13 µm library. The NMOS transistors are the N_12_RF component, the resistances are the RNNOP_RF component and the capacitor is the MIMCAPS_RF component.

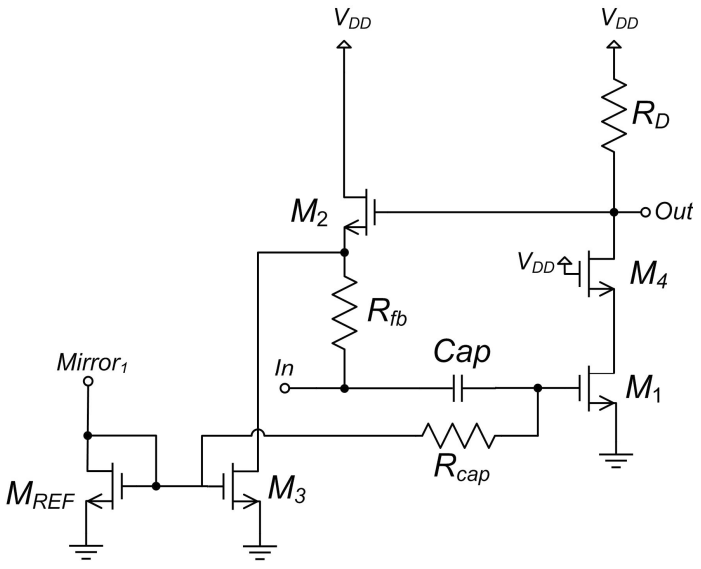


Figure 5-4. Schematic of the simulated LNA_C.

The sizes of the components are presented in Table 5.7 and the simulation results in Table 5.8. It

should be noted that in the bandwidth calculation a threshold of 3.25 dB was considered for the noise figure, as the circuit never goes below the 3 dB mark. In ANNEX VII, plots of the gain, S_{11} and noise figure can be consulted.

Table 5.7. Dimensioning of LNA_C.

	W(μm)	L(nm)	Gate Finger	Multiplier
M_1	1.8	120	16	5
M_2	4.0	130	3	2
M_4	1.8	120	16	1
Mirror 1 (M_3)	0.9	120	16	4
Mirror 1 (M_{Ref})	0.9	120	16	1
R_D = 134.71 Ω	R_{fb} = 272.64 Ω	R_{cap} = 567.85 Ω	**Cap** = 2.02 pF	
I_{ref} of mirror 1 = 0.157 mA				

Table 5.8. LNA_C results.

Current consumption	2.64 mA
Voltage gain at 2.4GHz	10.14 dB
S_{11} at 2.4GHz	-10.75 dB
Noise figure at 2.4GHz	3.18 dB
IIP_3	-0.54 dBm
P_{-1dB}	-14.93 dBm
Bandwidth	3.62-1.26 = 2.36 GHz

The results obtained are disappointing in regards to the gain of the circuit. Nevertheless this circuit presents some interesting characteristics such as great linearity and narrowband behaviour (see ANNEX VII), which is a result of the capacitor at the gate.

5.3 Choosing the LNA

To help make the decision of which LNA should be chosen for the radio receiver, figures of merit (FoM) of the several options were calculated. The FoM expressions used can be seen in [20] and are reproduced in (5.1) and (5.2). (5.1) does not take into account linearity, while (5.2) does.

$$\mathrm{FoM}_1 = 20\log_{10}\left(\frac{\mathrm{BW[GHz]}\cdot \mathrm{Gain[linear]}}{P_{DC}\,[\mathrm{mW}]\cdot (F-1)}\right) \tag{5.1}$$

$$\mathrm{FoM}_2 = 20\log_{10}\left(\frac{\mathrm{BW[GHz]}\cdot \mathrm{Gain[linear]}\cdot \mathrm{IIP_3[mW]}}{P_{DC}\,[\mathrm{mW}]\cdot (\mathrm{F}-1)}\right) \tag{5.2}$$

The results obtained using the FoM formulas above are presented in Table 5.9. The table clearly shows that if linearity is not taken in account, LNA_A and its MOSFET only version are the best options due to their lower current consumption. But if linearity is considered, then LNA_B is the most balanced circuit. Finally, the LNA_C results show that despite its great linearity, it has too many shortcomings to be considered as a viable option.

Table 5.9. FoM results of the LNAs.

	$\mathrm{FoM_1}$	**$\mathrm{FoM_2}$**
LNA_A	**26.40**	-6.68
MOSFET only LNA_A	25.01	-6.61
LNA_B	17.18	**7.24**
LNA_C	6.92	5.84

After some consideration, LNA_B was the chosen LNA to be implemented in the radio receiver. It failed to satisfy all the initial specifications (Table 4.1), being the most problematic the current consumption. Nevertheless, the 2.64 mA of current consumption for the LNA was considered acceptable and within the “budget” for the whole radio receiver.

5.4 LNA_B Corner simulation results

CMOS technologies suffer from substantial parameter variations from wafer to wafer and from lot to lot, known as process corners, which affect the performance of a circuit [21]. In order to verify the robustness of the LNA_B, several simulations of the circuit were performed for different process corners as well as supply voltage and temperature variations (PVT variations). These simulations are presented in Table 5.10, while the results can be seen in Table 5.11.

Table 5.10. Corner simulations performed.

	Transistors	Resistors	Capacitors	Temp [ºC]	V_{DD} [V]
Typical	Typ	Typ	Typ	27	1.2
Corner 1	FastFast	Max	Max	-30	1.32
Corner 2	FastFast	Min	Min	-30	1.32
Corner 3	SlowSlow	Max	Max	120	1.08
Corner 4	SlowSlow	Min	Min	120	1.08
Corner 5	FastSlow	Max	Max	-30	1.32
Corner 6	FastSlow	Min	Min	-30	1.32
Corner 7	FastSlow	Max	Max	120	1.08
Corner 8	FastSlow	Min	Min	120	1.08
Corner 9	SlowFast	Max	Max	-30	1.32
Corner 10	SlowFast	Min	Min	-30	1.32
Corner 11	SlowFast	Max	Max	120	1.08
Corner 12	SlowFast	Min	Min	120	1.08

Table 5.11. Corner simulations results.

	Gain [dB]	Current consumption [mA]	S_{11} [dB]	NF [dB]
Typical	16.50	2.68	-11.77	2.66
Corner 1	15.87	3.51	-10.92	1.99
Corner 2	-7.35	7.48	-3.02	4.53
Corner 3	-32.14	0.84	-2.70	43.17
Corner 4	9.99	1.75	-6.72	5.18
Corner 5	17.35	2.26	-10.91	2.50
Corner 6	3.99	6.78	-4.97	2.54
Corner 7	13.02	2.78	-7.60	2.78
Corner 8	-0.67	5.05	-3.55	4.66
Corner 9	-37.04	1.60	-2.23	45.84
Corner 10	16.93	3.29	-15.34	2.48
Corner 11	-7.13	1.22	-3.82	19.11
Corner 12	13.84	3.01	-9.66	3.44

The results show that the circuit is quite susceptible to some of these worst-case scenarios. This fragile behaviour of the circuit is consequence of its aggressive dimensioning, which aimed to maximize the performance of the circuit in typical conditions. Nevertheless, the circuit can be easily adjusted by varying the reference currents in the current mirrors, which for testing purposes are defined by external variable resistances connected to the circuit.

Some examples of these adjustments are shown in Table 5.12.

Table 5.12. Corner simulations results with adjusted reference current.

	Gain [dB]	Current consumption [mA]	S_{11} [dB]	NF [dB]	Reference current [mA]
Corner 2	15.39	5.20	-13.77	2.27	1.30
Corner 3	13.39	2.30	-6.21	3.14	0.28
Corner 8	12.74	4.11	-10.58	2.97	0.93
Corner 9	19.38	2.50	-12.83	2.23	0.51
Corner 11	15.24	1.92	-6.92	3.72	0.45

The LNA is therefore considered to be appropriate for non-critical applications.

In addition to corner analysis, Monte Carlo analyses are usually done for analog circuits. Unfortunately, this type of analysis is unavailable for UMC 0.13µm technology at the time of this writing.

5.5 Conclusions

LNA_B was chosen as the LNA to be implemented in the radio receiver because it was the most capable of fulfilling the desired specifications. To further analyze this LNA, corner simulations were performed to measure how its performance was affected by variation of parameters and it was found that the LNA is suited for non-critical applications as desired.

Chapter 6

Implementing the LNA

6.1 Introduction

This chapter details the steps for implementing the chosen LNA. In section 6.2, the LNA is connected directly to the mixer, showing the need for a buffer between the blocks. In section 6.3, an output stage for the LNA for standalone testing purposes is presented, while in section 6.4, the extra circuitry added to the blocks to prevent electrostatic discharges is shown. Section 6.5 deals with the final pre-layout simulations that take into account the pads and the bonding wires. The final LNA layout it shown in section 6.6 and finally the radio receiver is presented in section 6.7.

6.2 Connecting the LNA to the mixer

The first step of the LNA implementation for the radio receiver is to see how the performance of the LNA is affected by connecting it to the mixer block. To do so, the LNA was connected to an instance of the final schematic of the mixer block. The results are shown in Table 6.1.

Table 6.1.LNA results comparison between connecting the LNA directly to the mixer block and connecting it to an infinite resistance.

	LNA connected to the mixer	**LNA connected to ∞ resistance**
Current consumption	2.68 mA	2.68 mA
Voltage gain at 2.4 GHz	10.54 dB	16.50 dB
S_{11} at 2.4 GHz	-5.67 dB	-11.77 dB
Noise figure at 2.4 GHz	2.75 dB	2.66 dB

As predicted in chapter 4, the performance of the LNA is deeply affected by the load impedance from the mixer. As show in ANNEX IV, the input impedance of the mixer is approximately 1 kΩ, where the output impedance of the LNA is approximately equal to R_D (R_D=344 Ω). Therefore, the input impedance of the mixer cannot be considered infinite when compared to R_D, with consequent deterioration of the LNA results, especially regarding impedance matching and voltage gain. The proposed solution consists in using a common drain stage as a buffer between the LNA and the mixer.

Buffer between the LNA and the mixer

The schematic of the buffer between the LNA and the mixer is represented in Figure 6-1.

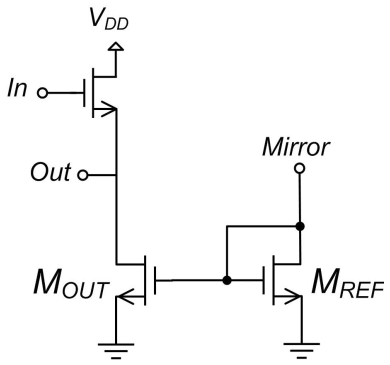


Figure 6-1. Buffer schematic.

The sizes of the components are presented in Table 6.2, while the simulation results are shown in Table 6.3 and Table 6.4. In Figure 6-2, the connections between the LNA, the buffer and the mixer are detailed.

Table 6.2. Dimensioning of the buffer.

	W(μm)	L(nm)	Gate Finger	Multiplier
M_{IN}	7	120	16	1
M_{OUT}	5.5	120	12	1
M_{REF}	2	120	4	1
I_{ref} in M_{REF} = 155 μA				

Table 6.3. Buffer results.

	Buffer
Current consumption	1.44 mA
Voltage gain at 2.4 GHz	-3.03 dB

Table 6.4.Results of different connection scenarios for the LNA.

	LNA connected to ∞ resistance	LNA connected to the mixer	LNA+Buffer connected to the mixer
Current consumption	2.68 mA	2.68 mA	(2.68 + 1.44) = 4.12 mA
Voltage gain at 2.4 GHz	16.50 dB	10.54 dB	12.92 dB
S_{11} at 2.4 GHz	-11.77 dB	-5.67 dB	-10.21 dB
Noise figure at 2.4 GHz	2.66 dB	2.75 dB	2.67 dB

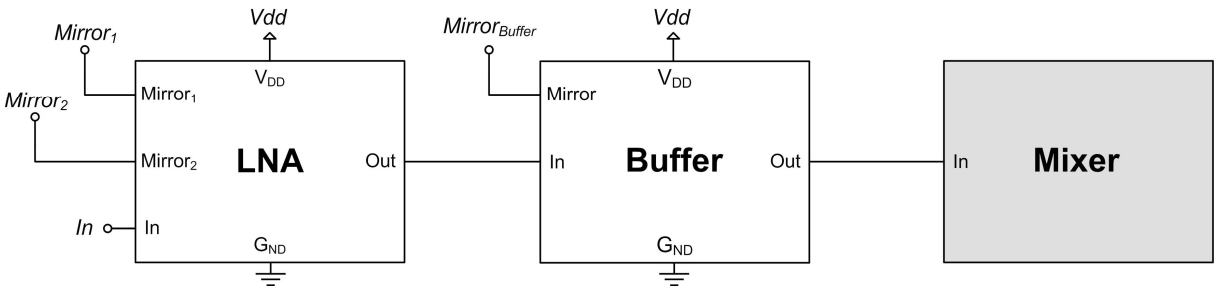


Figure 6-2. LNA, buffer and mixer connections.

The results show that using a buffer comes at a cost of lower voltage gain and higher current consumption. Nevertheless, it is a necessary component if one wishes to connect an LNA to the mixer. The gain reduces to 13 dB, while representing a significant reduction it does not compromise the functioning of the radio receiver, but the increased current consumption is far from ideal. A possible future work could be focused around the optimization of the connections between circuit blocks as most articles only deal with a single block and ignore the hardships of building complete systems with interconnected blocks.

6.3 Output stage for testing purposes

The LNA is not going to be produced standalone but the radio receiver is. Therefore, an output stage for the LNA will be included in the radio receiver testing samples to allow the measurement of the LNA. The output stage is simply a NMOS transistor with its gate connected to the output of the LNA (its high input impedance doesn't affect the performance of the LNA) and the output corresponds to the source of the transistor.

6.4 Protection against electrostatic discharges

Electrostatic discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field [22]. ESD is a serious issue in integrated circuits, which can suffer permanent damage when subjected to high voltages. A common example of a possible ESD scenario can happen when a person touches the circuit. This leads to the need of adding ESD protection diodes to the circuits.

The ESD protection diodes were connected to the gates of the transistors that are directly connected to pads, because these are the most sensitive parts of the circuit. The schematic of the ESD

protection circuit is shown in Figure 6-3, while the dimensioning of the components is detailed in Table 6.5. In Figure 6-6, the test bench for the bonding wires and pads simulation is shown and the ESD components are there represented.

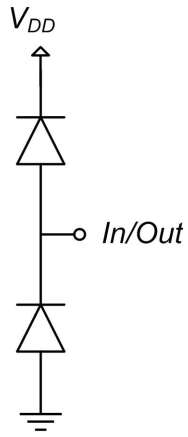


Figure 6-3. ESD protection diodes.

Table 6.5.ESD protection diode dimensioning.

	W(nm)	**L(μm)**	**Multiplier**
Diode	600	120	1
Component name: DI0DN_ESD_RF			

Another sensitive part of the LNA corresponds to the biasing of the transistor M_4, which is directly connected to V_{DD}. In this case, a pull-up circuitry was added to indirectly bias the transistor with V_{DD}, and consequently protect it from possible current discharges. This pull-up circuit can be seen in Figure 6-4 and the dimensioning in Table 6.6.

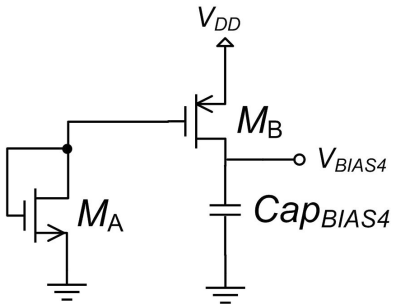


Figure 6-4. M_4 Pull-up circuit.

Table 6.6. Dimensioning of the M_4 pull-up circuit.

M_A: l = 120 nm ; W = 2 µm ; Finger number = 1 ; Source Drain Metal Width = 280 nm ***Component name***: N_LV_12_HSL130E
M_B: l = 120 nm ; W = 2 µm ; Finger number = 1 ; Source Drain Metal Width = 280 nm ***Component name***: P_LV_12_HSL130E
Cap_{BIAS4}: W=50 µm ; Finger number = 20 ; Nº metal layer = 3 ; Finger Width = 200 nm ***Component name***: MOMCAPS_RF

6.5 LNA testing with bonding wires and pads

The bonding wires and pads can affect the performance of the LNA and of the radio receiver. One zone that is very sensitive to the bonding parasitic inductance is the power supply. This parasitic inductance will be connected in series between either V_{DD} and G_{ND} and the circuit. One way to minimize it consists of increasing the number of pads and having several bonding wires in parallel. Therefore it is important to test the circuit varying the number of pads to measure the minimum number that guarantees the correct functioning of the LNA. The bonding wire model used is shown in Figure 6-5 and its dimensioning can be seen in Table 6.7.

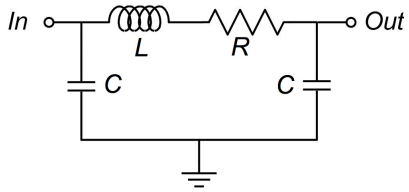


Figure 6-5. Bonding wire model.

Table 6.7. Bonding wire model.

	Bonding wire
Resistance	400 mΩ
Capacitance	100 fF
Inductance	2.1 nH

The schematic of the LNA, buffer and output stage with the pads, bonding wires and ESDs included is shown in Figure 6-6. It was found that the minimum number of V_{DD} and G_{ND} pads that result in no performance degradation was three, as shown in the figure.

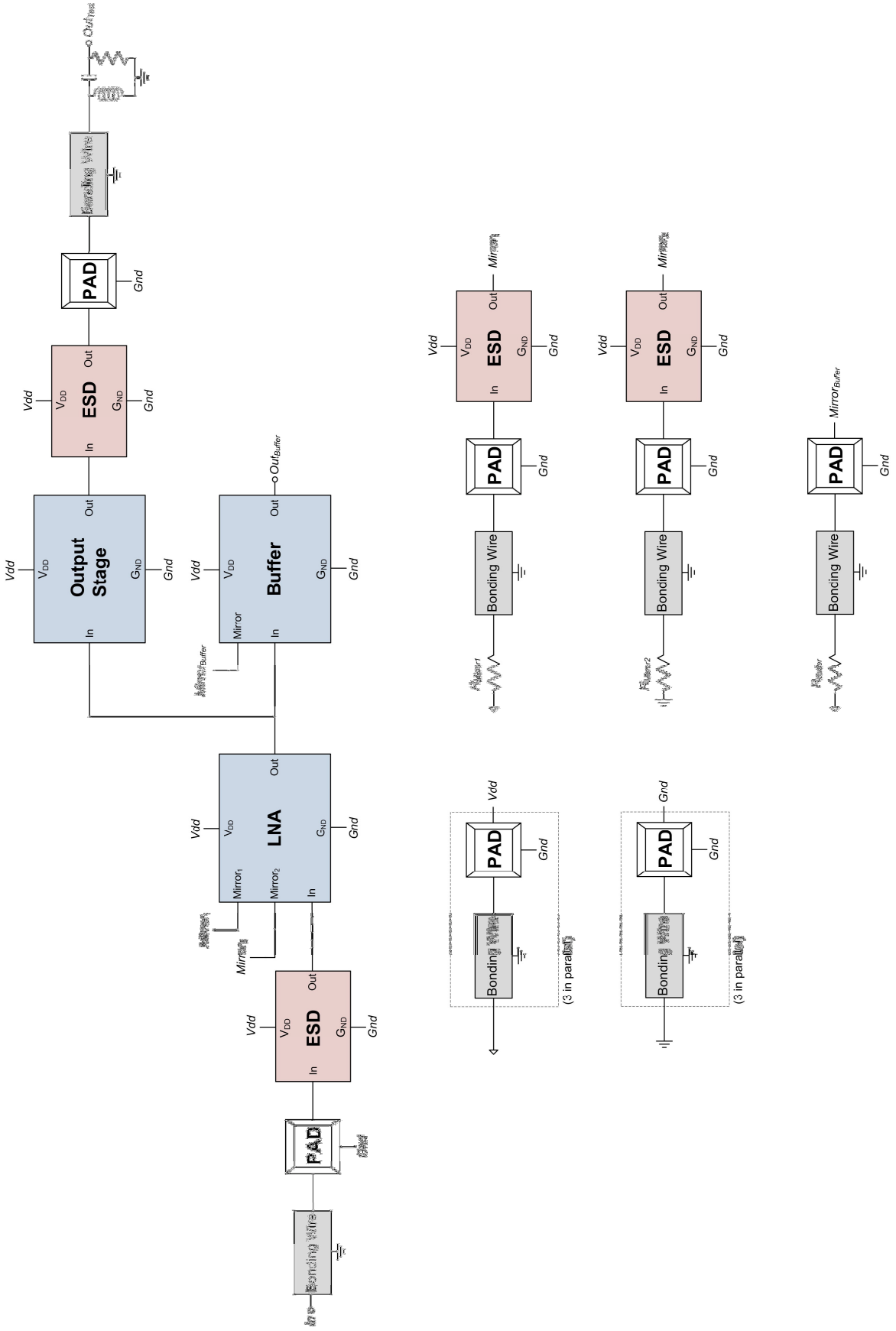


Figure 6-6. Schematic of the LNA, buffer and output stage with pads, bonding wires and ESDs included.

6.6 Layout design

The schematic of the circuit corresponding to the layout is shown in Figure 6-7.

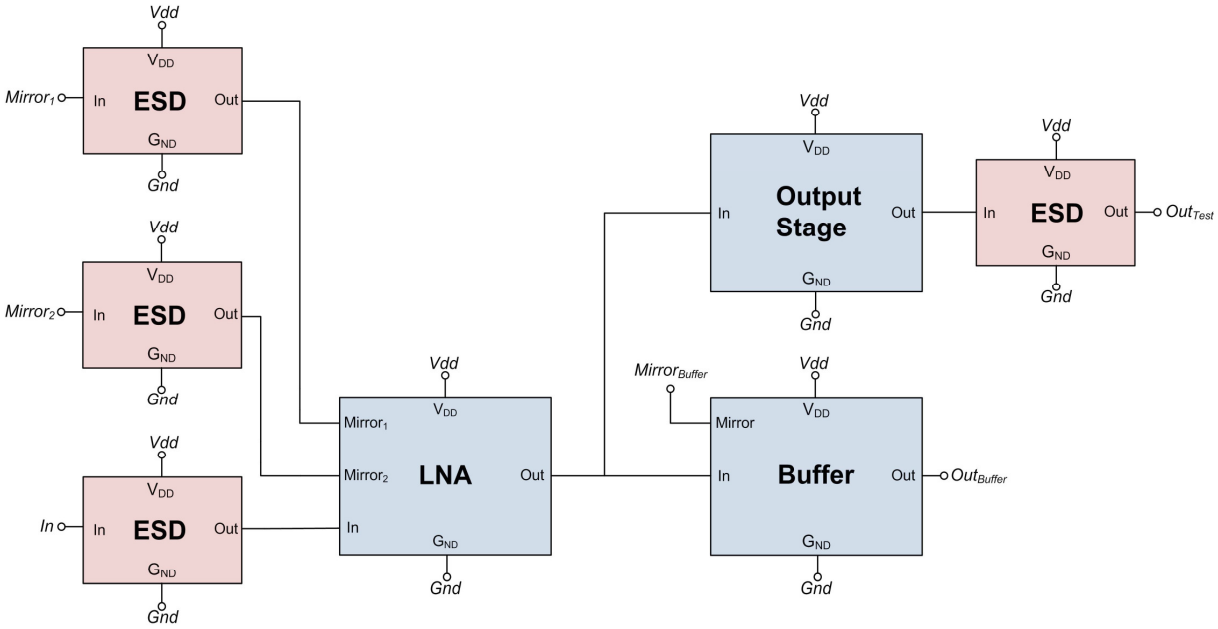


Figure 6-7. Layout schematic.

For the layout design the following precautions were taken:

- the connections to the substrate are distributed along the circuit to reduce parasitic effects and improve the biasing of the substrate;
- maximization of the connections between metal layers to decrease resistance and guard against possible manufacturing errors;
- all connections were designed to support a current higher than expected;
- connections were kept small and straight to decrease their resistance and parasitic effects;
- a guard ring was implemented to reduce noise, improve isolation and improve substrate biasing.

The layout design is shown in Figure 6-8 and has an area of 75 µm x 155 µm = 0.011625 mm^2.

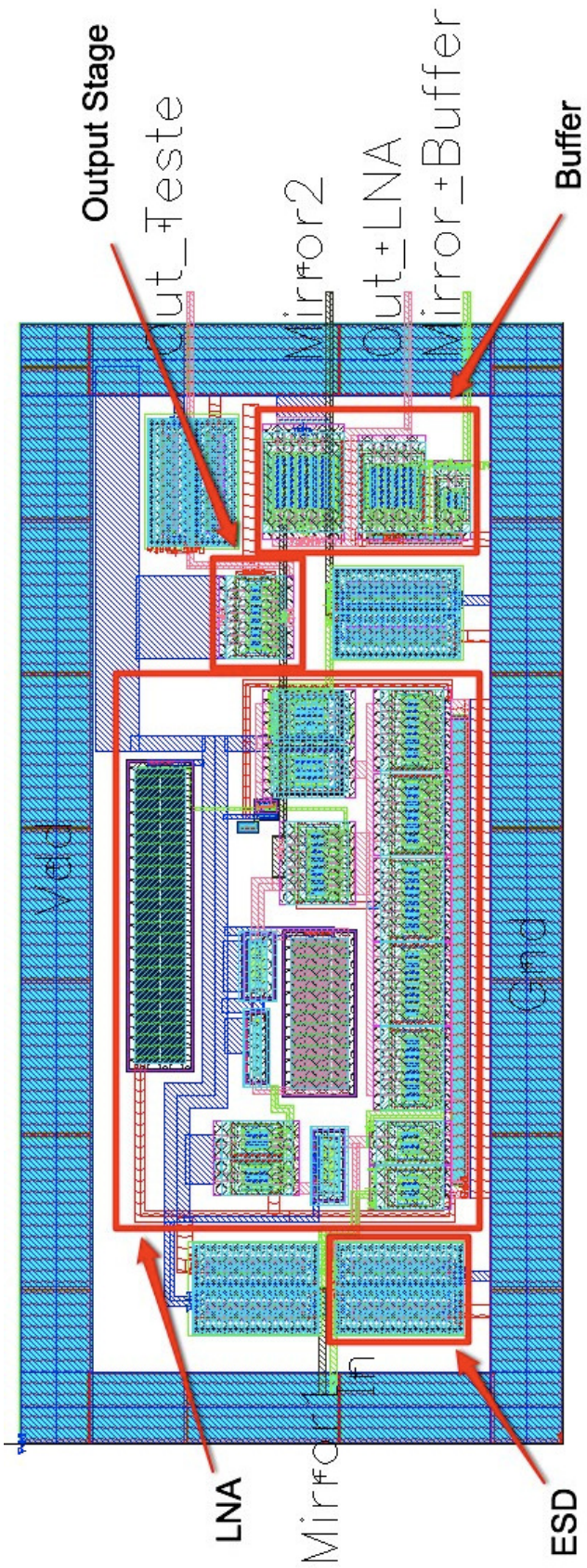


Figure 6-8. Layout design.

This layout does not show the pads, as they are located at the radio receiver layout level.

6.7 Radio receiver analog frontend

The schematic of the full radio receiver analog frontend is presented in Figure 6-9, including pads and bonding wires. The mixer block is a crossed-coupled relaxation oscillator with incorporated mixing capabilities, commonly called an Osmix, and its study and development can be consulted in [24]. The filter block is a low-pass G_m-C Butterworth filter with a 25 MHz cut-off frequency and can be consulted in [25].

The final results for the radio receiver are presented in Table 6.8 and an input/output plot of a signal discrete Fourier transformation in shown in Figure 6-9, from where the overall gain can be calculated (-11.52 – (-39.01) = 27.5 dB). The radio receiver operates at 2.41 GHz and down-converts the input signals to 10 MHz.

Table 6.8. Radio receiver results.

	LNA	**LNA Buffer**	**Mixer (Osmix)**	**Filter**	**Radio Receiver**
Gain [dB]	15.3	-2.9	1.2 [1]	14.0	27.6
Current consumption [2] [mA]	2.68	1.44	1.98	3.90	13.55
Circuit area (mm^2)	0.011625		0.013245	0.025851	0.39 [3]

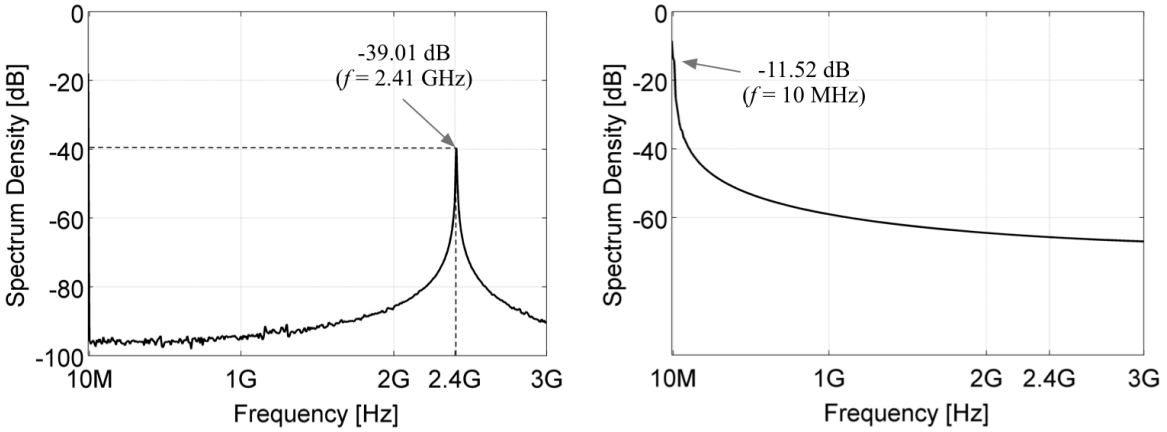


Figure 6-9. Radio receiver input/output plot of a signal discrete Fourier transformation.

[1] This gain is the voltage conversion gain defined as the ratio between the rms voltage of the IF signal and the rms voltage of the RF signal. f_{IF}= 10 MHz ; f_{RF}= 2.41 GHz.

[2] The current consumption of the radio receiver includes the current from the reference branches of the current mirrors.

[3] The area of the radio receiver includes the pads.

The schematic of the radio receiver is presented in Figure 6-10 and the layout design is shown in Figure 6-11.

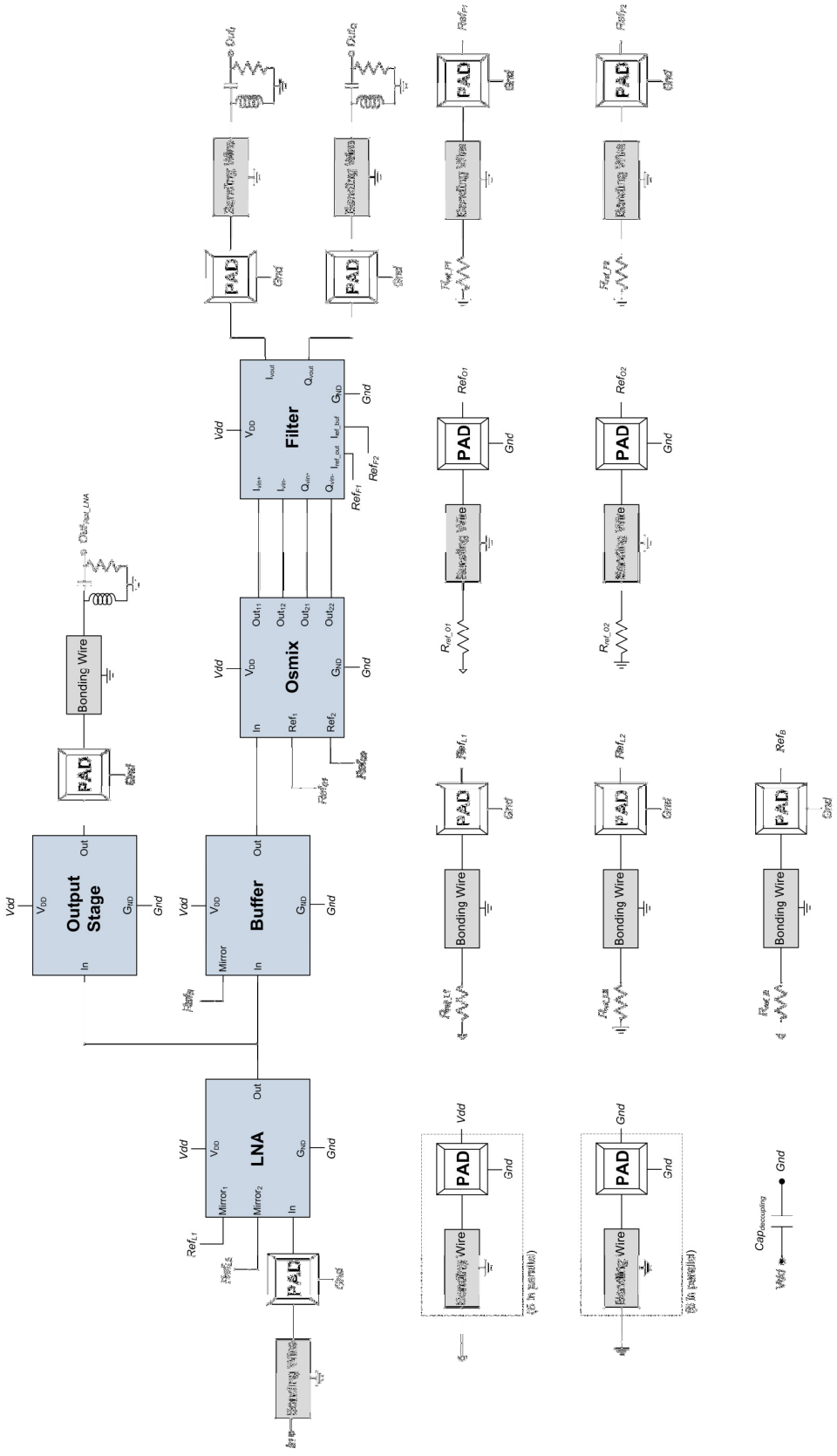


Figure 6-10. Schematic of the radio receiver with pads and bonding wires included.

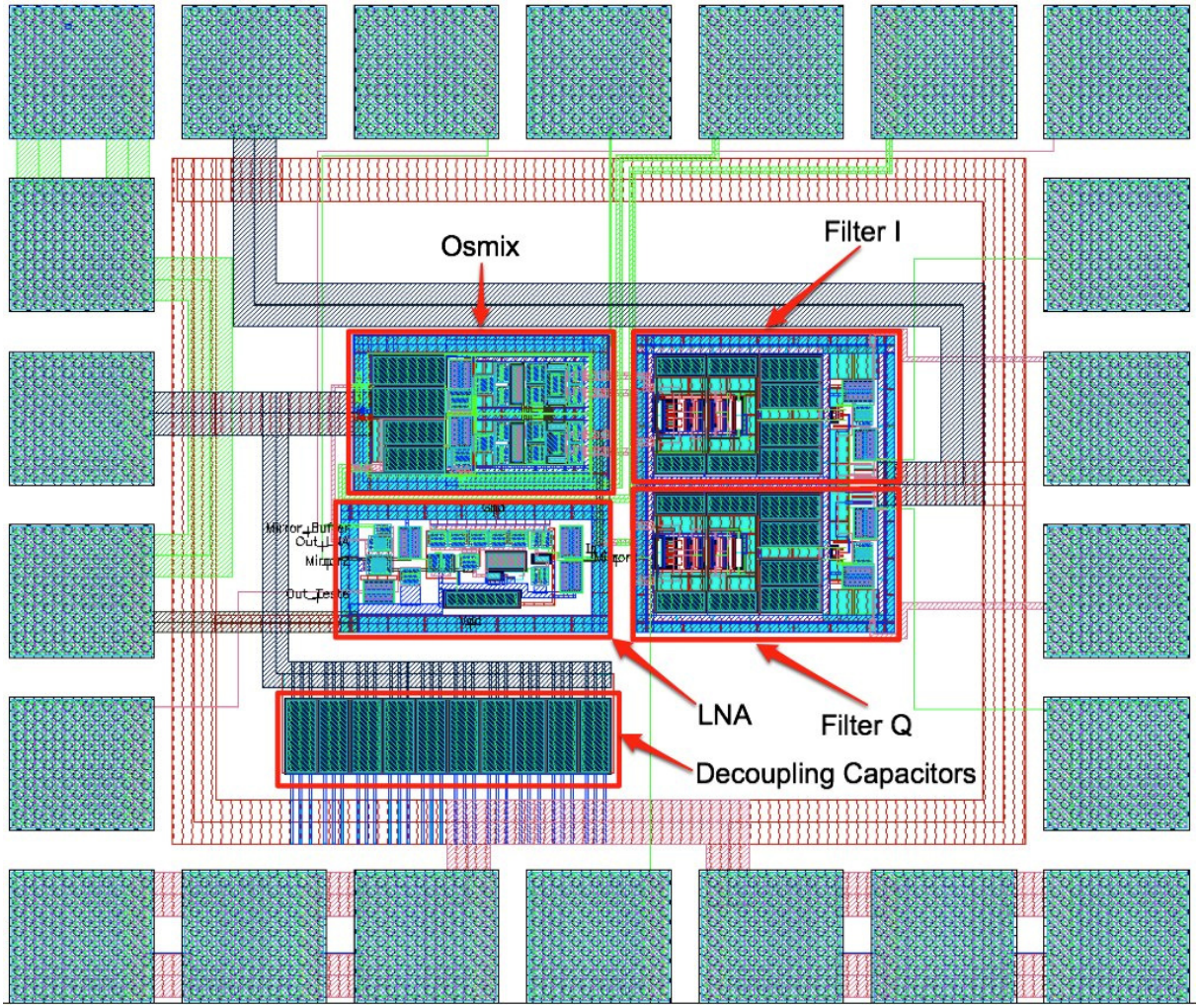


Figure 6-11. Layout of the radio receiver.

In Table 6.9, a comparison of the implemented radio receiver with a radio receiver presented in [19] is presented. The results show that the implemented radio receiver is very competitive, achieving higher gain and lower power consumption, while having a smaller circuit area.

Table 6.9.Results comparison between two radio receivers.

	Implemented radio receiver	**Radio receiver presented in [19]**
Technology	UMC 130 nm	UMC 130 nm
V_{DD} (V)	1.2	1.2
Gain (dB)	27.6	20
Current consumption (mA)	13.55	146.67
Circuit area (mm^2)	0.39	0.48

6.8 Conclusions

In this chapter, the steps taken to implement the LNA were detailed. As predicted in the chapters before it is impossible to connect the LNA directly to the mixer block due to severe performance degradation caused by its low input impedance. Therefore, a buffer was designed to minimize this problem at the cost of increased current consumption and slightly lower voltage gain.

As the first samples of the radio receiver will be used for testing purposes, an output stage was added to allow the testing of the LNA.

To prevent electrostatic discharges extra circuitry was added to the blocks, such as ESD diodes and a pull-up circuit to M_4 to avoid connecting the gate directly to V_{DD}.

Some simulations were performed to measure the effect of the bonding wires and pads in the circuit. It was found that the minimum number of pads for V_{DD} and G_{ND} that allow the functioning of the circuit without performance degradation was three.

Finally, the layout of the LNA block and of the radio receiver was presented. The LNA has an area of area of 0.011625 mm^2 and the radio receiver has an area of 0.39 mm^2.

Chapter 7

Conclusions

7.1 Conclusions

The objective of this work was to implement a low noise amplifier for the analog frontend of a radio receiver operating in the 2.4 GHz ISM band using 0.13 μm CMOS technology. This analog frontend is to be used in ongoing projects at INESC-ID with focus in portable non-critical applications and has as its key features low cost and low power. In order to accommodate those demands, a focus was put in inductorless LNAs with feedback because these circuits while capable of achieving input matching with the antennas' output impedance do not use inductors. This is a significant advantage because the high area of an inductor is translated directly in an increased cost of the circuit.

Two circuits in particular were considered as possible options for the LNA and they are presented in chapter 4, where a theoretical analysis of these circuits was performed. The proposed LNAs use shunt-shunt feedback topologies, being the main difference between them using or not a capacitor to disconnect the feedback loop for low frequencies. This creates a trade-off between area and more freedom in the dimensioning constraints. The gain and input impedance expressions were determined and a first dimensioning of the circuits was produced. The gain, input impedance, noise and stability analyses in function of frequency indicated that both circuits were capable of satisfying the specifications. Therefore, the circuits along with some variations of them were dimensioned and simulated (chapter 5). The LNA that achieved the best overall results was the one first discussed in [19] and a decision to implement it was reached. Corner simulations of the chosen LNA showed that the circuit was acceptable for non-critical applications.

During the LNA implementation, circuit changes were performed with the inclusion of biasing transistors and protection against electrostatic discharges. It was found that connecting directly the LNA to the mixer block resulted in severe performance degradation, which lead to designing a buffer between the blocks to attenuate the problem. The cost of this buffer was an increased current consumption of the radio receiver and a slightly decreased voltage gain at the input of the mixer block.

An output stage was also designed to allow testing of the LNA block in the radio receiver testing samples.

Finally, the circuit layout was designed with a final active area of 75x155 μm^2 for the LNA plus buffer and output stage and thus providing huge area savings when compared with LNAs that use inductors. The radio receiver was also presented and has an area of 0.39 mm^2, including pads.

A comparison between the implemented LNA and other LNA implementations is presented in Table 7.1.

Table 7.1.Results comparison between different LNAs.

	Implemented LNA	**LNA presented in [19]**	**LNA presented in [20]**
Technology (nm)	130	130	90
V_{DD} (V)	1.2	1.4	1.2
Power consumption (mW)	3.2	25.0	9.7
Voltage gain (dB)	16.50 @2.4 GHz	17.00 @1 GHz	16.50 @1 GHz
Min Noise figure (dB)	2.60	2.40	2.70
IIP_3 (dBm)	-4.97	-4.1	-2
Bandwidth (GHz)	1.26-3.62	0-6.5	1-7

The comparison between the implemented LNA and the original LNA presented in [19] shows a substantial decrease in power consumption due to dimensioning the circuit specifically to the 2.4 GHz ISM band. Even considering the current from the reference transistors of the current mirrors (which raise the power consumption to 5.11 mW), the implemented LNA still has a power consumption five times smaller than the one presented in [19]. The implemented LNA also remains competitive with the LNA presented in [20], which uses a more advanced technology. Thus, the objective of this work to implement a low power and low cost LNA for the 2.4GHz ISM band was successfully achieved.

7.2 Future work

When designing a LNA, the connectivity of the circuit with other blocks is not always the first concern. Nevertheless, these challenges appear when designing a whole radio receiver. If one designs a radio receiver by simply connecting different blocks there will be design inefficiencies such as excess of current mirrors and buffer blocks. Improving the current radio receiver by minimizing the current mirrors and improving the connectivity of the blocks, would be translated in lower current consumptions and smaller areas, and seems like an area where further investigation would be worthwhile.

Regarding the LNA block, further investigation is proposed by dimensioning the studied circuits in smaller transistors technologies, with potential to further decrease the power consumption of the circuits and its area.

Annexes

ANNEX I. 2-port matrices

In Table A.1, the five most used 2-port matrix descriptions are represented [10]. The voltages and currents are related to Figure 2-5, which is reproduced here for convenience.

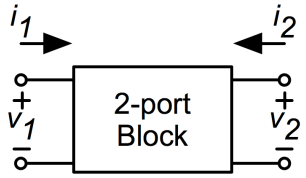


Figure A-1. 2-port block.

Table A.1. Most used 2-port matrix descriptions.

Reference	Matrix description	Name
Y	$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$	Admittance Matrix
Z	$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$	Impedance Matrix
H	$\begin{bmatrix} v_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ v_2 \end{bmatrix}$	Hybrid Matrix
H'	$\begin{bmatrix} i_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} h'_{11} & h'_{12} \\ h'_{21} & h'_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ i_2 \end{bmatrix}$	Dual Hybrid Matrix
T	$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} t_{11} & t_{12} \\ t_{21} & t_{22} \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix}$	Chain Matrix

It is possible to transform the chain matrix coefficients in admittance coefficients [11]. Those transformations are:

$$\begin{bmatrix} t_{11} & t_{12} \\ t_{21} & t_{22} \end{bmatrix} = \begin{bmatrix} -\frac{y_{22}}{y_{21}} & -\frac{1}{y_{21}} \\ -\frac{|Y|}{y_{21}} & -\frac{y_{11}}{y_{21}} \end{bmatrix} \tag{A.1}$$

ANNEX II. Source transformations

In this annex, some source transformations suitable for noise analysis are presented.

In Figure A-2, the Bakesley transformation, also known as voltage source shifting is presented. The polarity of the new voltage sources must be respected as represented, to ensure the network equations are not changed.

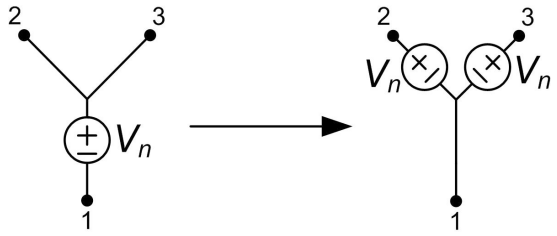


Figure A-2. Voltage source shifting.

In Figure A-3, the splitting of a current source is represented. A current source can be splitted into two current sources having the same value, and being connected to one of the terminals of the original current source. The polarity must be as indicated.

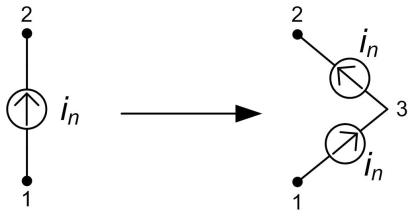


Figure A-3. Splitting of a noise source.

In Figure A-4, the Norton-Thevenin sources equivalence is presented. The voltage source v_n in series with resistance R has a Norton equivalent that is a current source $i_n=v_n / R$ in parallel with resistance R and vice-versa.

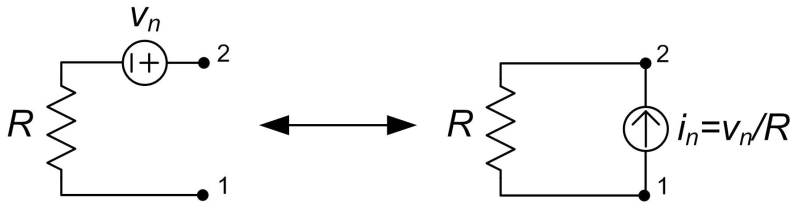


Figure A-4. Norton-Thevenin sources equivalence.

In a 2-port, it is possible to transfer a source connected to one of the ports to the other port. Consider the 2-port of Figure A-5-A characterized by a chain matrix T and having a voltage source and a current source at the output. The resulting sources at the input have the values represented in Figure A-5-B.

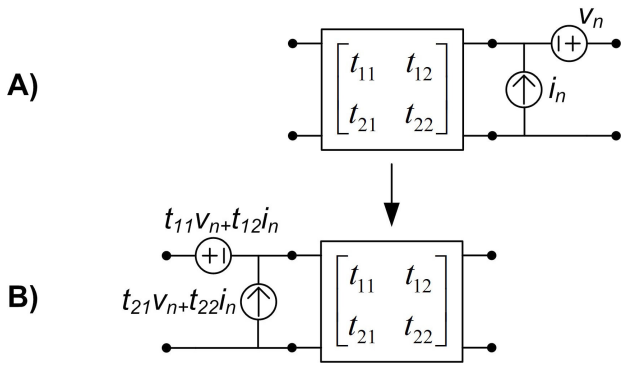


Figure A-5. 2-port transformation of noise sources.

ANNEX III. Y-matrix coefficients calculation

The results presented in section 4.3, were obtained through the following calculations.

Amplifying Block

In Figure A-6, the small-signal circuit of the amplifying block is shown.

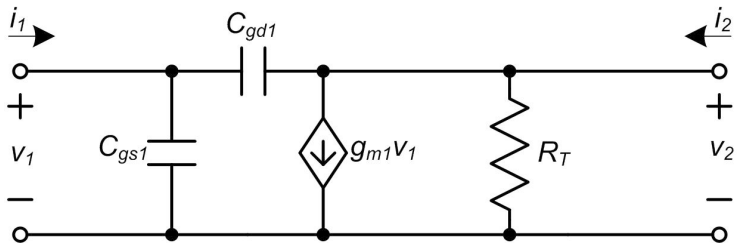


Figure A-6. Amplifying block.

For v_1 equal to zero, the circuit simplifies to:

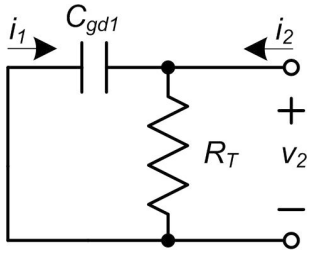


Figure A-7. Amplifying block: v_1 = 0V.

from which follows:

$$\begin{cases} i_2 = \left(\frac{1}{R_T} + sC_{gd1}\right)v_2 \\ i_1 = -sC_{gd1}v_2 \end{cases} \Leftrightarrow \begin{cases} y_{22A} = \frac{i_2}{v_2} = \frac{1}{R_T} + sC_{gd1} \\ y_{12A} = \frac{i_1}{v_2} = -sC_{gd1} \end{cases} \quad \text{(A.2)}$$

For v_2 equal to zero, the circuit simplifies to:

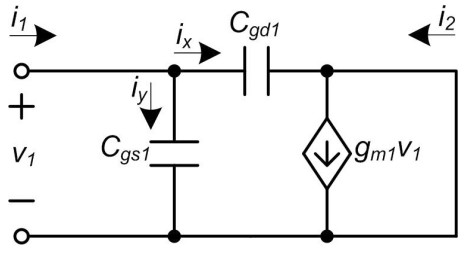


Figure A-8. Amplifying block: v_2 = 0V.

from which follows:

$$\begin{cases} i_1 = i_x + i_y \\ i_x + i_2 = g_{m1} v_1 \end{cases} \Leftrightarrow \begin{cases} y_{11A} = s\left(C_{gs1} + C_{gd1}\right) \\ y_{21A} = \dfrac{i_2}{v_1} = g_{m1} - sC_{gd1} \end{cases} \tag{A.3}$$

Feedback Block

In Figure A-9, the small-signal circuit of the feedback block is shown.

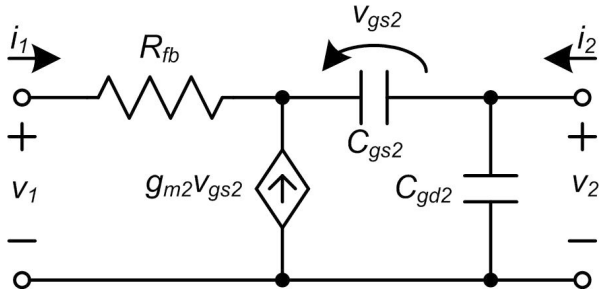


Figure A-9. Feedback block.

For v_1 equal to zero, the circuit simplifies to:

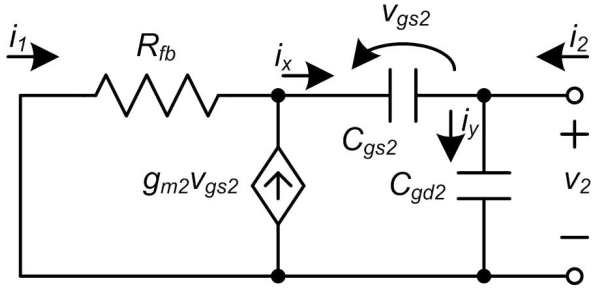


Figure A-10. Feedback block: v_1 = 0V.

from which follows:

$$\begin{cases} i_2 + i_x = i_y \\ i_1 + g_{m2} v_{gs2} = i_x \\ v_{gs2} = -\dfrac{1}{sC_{gs2}} i_x \\ v_2 = v_{gs2} - R_{fb} i_1 \end{cases} \Leftrightarrow \begin{cases} y_{12\beta} = \dfrac{i_1}{v_2} = -\dfrac{g_{m2} + sC_{gs2}}{1 + g_{m2}R_{fb} + sC_{gs2}R_{fb}} \\ y_{22\beta} = \dfrac{i_2}{v_2} = \dfrac{s\left(C_{gd2} + C_{gs2} + g_{m2}C_{gd2}R_{fb} + sC_{gd2}C_{gs2}R_{fb}\right)}{1 + g_{m2}R_{fb} + sC_{gs2}R_{fb}} \end{cases} \tag{A.4}$$

For v_2 equal to zero, the circuit simplifies to:

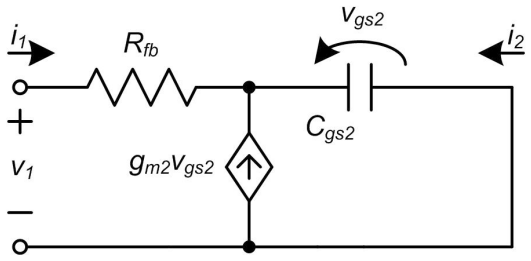


Figure A-11. Feedback block: v_2 = 0V.

from which follows:

$$\begin{cases} i_1 + i_2 + g_{m2} v_{gs2} = 0 \\ v_1 = R_{fb} i_1 - v_{gs2} \\ v_{gs2} = \dfrac{1}{sC_{gs2}} i_2 \end{cases} \Leftrightarrow \begin{cases} y_{11\beta} = \dfrac{i_1}{v_1} = \dfrac{g_{m2} + sC_{gs2}}{1 + g_{m2}R_{fb} + sC_{gs2}R_{fb}} \\ y_{21\beta} = \dfrac{i_2}{v_1} = -\dfrac{sC_{gs2}}{1 + g_{m2}R_{fb} + sC_{gs2}R_{fb}} \end{cases} \quad \text{(A.5)}$$

ANNEX IV. Osmix: Oscillator/Mixer block

The LNA block will be connected to an Osmix, a crossed-coupled relaxation oscillator with incorporated mixing function. Its schematic can be seen in Figure A-12.

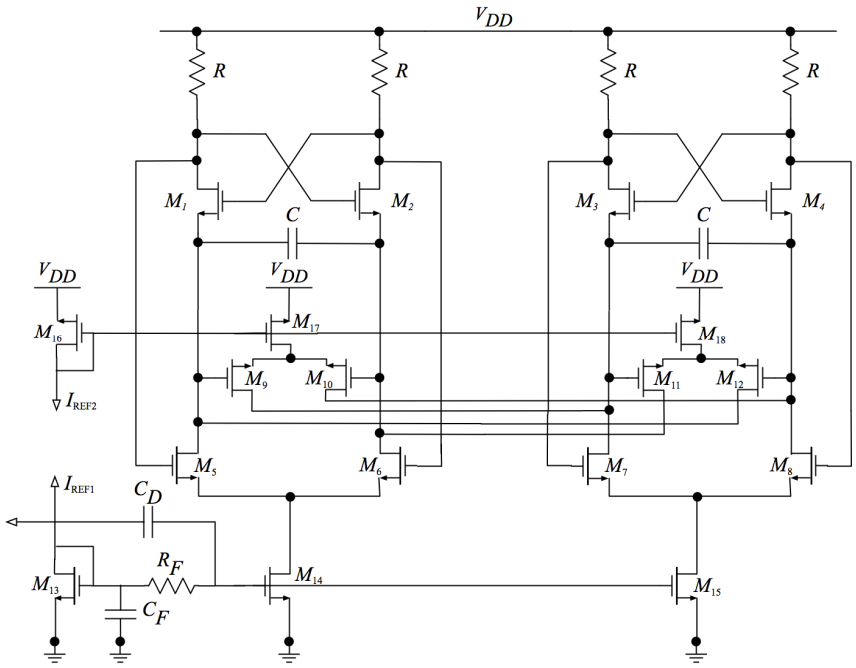


Figure A-12. Osmix block.

In Figure A-13, the input of the Osmix is evidenced and the LNA will be connected to the RF Input Pin. The input impedance of the Osmix might impact the performance of the LNA. Ideally, the input impedance of the Osmix should be infinite, so that its impact in the LNA can be inexistent. In reality, the input impedance of the Osmix should be at least one order of magnitude higher than the output impedance of the LNA.

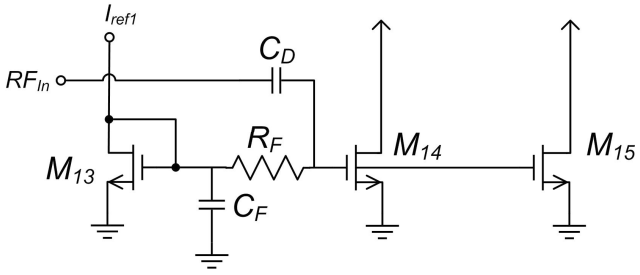


Figure A-13. Input of the Osmix block.

To get an estimative of the input impedance of the Osmix, the small-signal circuit of Figure A-13 was obtained and can be seen in Figure A-14.

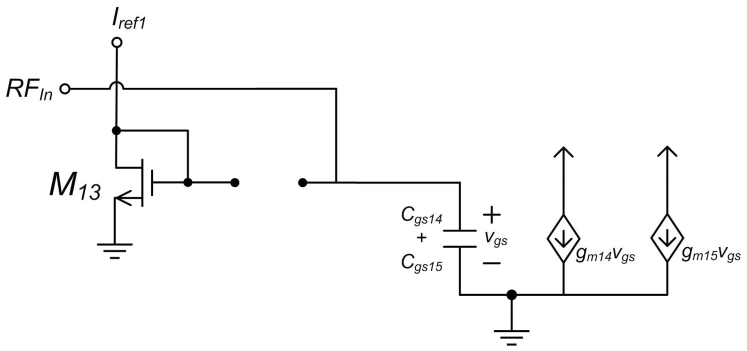


Figure A-14. Small-signal circuit of the input of the OSMIX block.

As can be seen from the figure, the low-pass filter acts as a open circuit, disconnecting the gate of the transistors from the DC current, and the decoupling capacitor can be seen as a short-circuit. Therefore, the input of the Osmix is simply the parallel of the C_{gs} of the transistors. Experimentally, it was seen that the value of the transistors are about 35fF each, so at 2.4 GHz, the input impedance is approximately 1kΩ.

$$Z_{in} = \left| \frac{1}{2\pi f \left(C_{gs1} + C_{gs2} \right)} \right| = \left| \frac{1}{2\pi \left(2.4 \times 10^{9} \right) \left(35 \times 10^{-15} + 35 \times 10^{-15} \right)} \right| \approx 1\text{k}\Omega$$

ANNEX V. Noise equations demonstration

LNA_A noise equation demonstration

The main noise contributions for LNA_A are from the resistances and from transistors M_1 and M_3. The other noise sources can be considered negligible when compared with the main ones.

In Figure A-15 the small signal circuit of LNA_A with the relevant noise sources is shown.

- $v_{n,Rfb}$ is the thermal noise source related to R_{fb};
- $v_{n,RT}$ is the thermal noise source related to R_T;
- $v_{n,Rg1}$ and $i_{n,d1}$ are, respectively, the noise source associated with the gate resistance and the thermal noise generated by the channel admittance of the transistor M_1;
- $v_{n,Rg3}$ and $i_{n,d3}$ are, respectively, the noise source associated with the gate resistance and the thermal noise generated by the channel admittance of the transistor M_3.

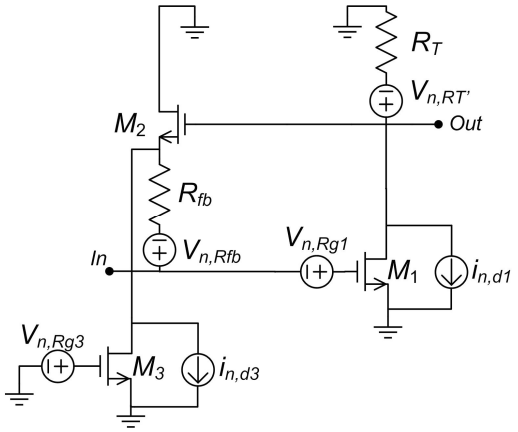
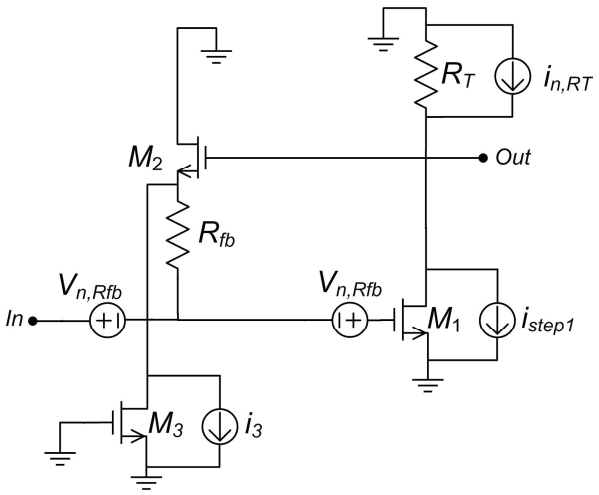


Figure A-15. LNA_A and its relevant noise sources.

To achieve the analytical expression of the input noise power spectral density, some noise source transformations need to be performed. Those transformations are detailed below.



Operations performed:

- Norton-Thevenin source equivalence in R_T;
- Voltage-source shifting for $v_{n,Rfb}$;
- Voltage-current transformation in M_1 and M_3.

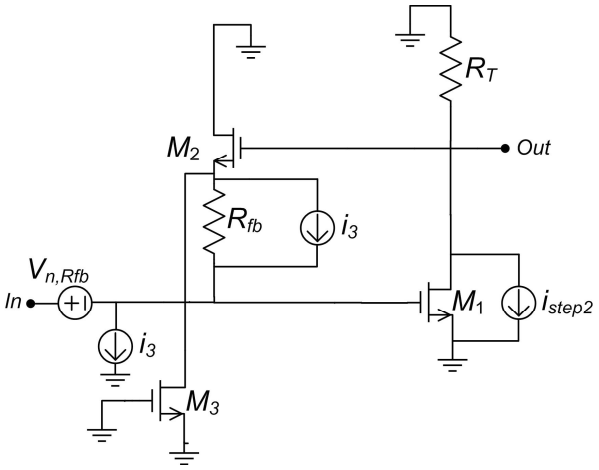
New variables:

$$i_{n,R_T} = \frac{v_{n,R_T}}{R_T} \tag{A.6}$$

$$i_{STEP1} = i_{n,d_1} + g_{m1} v_{n,R_{g1}} \tag{A.7}$$

$$i_3 = i_{n,d_3} + g_{m3} v_{n,R_{g3}} \tag{A.8}$$

Step 1 of the noise source transformations for LNA_A.



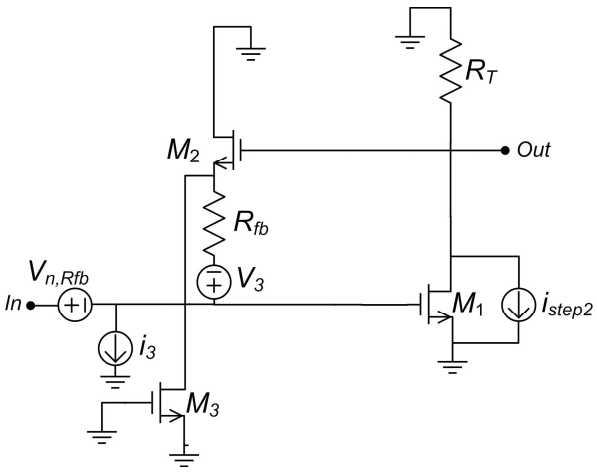
Operations performed:

- Voltage-current transformation in M_1;
- Splitting of current source i_3;
- Inclusion of $i_{n,RT}$ in i_{STEP2}.

New variables:

$$i_{STEP2} = i_{STEP1} + g_{m1} v_{n,R_{fb}} - i_{n,R_T} = i_{n,d_1} + g_{m1}\left(v_{n,R_{fb}} + v_{n,R_{g1}}\right) - \frac{v_{n,R_T}}{R_T} \tag{A.9}$$

Step 2 of the noise source transformations for LNA_A.



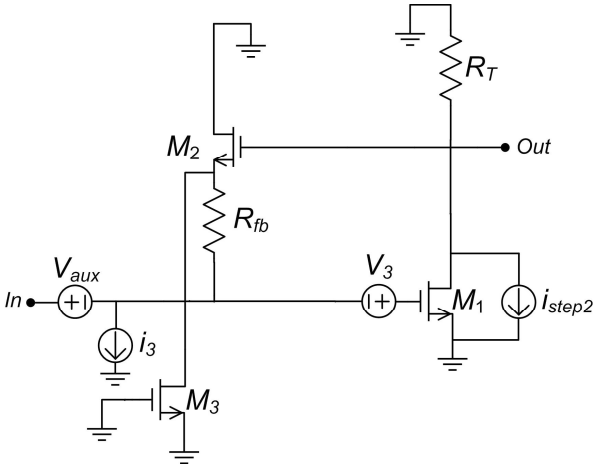
Operations performed:

- Norton-Thevenin source equivalence in R_{fb}.

New variables:

$$v_3 = R_{fb} i_3 = R_{fb}\left(i_{n,d_3} + g_{m3} v_{n,R_{g3}}\right) \tag{A.10}$$

Step 3 of the noise source transformations for LNA_A.



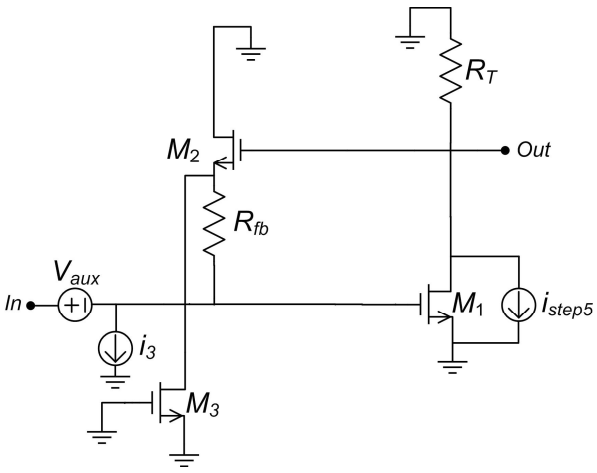
Operations performed:

- Voltage-source shifting for v_3.

New variables:

$$v_{aux} = v_{n,R_{fb}} + v_3 = v_{n,R_{fb}} + R_{fb}\left(i_{n,d_3} + g_{m3} v_{n,R_{g3}}\right) \tag{A.11}$$

Step 4 of the noise source transformations for LNA_A.



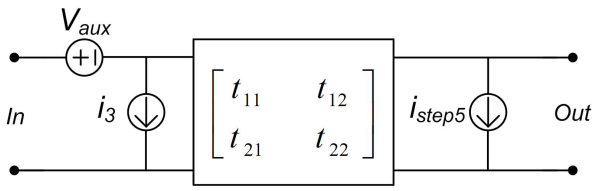
Operations performed:

- Voltage-current transformation in M_1 of v_3.

New variables:

$$i_{STEP\,5} = i_{STEP\,2} + g_{m1} v_3 =$$
$$= i_{n,d1} + g_{m1}\left(v_{n,R_{g1}} + v_{n,R_{fb}} + v_3\right) - \frac{v_{n,R_T}}{R_T} \qquad \text{(A.12)}$$
$$= i_{n,d1} + g_{m1}\left[v_{n,R_{g1}} + v_{n,R_{fb}} + R_{fb}\left(i_{n,d_3} + g_{m3} v_{n,R_{g3}}\right)\right] - \frac{v_{n,R_T}}{R_T}$$

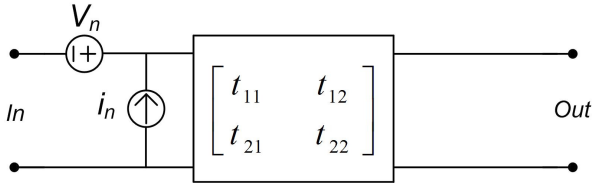
Step 5 of the noise source transformations for LNA_A.



Operations performed:

- See the circuit as a chain matrix.

Step 6 of the noise source transformations for LNA_A.



Operations performed:

- 2-port transformation of noise sources.

$$t_{12} = -\frac{1}{Y_{21}} \qquad t_{22} = -\frac{Y_{11}}{Y_{21}}$$

New variables:

$$\begin{cases} v_n = -v_{aux} - t_{12} i_{STEP\,5} \\ i_n = -i_3 - t_{22} i_{STEP\,5} \end{cases} \qquad \text{(A.13)}$$

Step 7 of the noise source transformations for LNA_A.

The total input noise is expressed as:

$$\begin{aligned} & v_T = v_n + R_S i_n = -v_{aux} - t_{12} i_{STEP5} - R_S i_3 - R_S t_{22} i_{STEP5} \\ & \Leftrightarrow v_T = -(v_{aux} + R_S i_3) - (t_{12} + R_S t_{22}) i_{STEP5} \Leftrightarrow v_T = -(v_{aux} + R_S i_3) - \alpha i_{STEP5} \\ & \Leftrightarrow v_T = -v_{n,R_{fb}}(1 + g_{m1}\alpha) + v_{n,R_T}\left(\frac{\alpha}{R_T}\right) - i_{n,d1}(\alpha) - v_{n,R_{g1}}(g_{m1}\alpha) \\ & -i_{n,d3}(R_{fb} + R_S + g_{m1}R_{fb}\alpha) - v_{n,R_{g3}}(g_{m3}R_{fb} + g_{m3}R_S + g_{m1}g_{m3}R_{fb}\alpha) \end{aligned} \quad \text{(A.14)}$$

with $\alpha = t_{12} + R_S t_{22}$.

Finally, the input noise power spectral density, using the Wiener-Khintchine theorem is:

$$\begin{aligned} & N_i(f) = N_{v_{n,R_{fb}}}\left|1 + g_{m1}\alpha\right|^2 + N_{v_{n,R_T}}\left|\frac{\alpha}{R_T}\right|^2 + N_{i_{n,d1}}\left|\alpha\right|^2 + N_{v_{n,R_{g1}}}\left|g_{m1}\alpha\right|^2 \\ & + N_{i_{n,d3}}\left|R_{fb} + R_S + g_{m1}R_{fb}\alpha\right|^2 + N_{v_{n,R_{g3}}}\left|g_{m3}R_{fb} + g_{m3}R_S + g_{m1}g_{m3}R_{fb}\alpha\right|^2 \end{aligned} \quad \text{(A.15)}$$

where

$$\begin{aligned} & N_{v_{n,R_{fb}}} = 4k_B T R_{fb} \quad N_{i_{n,d1}} = 4k_B T \gamma g_{m1} \quad N_{v_{n,R_{g1}}} = 4k_B T R_{g1} \\ & N_{v_{n,R_T}} = 4k_B T R_T \quad N_{i_{n,d3}} = 4k_B T \gamma g_{m3} \quad N_{v_{n,R_{g3}}} = 4k_B T R_{g3} \end{aligned} \quad \text{(A.16)}$$

with γ=2/3 and T=300.15K (27ºC). R_{g1} and R_{g3}, were estimated as 1Ω and 10Ω, respectively, after analyzing the spice models of the transistor to be used and some preliminary simulations.

LNA_B noise equation demonstration

The main noise contributions for LNA_B are from the resistances and from transistors M_1 and M_3. The other noise sources can be considered negligible when compared with the main ones.

In Figure A-16, the small signal circuit of LNA_B with the relevant noise sources is shown.

- $v_{n,Rfb}$ is the thermal noise source related to R_{fb};
- $v_{n,RT}$ is the thermal noise source related to R_T;
- $v_{n,Rg1}$ and $i_{n,d1}$ are, respectively, the noise source associated with the gate resistance and the thermal noise generated by the channel admittance of the transistor M_1;
- $v_{n,Rg3}$ and $i_{n,d3}$ are, respectively, the noise source associated with the gate resistance and the

thermal noise generated by the channel admittance of the transistor M_3.

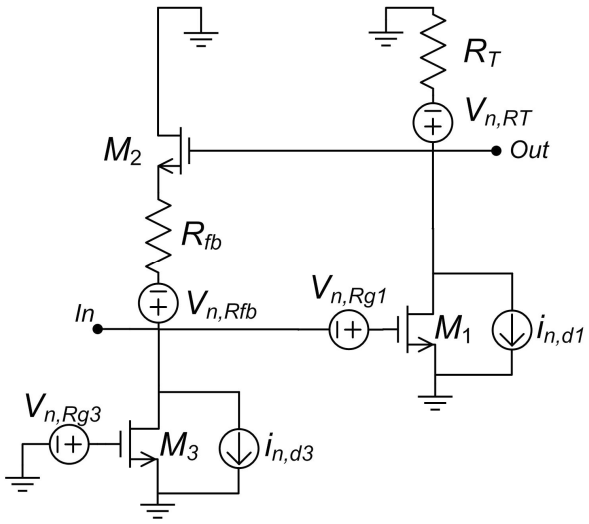
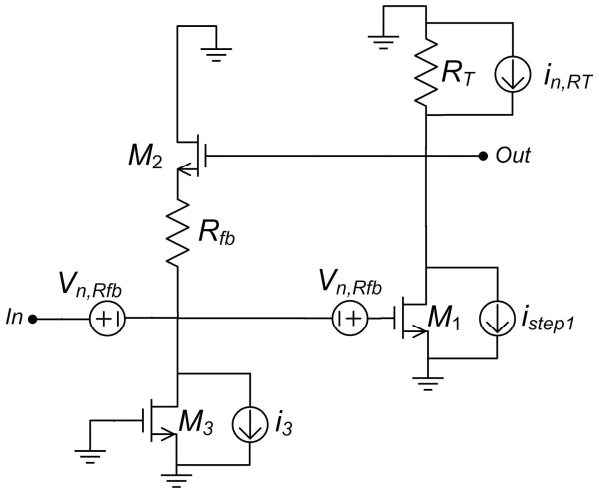


Figure A-16. LNA_B and its relevant noise sources.

To achieve the analytical expression of the input noise power spectral density, some noise source transformations need to be performed. Those transformations are detailed below.



Operations performed:

- Norton-Thevenin source equivalence in R_T;
- Voltage-source shifting for $v_{n,Rfb}$;
- Voltage-current transformation in M_1 and M_3.

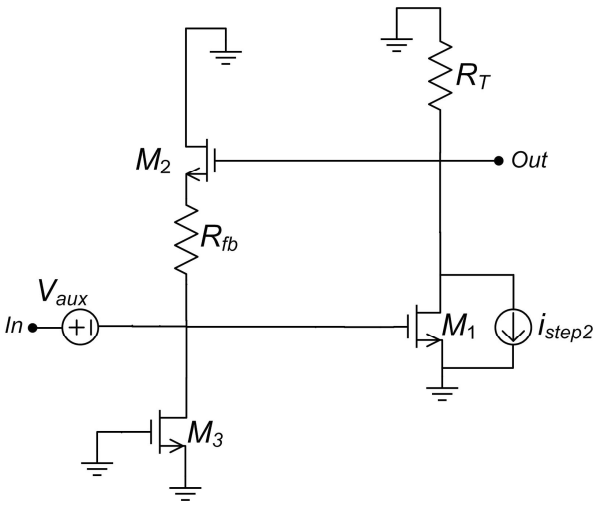
New variables:

$$i_{n,R_T} = \frac{v_{n,R_T}}{R_T} \tag{A.17}$$

$$i_{STEP1} = i_{n,d_1} + g_{m1} v_{n,R_{g1}} \tag{A.18}$$

$$i_{STEP1} = i_{n,d_3} + g_{m1} v_{n,R_{g3}} \tag{A.19}$$

Step 1 of the noise source transformations for LNA_B.



Operations performed:

- Voltage-current transformation of $v_{n,Rfb}$ into i_{STEP2};
- Norton-Thevenin source equivalence in M_3 with R_S;
- Inclusion of $i_{n,RT}$ into i_{STEP2};
- Voltage-shifting of $v_{n,Rfb}$ into v_{aux}.

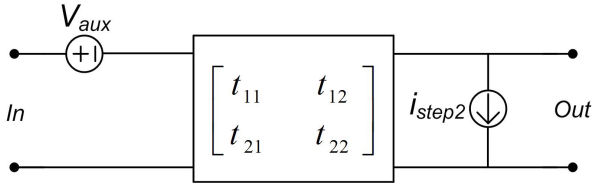
(R_S is the source resistance)

New variables:

$$i_{STEP\,2} = i_{STEP1} + g_{m1} v_{n,R_{fb}} - i_{n,R_T} = i_{n,d_1} + g_{m1}\left(v_{n,R_{fb}} + v_{n,R_{g1}}\right) - \frac{v_{n,R_T}}{R_T} \qquad \text{(A.20)}$$

$$v_{aux} = v_{n,R_{fb}} + R_S i_{n,d_3} + R_S g_{m3} v_{n,R_{g3}} \qquad \text{(A.21)}$$

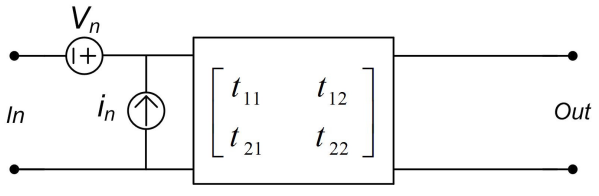
Step 2 of the noise source transformations for LNA_A.



Operations performed:

- See the circuit as a chain matrix.

Step 3 of the noise source transformations for LNA_A.



Operations performed:

- 2-port transformation of noise sources.

$$t_{12} = -\frac{1}{Y_{21}} \qquad t_{22} = -\frac{Y_{11}}{Y_{21}}$$

New variables:

$$\begin{cases} v_n = -v_{aux} - t_{12} i_{STEP\,2} \\ i_n = -t_{22} i_{STEP\,2} \end{cases} \quad \text{(A.22)}$$

Step 4 of the noise source transformations for LNA_A.

The total input noise is expressed in (6.14), where R_S is the source resistance.

$$\begin{aligned} & v_T = v_n + R_S i_n = -v_{aux} - t_{12} i_{STEP\,2} - R_S t_{22} i_{STEP\,2} \\ & \Leftrightarrow v_T = -v_{aux} - (t_{12} + R_S t_{22}) i_{STEP\,2} \Leftrightarrow v_T = -v_{aux} - \alpha i_{STEP\,2} \\ & \Leftrightarrow v_T = -v_{n,R_{fb}} (1 + g_{m1}\alpha) + v_{n,R_T} \left(\frac{\alpha}{R_T} \right) - i_{n,d1}(\alpha) - v_{n,R_{g1}} (g_{m1}\alpha) - i_{n,d3}(R_S) - v_{n,R_{g3}} (g_{m3} R_S) \end{aligned} \quad \text{(A.23)}$$

with $\alpha = t_{12} + R_S t_{22}$.

Finally, the input noise power spectral density, using the Wiener-Khintchine theorem, is:

$$N_i(f) = N_{v_{n,R_{fb}}} \left| 1 + g_{m1}\alpha \right|^2 + N_{v_{n,R_T}} \left| \frac{\alpha}{R_T} \right|^2 + N_{i_{n,d1}} \left| \alpha \right|^2 + N_{v_{n,R_{g1}}} \left| g_{m1}\alpha \right|^2 + N_{i_{n,d3}} \left| R_S \right|^2 + N_{v_{n,R_{g3}}} \left| g_{m3} R_S \right| \quad \text{(A.24)}$$

where

$$\begin{aligned} & N_{v_{n,Rfb}} = 4 k_B T R_{fb} \quad N_{i_{n,d1}} = 4 k_B T \gamma g_{m1} \quad N_{v_{n,R_{g1}}} = 4 k_B T R_{g1} \\ & N_{v_{n,RT}} = 4 k_B T R_T \quad N_{i_{n,d3}} = 4 k_B T \gamma g_{m3} \quad N_{v_{n,R_{g3}}} = 4 k_B T R_{g3} \end{aligned} \quad \text{(A.25)}$$

with γ=2/3 and T=300.15K (27ºC). R_{g1} and R_{g3}, were estimated as 1Ω and 10Ω, respectively, after analyzing the spice models of the transistor to be used and some preliminary simulations.

ANNEX VI. *Mathematica* source code used for chapter 4 simulations

To simulate for LNA_B uncomment the LNA_B circuit dimensioning values and comment the LNA_A circuit dimensioning values.

```
Clear["`*"]

y11a = s*(Cgs1 + Cgd1);
y12a = - s*Cgd1;
y21a = gm1 - s*Cgd1;
y22a = (1/Rt + s*Cgd1);

y11b = 1/(Rfb + 1/(s*Cgs2*(gm2/(s*Cgs2) + 1)));
y12b = -1/((1/(1 + (gm2/(s*Cgs2))))*(1/(s*Cgs2)) + Rfb);
y21b = -1/((gm2/(s*Cgs2) + 1)*Rfb + 1/(s*Cgs2));
y22b = s*Cgd2*(1 + ((1/((1/(1 + (gm2/(s*Cgs2))))*(1/(s*Cgs2)) + Rfb))*(1/(s*
           Cgd2))*(1/(1 + (gm2/(s*Cgs2))))));

Print["y11b"];
y11b = FullSimplify[y11b]
Print["y12b"];
y12b = FullSimplify[y12b]
Print["y21b"];
y21b = FullSimplify[y21b]
Print["y22b"];
y22b = FullSimplify[y22b]


Y11 = s*(Cgs1 + Cgd1) + 1/(Rfb + 1/(s*Cgs2*(gm2/(s*Cgs2) + 1)));
Y12 = - s*Cgd1 - 1/((1/(1 + (gm2/(s*Cgs2))))*(1/(s*Cgs2)) + Rfb);
Y21 =  gm1 - s*Cgd1 - 1/((gm2/(s*Cgs2) + 1)*Rfb + 1/(s*Cgs2));
Y22 = (1/Rt + s*Cgd1) +
   s*Cgd2*(1 + ((1/((1/(1 + (gm2/(s*Cgs2))))*(1/(s*Cgs2)) + Rfb))*(1/(s*
            Cgd2))*(1/(1 + (gm2/(s*Cgs2))))));


Print["Y11"];
Y11 = FullSimplify[Y11]
Print["y12"];
Y12 = FullSimplify[Y12]
Print["y21"];
Y21 = FullSimplify[Y21]
Print["y22"];
Y22 = FullSimplify[Y22]

Print["Av = -y21/(y22+Gl), com Gl=s*Cl"]

Av = -(gm1 - s*Cgd1 -
      1/((gm2/(s*Cgs2) + 1)*Rfb + 1/(s*Cgs2)))/(((1/Rt + s*Cgd1) +
       s*Cgd2*(1 + ((1/((1/(1 + (gm2/(s*Cgs2))))*(1/(s*Cgs2)) + Rfb))*(1/(s*
                 Cgd2))*(1/(1 + (gm2/(s*Cgs2)))))) + s*Cl);
Av = FullSimplify[Av]

Print["Avlim =  Limit[Av,Cgd1® 0, Cgd2® 0, Cgs1® 0, Cgs2® 0, Cl® 0]"];
Avlim = Limit[Av, Cgd1 -> 0];
Avlim = Limit[Avlim, Cgd2 -> 0];
Avlim = Limit[Avlim, Cgs1 -> 0];
Avlim = Limit[Avlim, Cgs2 -> 0];
Avlim = Limit[Avlim, Cl -> 0];
Avlim = FullSimplify[Avlim]

Print["Zin = [y11-(y12*y21)/(y22+Gl)]^-1, com Gl=s*Cl"];

Zin = ((s*(Cgs1 + Cgd1) +
       1/(Rfb + 1/(s*Cgs2*(gm2/(s*Cgs2) + 1)))) - ((- s*Cgd1 -
          1/((1/(1 + (gm2/(s*Cgs2))))*(1/(s*Cgs2)) + Rfb))*(gm1 - s*Cgd1 -
          1/((gm2/(s*Cgs2) + 1)*Rfb + 1/(s*Cgs2))))/(((1/Rt + s*Cgd1) +
          s*
           Cgd2*(1 + ((1/((1/(1 + (gm2/(s*Cgs2))))*(1/(s*Cgs2)) + Rfb))*(1/(s*
                     Cgd2))*(1/(1 + (gm2/(s*Cgs2)))))) + s*Cl))^-1;
Zin = FullSimplify[Zin]

Print["Zinlim =  Limit[Zin,Cgd1® 0, Cgd2® 0, Cgs1® 0, Cgs2® 0, Cl® 0]"];
Zinlim = Limit[Zin, Cgd1 -> 0];
Zinlim = Limit[Zinlim, Cgd2 -> 0];
Zinlim = Limit[Zinlim, Cgs1 -> 0];
Zinlim = Limit[Zinlim, Cgs2 -> 0];
Zinlim = Limit[Zinlim, Cl -> 0];
```

```
Zinlim = FullSimplify[Zinlim]

(*Print["A carregado: A'=-(Y21)/(Y22+1/Rg)(Y11+sCl)"]*)

A = -(Y21)/((Y22 + 1/Rg)*(Y11 + s*Cl));

(*Print["B ideal: Y12"]*)
Bideal = Y12;

(*Noise power spectral density equations*)
t12 = -1/Y21;
t22 = -Y11 / Y21;
a = t12 + Rs*t22;

Nvrfb = 4*Kb*T*Rfb;
Nind3 = 4*Kb*T*L*gm3;
Nvrg3 = 4*Kb*T*Rg3;
Nind1 = 4*Kb*T*L*gm1;
Nvrg1 = 4*Kb*T*Rg1;
Nvrt = 4*Kb*T*Rt;

(*Noise power spectral density LNA_A*)

NiLNA_A = Nvrfb*Abs[1 + a*gm1]^2 + Nind3*Abs[Rfb + Rs + gm1*Rfb*a]^2 +
   Nvrg3*Abs[gm3*Rfb + gm3*Rs + gm3*gm1*Rfb*a]^2 + Nind1*Abs[a]^2 +
   Nvrg1*Abs[a*gm1]^2 + Nvrt*Abs[a/Rt]^2;

NFLNA_A = Simplify[1 + NiLNA_A/(4*Kb*T*Rs)];

(*Noise power spectral density LNA_B*)

NiLNA_B = Nvrfb*Abs[1 + a*gm1]^2 + Nind3*Abs[Rs]^2 + Nvrg3*Abs[gm3*Rs]^2 +
   Nind1*Abs[a]^2 + Nvrg1*Abs[a*gm1]^2 + Nvrt*Abs[a/Rt]^2;
NFLNA_B = Simplify[1 + NiLNA_B/(4*Kb*T*Rs)];


(*LNA_A Circuit Dimensioning*)
s = I*2*3.14*f;
Cgs1 = 40*10^-15;
Cgs2 = 40*10^-15;
Cgd1 = 20*10^-15;
Cgd2 = 20*10^-15;
(*Cl = 0;*)
Rfb = 500;
Rt = 100;
Rg = 50;
Rs = 50;
gm1 = 100*10^-3;
gm2 = 20*10^-3;

Kb = 1.38*10^-23;
L = 2/3;
T = 300.15;
Rg1 = 10.850;
Rg3 = 10.850;
gm3 =  5*10^-3;

(*LNA_B Circuit Dimensioning*)
(*
s=I*2*3.14*f;
Cgs1=40*10^-15;
Cgs2=40*10^-15;
Cgd1=20*10^-15;
Cgd2=20*10^-15;
(*Cl = 0;*)
Rfb=367;
Rt=366;
Rg = 50;
Rs = 50;
gm1= 27*10^-3;
gm2=5.5*10^-3;

Kb = 1.38*10^-23;
L = 2/3;
T = 300.15;
Rg1 = 10.850;
Rg3 = 10.850;
gm3 =  5*10^-3;
*)

(*
f=3.2*10^9;
Cl=0;

20*Log[10,Abs[Av]] // N
20*Log[10,Abs[((Zin-50)/(Zin+50))]] // N
20*Log[10,Abs[(A*Bideal)]]
```

```
phase_rad = Abs[-Pi-Arg[(A*Bideal)]]
phase_deg = 2.705*180/Pi // N
10*Log[10,Abs[NFLNA_B]] // N
*)


(* Gr·ficos do ganho *)
Print["Gr·fico do ganho (Cl== 0)"];
LogLinearPlot[{20*Log[10, Abs[Av /. {Cl -> 0}]]}, {f, 100*10^6, 10*10^9},
 Frame -> True,
 FrameLabel -> {Frequency[Hz], Gain[dB]} ,
 PlotStyle -> {RGBColor[0, 0, 0], Thickness[0.005]},
 BaseStyle -> {FontWeight -> "Bold", FontSize -> 25, FontFamily -> "Arial",
   FontColor -> Black},
 ImageSize -> {1000, 600}]

Print["Gr·fico do ganho: Cl=0F (Black), Cl=50fF (Red), Cl=100fF (Green), \
Cl=500fF (Blue), Cl=1pF (Orange)"];
LogLinearPlot[{20*Log[10, Abs[Av /. {Cl -> 0}]],
  20*Log[10, Abs[Av /. {Cl -> 50*10^-15}]],
  20*Log[10, Abs[Av /. {Cl -> 100*10^-15}]],
  20*Log[10, Abs[Av /. {Cl -> 500*10^-15}]],
  20*Log[10, Abs[Av /. {Cl -> 1000*10^-15}]]}, {f, 100*10^6, 10*10^9},
 Frame -> True,
 FrameLabel -> {Frequency[Hz], Gain[dB]},
 PlotStyle -> {{Black, Thickness[0.005]}, {RGBColor[1, 0, 0],
    Thickness[0.005]}, {RGBColor[0, 1, 0],
    Thickness[0.005]}, {RGBColor[0, 0, 1],
    Thickness[0.005]}, {RGBColor[1, 0.65, 0], Thickness[0.005]}},
 BaseStyle -> {FontWeight -> "Bold", FontSize -> 25, FontFamily -> "Arial",
   FontColor -> Black},
 ImageSize -> {1000, 600}]

(* Gr·ficos de S11 *)
Print["Gr·fico de S11: Cl== 0"];
LogLinearPlot[{20*Log[10, Abs[((Zin - 50)/(Zin + 50)) /. {Cl -> 0}]]}, {f,
  100*10^6, 10*10^9},
 Frame -> True,
  FrameLabel -> {Frequency[Hz], S11[dB]},
 PlotStyle -> {RGBColor[0, 0, 0], Thickness[0.005]},
 BaseStyle -> {FontWeight -> "Bold", FontSize -> 25, FontFamily -> "Arial",
   FontColor -> Black},
 ImageSize -> {1000, 600}]

Print["Gr·fico de S11: Cl=0F (Black), Cl=50fF (Red), Cl=100fF (Green), \
Cl=500fF (Blue), Cl=1pF (Orange)"];
LogLinearPlot[{20*Log[10, Abs[((Zin - 50)/(Zin + 50)) /. {Cl -> 0}]],
  20*Log[10, Abs[((Zin - 50)/(Zin + 50)) /. {Cl -> 50*10^-15}]],
  20*Log[10, Abs[((Zin - 50)/(Zin + 50)) /. {Cl -> 100*10^-15}]],
  20*Log[10, Abs[((Zin - 50)/(Zin + 50)) /. {Cl -> 500*10^-15}]],
  20*Log[10, Abs[((Zin - 50)/(Zin + 50)) /. {Cl -> 1000*10^-15}]]}, {f,
  100*10^6, 10*10^9},
 Frame -> True,
 FrameLabel -> {Frequency[Hz], S11[dB]},
 PlotStyle -> {{Black, Thickness[0.005]}, {RGBColor[1, 0, 0],
    Thickness[0.005]}, {RGBColor[0, 1, 0],
    Thickness[0.005]}, {RGBColor[0, 0, 1],
    Thickness[0.005]}, {RGBColor[1, 0.65, 0], Thickness[0.005]}},
 BaseStyle -> {FontWeight -> "Bold", FontSize -> 25, FontFamily -> "Arial",
   FontColor -> Black},
 ImageSize -> {1000, 600}]

(* Gr·ficos de noise figure LNA_A*)
Print["Gr·fico de abs(NFLNA_A): Cl== 0"];
LogLinearPlot[{10*Log[10, Abs[(NFLNA_A) /. {Cl -> 0}]]}, {f, 100*10^6, 10*10^9},
 Frame -> True,
 FrameLabel -> {Frequency[Hz], Noise Figure[dB]},
 PlotStyle -> {RGBColor[0, 0, 0], Thickness[0.005]},
 BaseStyle -> {FontWeight -> "Bold", FontSize -> 25, FontFamily -> "Arial",
   FontColor -> Black},
 ImageSize -> {1000, 600}]

(*
(* Gr·ficos de noise figure LNA_B*)
Print["Gr·fico de abs(NFLNA_A): Cl== \
0"];
LogLinearPlot[{10*Log[10,Abs[(NFLNA_B)/.{Cl->0}]]},{f,100*10^6,10*10^9},
Frame->True,
FrameLabel -> {Frequency[Hz], Noise Figure[dB]},
PlotStyle->{RGBColor[0,0,0],Thickness[0.005]},
BaseStyle->{FontWeight->"Bold",FontSize->25,FontFamily->"Arial",FontColor->\
Black},
ImageSize->{1000,600}]
*)

(* Gr·ficos de estabilidade *)
Print["Gr·fico de abs(A*B): Cl== 0"];
```

```
LogLinearPlot[{20*Log[10, Abs[(A*Bideal) /. {Cl -> 0}]]}, {f, 100*10^6,
  10*10^9},
 Frame -> True,
 FrameLabel -> {Frequency[Hz], magnitude AB[dB]},
 PlotStyle -> {RGBColor[0, 0, 0], Thickness[0.005]},
 BaseStyle -> {FontWeight -> "Bold", FontSize -> 25, FontFamily -> "Arial",
   FontColor -> Black},
 ImageSize -> {1000, 600}]
Print["Gr·fico de arg(A*B): Cl== 0"];
LogLinearPlot[{Arg[(A*Bideal) /. {Cl -> 0}]}, {f, 100*10^6, 10*10^9},
 Frame -> True,
 FrameLabel -> {Frequency[Hz], phase AB[rad]},
 PlotStyle -> {RGBColor[0, 0, 0], Thickness[0.005]},
 BaseStyle -> {FontWeight -> "Bold", FontSize -> 25, FontFamily -> "Arial",
   FontColor -> Black},
 ImageSize -> {1000, 600}]

Print["Gr·fico de abs(A*B): Cl=0F (Black), Cl=50fF (Red), Cl=100fF (Green), \
Cl=500fF (Blue), Cl=1pF (Orange)"];
LogLinearPlot[{20*Log[10, Abs[(A*Bideal) /. {Cl -> 0}]],
  20*Log[10, Abs[(A*Bideal) /. {Cl -> 50*10^-15}]],
  20*Log[10, Abs[(A*Bideal) /. {Cl -> 100*10^-15}]],
  20*Log[10, Abs[(A*Bideal) /. {Cl -> 500*10^-15}]],
  20*Log[10, Abs[(A*Bideal) /. {Cl -> 1000*10^-15}]]}, {f, 100*10^6,
  10*10^9},
 Frame -> True,
 FrameLabel -> {Frequency[Hz], magnitude AB[dB]},
 PlotStyle -> {{Black, Thickness[0.005]}, {RGBColor[1, 0, 0],
    Thickness[0.005]}, {RGBColor[0, 1, 0],
    Thickness[0.005]}, {RGBColor[0, 0, 1],
    Thickness[0.005]}, {RGBColor[1, 0.65, 0], Thickness[0.005]}},
 BaseStyle -> {FontWeight -> "Bold", FontSize -> 25, FontFamily -> "Arial",
   FontColor -> Black},
 ImageSize -> {1000, 600}]

Print["Gr·fico de arg(A*B): Cl=0F (Black), Cl=50fF (Red), Cl=100fF (Green), \
Cl=500fF (Blue), Cl=1pF (Orange)"];
LogLinearPlot[{Arg[(A*Bideal) /. {Cl -> 0}],
  Arg[(A*Bideal) /. {Cl -> 50*10^-15}], Arg[(A*Bideal) /. {Cl -> 100*10^-15}],
   Arg[(A*Bideal) /. {Cl -> 500*10^-15}],
  Arg[(A*Bideal) /. {Cl -> 1000*10^-15}]}, {f, 100*10^6, 10*10^9},
 Frame -> True,
 FrameLabel -> {Frequency[Hz], phase AB[rad]},
 PlotStyle -> {{Black, Thickness[0.005]}, {RGBColor[1, 0, 0],
    Thickness[0.005]}, {RGBColor[0, 1, 0],
    Thickness[0.005]}, {RGBColor[0, 0, 1],
    Thickness[0.005]}, {RGBColor[1, 0.65, 0], Thickness[0.005]}},
 BaseStyle -> {FontWeight -> "Bold", FontSize -> 25, FontFamily -> "Arial",
   FontColor -> Black},
 ImageSize -> {1000, 600}]
```

ANNEX VII. Gain, S_{11} and NF Plots of chapter 5

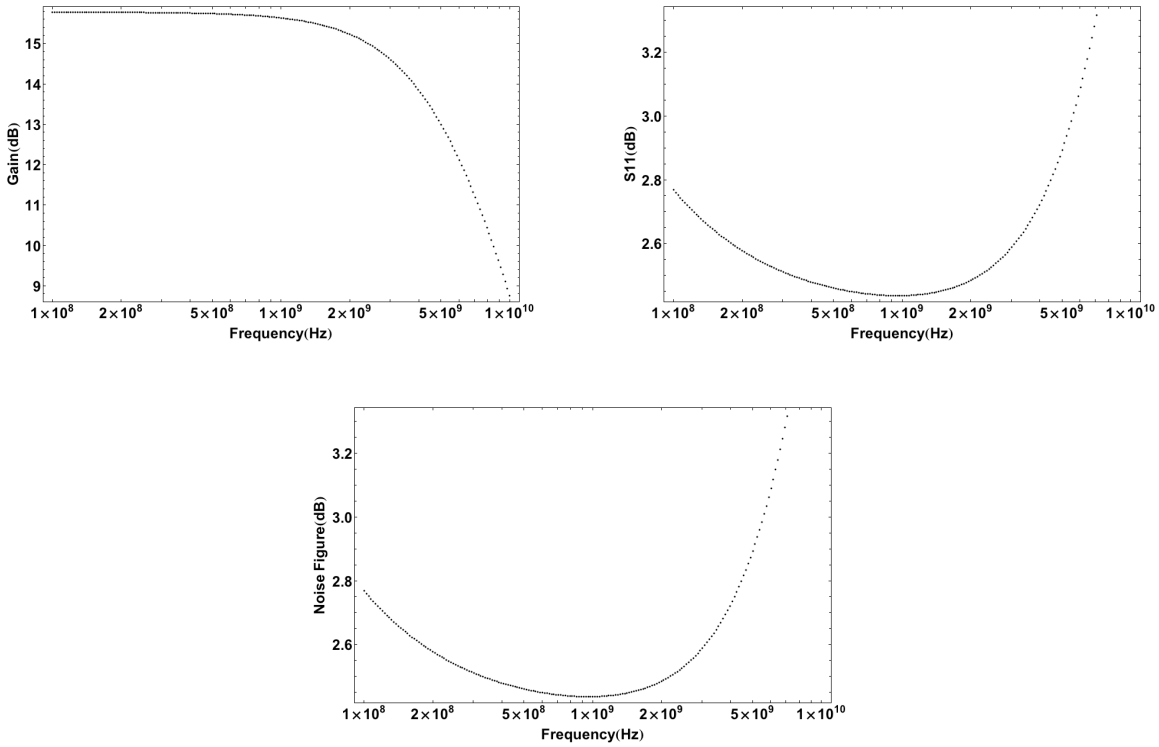


Figure A-17. Gain, S_{11} and NF plots of LNA_A.

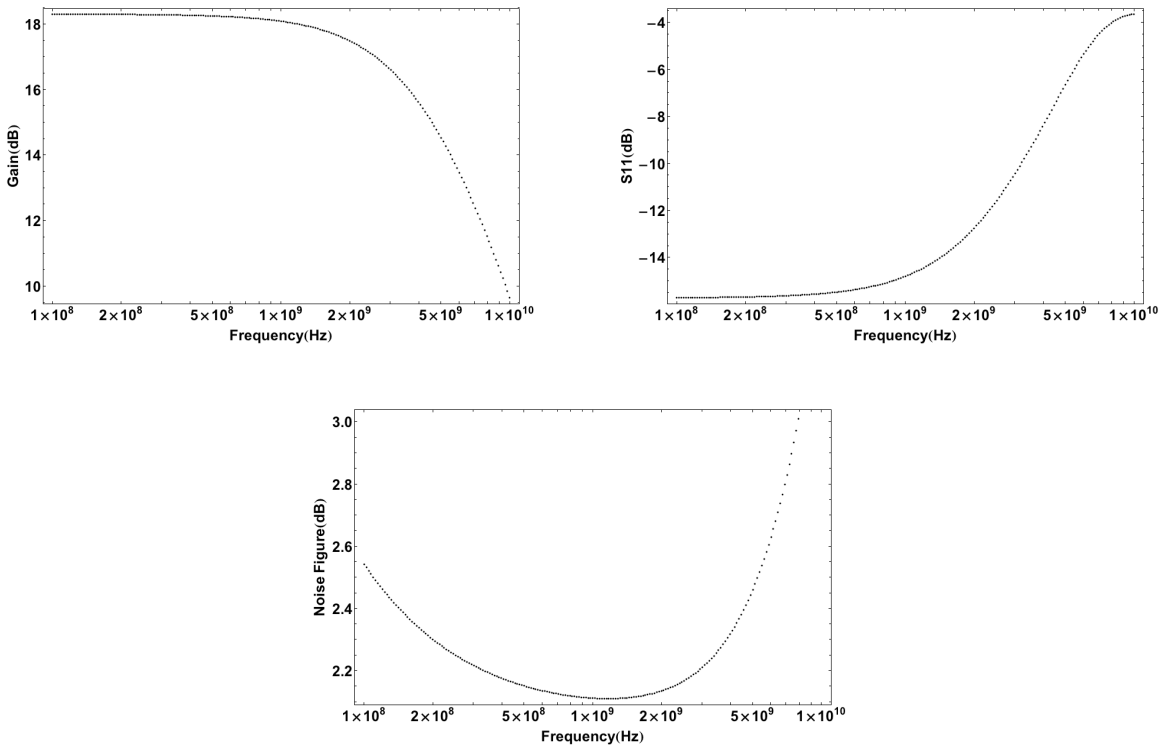


Figure A-18. Gain, S_{11} and NF plots of MOSFET only LNA_A.

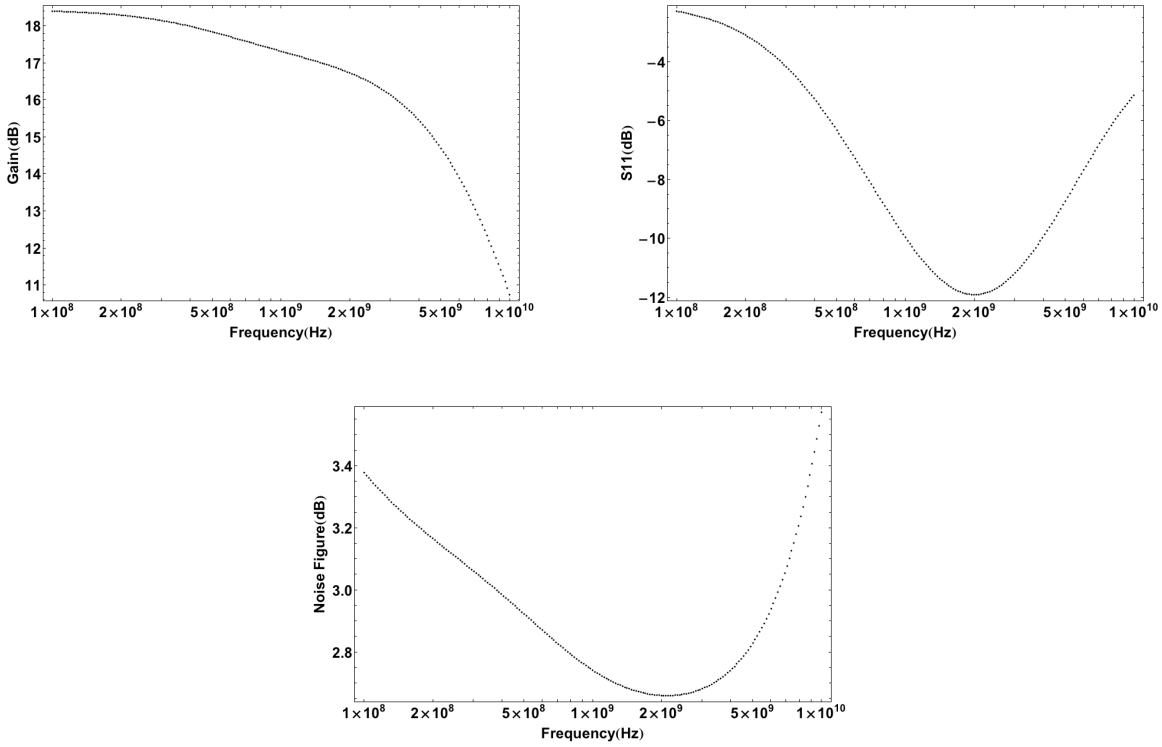


Figure A-19. Gain, S_{11} and NF plots of LNA_B.

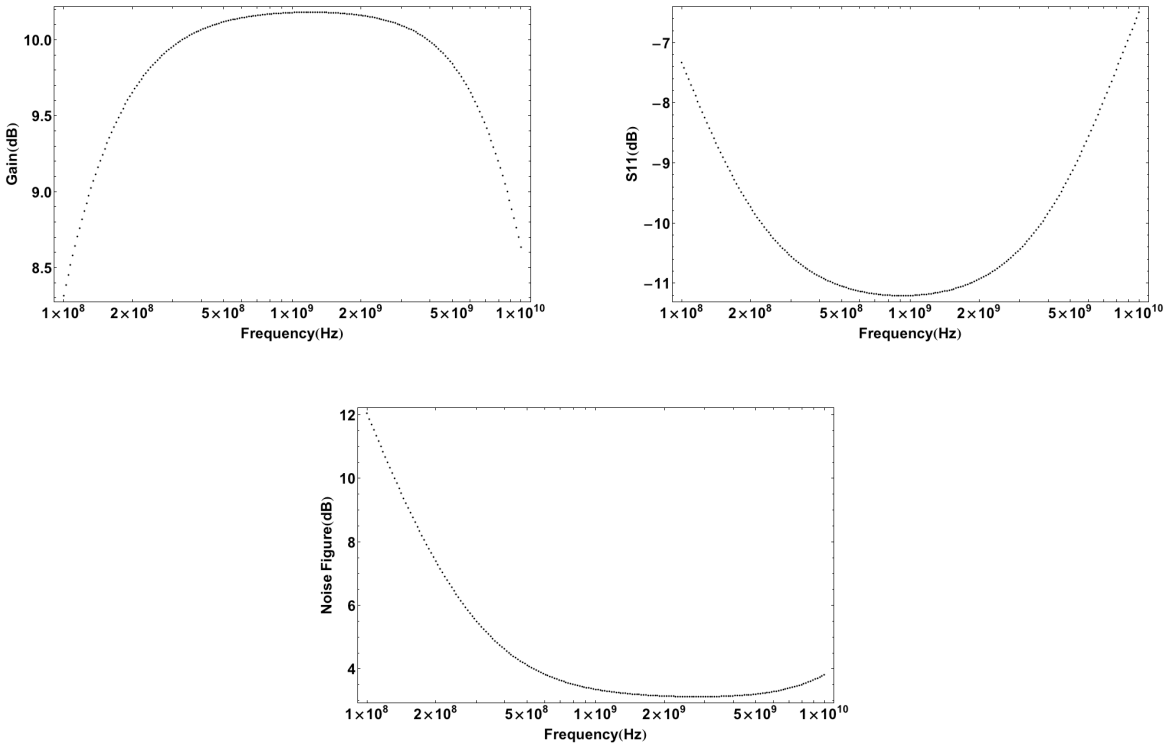


Figure A-20. Gain, S_{11} and NF plots of LNA_C.

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