INSTITUTO SUPERIOR TÉCNICO
Universidade Técnica de Lisboa

PLASTIC

CIRCUIT PROJECTION, CHARACTERIZATION AND MODELLING

António de Matos Tavares Proença

Dissertação para obtenção do GRAU DE MESTRE em

Engenharia Electrotécnica e Computadores

Júri

Presidente: Prof. Marcelino Bicho dos Santos
Orientador: Prof. Nuno Gomes Cavaco Horta
Co-Orientador: Prof. Jorge Manuel Ferreira Morgado
Vogais: Prof. Jorge Manuel dos Santos Ribeiro Fernandes

Abril 2010

ACKNOWLEDGEMENTS

The author would like to tank to Prof. Nuno Horta who was the coordinator of this Msc thesis, and gave excellent advices and support for the realization of this work. The author would like also to tank to Prof. Jorge Morgado (the co-coordinator) for supplying the experimental data, explaining the technology and construct the devices. Also the author would like to tank Victor Pelado and Samuel Pinto, the authors of the previous work, for giving support for the work already developed and being at fully disposal for questions about this last. The tanks go also to Prof. Helena Fino, for giving directions and advices in the construction of the models.

The author would like to dedicate this work to his family and friends.

ABSTRACT

The advances in polymer semiconductors open some perspectives in flexible integrated circuits applications. Although this new generation of electronic circuits is not expected to achieve nor overcome the typical CMOS circuits' performance, they are expected to conquer their one space in some particular applications that can benefit from low cost production systems and do not require high speed processing.

This work aims to contribute to the organic circuit technologies' development by introducing new device models that enables circuit design with support of VHDL-AMS simulators. The development of the model is accompanied by experimental tests on organic devices, in a retroactive process that makes the adjustments easier. This work continues the previous work done by analysing a new technology among with extending the existing system capabilities in data acquisition and by analysing new polimer semiconductor technologies.

The final goal is to use the developed models in circuit design and simulation.

KEYWORDS

Organic Technology, Simulation, Model Implementation, Circuit Design

RESUMO

Os avanços recentes em tecnologias de polímeros semicondutores vieram abrir novas perspectivas ao nível das aplicações para circuitos integrados flexíveis. Apesar de não se esperar que esta nova geração de circuitos electrónicos venha a alcançar ou superar os desempenhos típicos de tecnologias CMOS, é expectável que em aplicações que possam beneficiar de um baixo custo de produção e que não necessitem de velocidades de processamento elevadas, esta tecnologia possa conquistar o seu próprio espaço.

Este trabalho visa contribuir para o desenvolvimento das tecnologias de circuitos orgânicos, apresentando modelos de dispositivos que possibilitam o projecto e simulação de circuitos em simuladores baseados nas tecnologias SPICE e VHDL-AMS. O desenvolvimento do modelo é acompanhado por testes experimentais em dispositivos orgânicos, num sistema de correcção retroactivo que facilite o processo de ajuste dos parâmetros do modelo. Este trabalho pretende continuar o trabalho efectuado anteriormente estendendo as capacidades do sistema de medida desenvolvido e estudo de modelação de novas tecnologias de polímeros semicondutores.

O objectivo final é a utilização dos modelos desenvolvidos para o projecto e simulação de circuitos em tecnologias orgânicas.

PALAVRAS-CHAVE

Tecnologia orgânica, simulação, implementação de modelos, projecto de circuitos.

TABLE OF CONTENTS

List of Figures

List of Tables

LIST OF ACRONYMS

TFT – Thin Film Transistor

MOSFET – Metal-Oxide Silicon Field Effect Transistor

OFET – Organic Field Effect Transistor

OTTB – Organic Test Board

VHDL-AMS – Very High Speed Integrated Hardware Description Language with Analogue Mixed Signal Extensions

SPICE – Simulation Program with Integrated Circuit Emphasis

OLED – Organic Light Emitting Device

OTFT – Organic Thin Film Transistor

1. Introduction

Plastic is a project concerning fully patterned all plastic integrated circuits. The main objectives of this project, are to establish solutions to model and built integrated circuits using this technology. This work intends to be a continuation of a previous work done as referenced in [11], and extends the study related to the process of modeling organic technology. This project was developed in Instituto de Telecomunicações (Lisbon) in collaboration with Instituto Superior Técnico and the Polymmer Materials Research Group (Instituto Superior Técnico), as a MSc thesis to conclude the Master Degree in Electrotechnic and Computer Engineering.

Polymer electronics, in few applications to the moment, are becoming an alternative to all-known silicon based technology in areas of low performance and low cost circuits. This technology allows much more cheaper and resistant circuits. The ease of these devices fabrication and the conditions required for the device fabrication, makes organic devices an important technology to model.

Organic field-effect transistors (OFETs) and organic thin-film transistors (OTFTs) have gained considerable interest due to their potential applications in large-area, low-performance, low-cost integrated circuits, as referenced in [5]. Organic field-effect transistors, organic thin-film transistors, organic light-emitting devices (OLEDs) and organic solar cells are already being used individually, or together in integrated circuits with satisfactory results, as stated in [2], [3] and [4].

As this works intends to be the extension of the previous one regarding the study of dynamic simulation of organic transistors. Also in this work, a new type of organic device technology is used for study and develop of models. New simulation technologies are also used in comparison with the technology used in the previous work for result comparison in static and dynamic model simulation.

1.1 Organic Technology Overview

Organic devices nowadays have great advantages for appliance in circuitry. From RFID tags to cell phones with OLED displays. The main advantages of this technology consisting in low power consumption, cheap build process and flexible circuits opens new opportunities for circuit implementation nowadays. The properties and capabilities in circuit development are introduced in this section for a start view regarding theses devices. The next subsections are intended to be a introduction to the organic technology properties, circuit implementation and model construction for simulation porposes. This section intends to be a resume and update of the current introduction presented in the previous work referenced in [11]. This section intends to be an introduction to new

device studied in this work. For a detailed introduction to the OTFTs, the previous work can be consulted.

1.1.1 Organic Device Structure and Properties

Organic semiconductors have low charge mobility. It's important to mention the comparison with inorganic semiconductors, as organic devices have much lower charge mobility, with such values of charge mobility reaching about 10^{-3} $cm^2 V^{-1} s^{-1}$ in disordered molecular systems or polymers. Although in more arranged molecular systems, the mobilities can reach 1 $cm^2 V^{-1} s^{-1}$ or higher. This is a disadvantage regarding the mobility of inorganic semiconductors which assume mobilities of 10^3 to 10^4 $cm^2 V^{-1} s^{-1}$ [4]. By having low charge mobilities, one of the goals of the development of organic technology consists in increasing the semiconductor charge mobility.

Most of the organic devices' charge transport consist in positively charged carriers (p-type devices). Although there are also some devices, were the charge transport is made by negatively charge carriers, but must remain in vacuum because they became degraded when exposed to air. For curiosity, there are also Ambipolar FETs [8] which can establish both properties mentioned above, opening a new possibilities regarding circuits built with complementary technology.

As a consequence of having small mobility, the need of higher voltages becomes a need. Common values vary between 12 V and 80 V. Also when manufactured properly under certain conditions, these devices are flexible. This makes the appliance and design of the devices in which the circuit are built in a challenge for designer and opens doors for new design ideas.

In this work, the device studied for dynamic model building is a F8T2 based semiconductor. The organic semi-conductor material of the device studied for dynamic model building in this work, is known as dictylfluorene-bithiophene – a polymeric organic liquid crystal semiconductor. This material is also known as F8T2, for easier reference is going to be called this way. F8T2 has many advantages, such like dissolving in solvents. This material has voltage values with range from 10 V to 60 V usually. The charge mobility is small and situated near 1.5 x 10^{-3} cm 2 V^{-1} s -1 [15].

1.1.2 Organic Devices' Development

The advances in the field of conjugated polymers allowed to develop field-effect transistors using organic materials. The majority of the devices fabricated, when comes to transistors, consists in TFT devices. For better understanding, in figure 1.1 the two most common designs for OTFTs are presented. As observed, the only difference between the two designs is the position of the

semiconductor polymer film, which can be above or bellow the source and drain contacts.

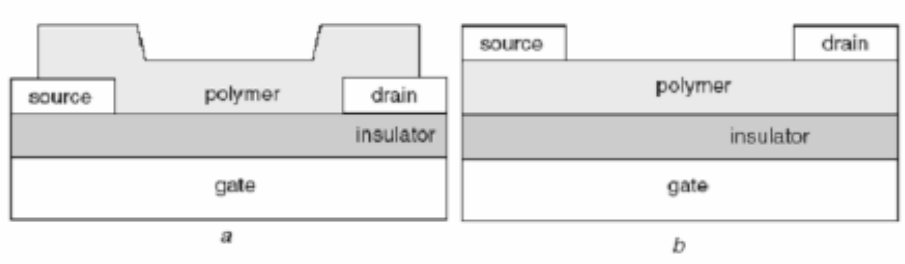

Fig. 1.1 - Typical Structures of OTFTs: a) – Bottom contact configuration; b) – Top Contact configuration.

These transistors have similar behavior (regarding working principles) when took in comparison with the p-type metal-oxide semiconductor field-effect transistors. They operate in accumulation regime, rather than in inversion.

The device used in this work, follows consists in a OTFT with the semiconductor made from F8T2. In figure 1.2 the device structure is presented. This device follows the Top Contact configuration presented in figure 1.1–b.

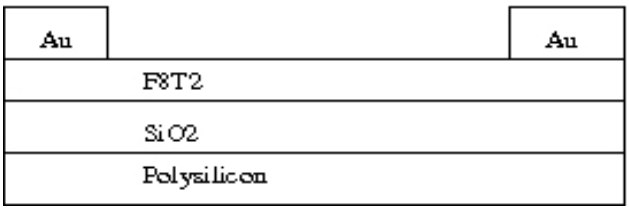

Fig. 1.2 - F8T2 TFT structure of the device analyzed

F8T2 has the advantage of dissolving in solvents making easy the fabrication process, which consists in the application of a thin layer of F8T2 above the dielectric. It's important to notice that this device consists in a hybrid design, due the fact that only the semiconductor is made from organic material. The gate is made with polysilicon (extremely doped silicon) and the contacts are made from gold (Au). The dielectric is made from Silicon Dioxide (SiO_2). These devices are p-type transistors and operate in enhancement mode. The main advantage of these transistors is the capability of being used in organic circuit printers which opens possibilities of cheap, effective and automated built of organic circuits as stated in [15].

1.1.2 Organic Circuits' Development

As already mentioned, the devices analyzed consist in p-type devices. This originates a difficult problem when applying a complementary approach to circuits design as n-type transistors using this kind of material are fragile to air. Circuits using this technology are non complementary, and this makes the designs having to be implemented in such manner also. For dynamic study, simple circuits using these devices have to implemented for circuit response measures. Next, two circuits using P-Type OTFTs are presented establishing the introduction to the application of these devices among with the discussion of their characteristics and performance.

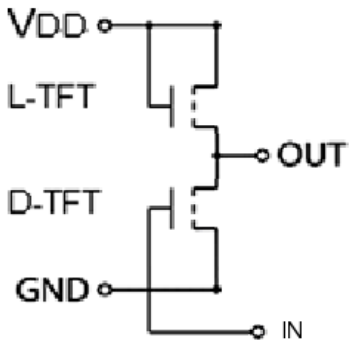

Fig. 1.3 - An F8T2 Inverter

Regarding the study of transistors, the first circuit presented must be the voltage inverter. A voltage inverter can be build with two P-type OTFTs using F8T2 semiconductor material. In figure 1.3, an inverter is displayed as found in [15], as a component of a ring oscillator circuit. The L-TFT acts as an active load, and the D-TFT acts as a driver or a switch. The idea is this circuit invert the input signal making it reach about 0 V in the output when the input value is equal to V_{DD}, and making the output reach the value V_{DD} when the circuit has 0 V in the input. This topology of inverter is known as the active load inverter, which consists in having a enhanced mode transistor acting as a load and the other doing the drive.

For a more complex circuit using F8T2 technology, figure 1.4 displays a ring oscillator built with F8T2 devices as referenced in [15].

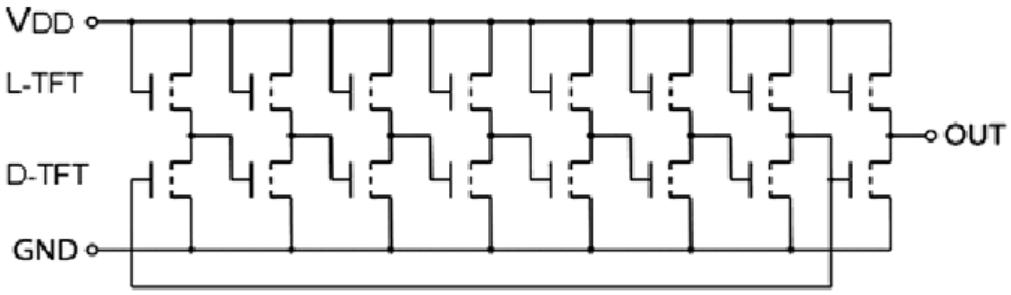

Fig. 1.4 - F8T2 ring oscillator

In [15] the ring oscillator circuit presented in figure 1.4 obtained good results. As can be observed, this ring oscillator consists in seven inverter stages, the last inverter (the last inverter reading from left to right) acts as a buffer stage for uncoupling the output signal.

1.2 Simulation of Organic Technology

Regarding the simulation of organic devices in the research found in [3], [5], [6], [7], [11] and [15]. There were found various sets of models able to simulate organic devices. It's important to introduce the simulation technology available for simulation of organic devices. Most of the models found are sustained only in DC Sweep Analysis but some models found have dynamic capabilities and can sustain Transient Analysis also. The main interest in this work is to found models able to simulate organic transistors both static and dynamically.

1.2.2 Parameter Extraction

Parameter extraction processes usually are used due the problem of not having concrete information regarding physical values such as the semiconductor charge mobility, for example. This speeds up the process of model building, since this method is used to extract the parameter values of a determinative model. A system for parameter extraction was built in the previous work consisting in a solution called the Organic Transistor Test Board [11], OTTB for short. The OTTB solution was used with good results in the previous work, having a good system for parameter extraction. The solution was based in the SILVACO's UTMOST tool [16] in which it's porpose is to extract the necessary model parameters for simulation. In figure 1.5, the architecture of the procedure is demonstrated.

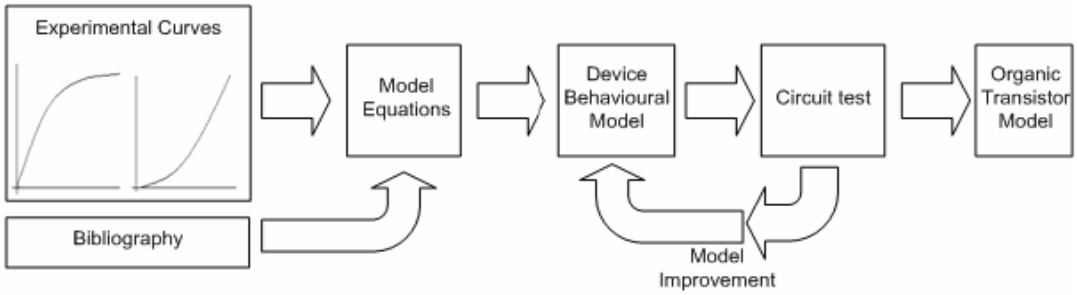

Fig. 1.5 - Solution for building a organic transistor behavioral model

As can be seen in figure 1.5, this method depends on experimental data taken from laboratory using the desired organic devices. This is method is used for static model parameter extraction, but with other measuring devices, such as an oscilloscope and very little alterations to the architecture it can be extended for the extraction of dynamic parameters.

In these work the OTTB solution is used with the new F8T2 devices, although other technique is analyzed and implemented for optimal parameter extraction. The other technique found consists in using non-linear optimization for extracting model parameters [17]. These technique comes handy, when comes to speed up the parameter extraction process and haves no dependency on the simulator used, only the mathematical model expressions are used. This allows more flexibility due the origin of the experimental data, which can come from other sources that were not measured with the OTTB system.

1.2.2 Static Organic Models

Organic static simulation is presented in many works. Already some models are used with success for organic circuit simulation. Some models found follow a simplistic approach, having only the the semiconductor conductivity and geometrical properties as factors in the simulation model. For further reference, [3], [7] and [11]. Models of this type of complexity were used in the previous work and obtained good results. Other models can be found having a more complex structure having also the temperature factor, which allows more realistic simulations as referenced in [5] and [6].

These models allow DC Sweep analyzes giving simulation possibilities regarding the DC behavior of the desired device or circuit. This comes handy when simulating simple digital circuits, since the exigence of the rigor of the analysis is not too ambitious.

1.2.3 Dynamic Organic Models

One of the main problems in organic simulation comes when time is also a factor having in account in the simulation. This happens when there is the need of knowing the circuit performance regarding frequency and evolution of the signal through time. This makes the urge of the necessity of having a dynamic model for the desired organic device.

There is little information about dynamic models for organic transistor devices, although some models were found in [5], [6] and [15]. Some models part from the charge orientated approach [5] [6]. There is a model found in [15] which was used with the F8T2 technology with success. According to [15], this model is able to represent the F8T2 dynamically and demonstrated average results with the inverter circuit and the ring oscillator. Also in [5] the OFET capacitances are included making the possibility of being able to implement a dynamic model also.

This models allow to extend the simulation types to Transient and AC analysis extending the possibilities of more complex organic circuit development and implementations. Also contribute to digital circuit development, making possible the analysis of clock frequencies and time responses.

1.2.4 New simulation technologies

All the models found were implemented in the well known simulation technology – SPICE. SPICE simulation technology is widely used for simulation in with silicon based semiconductors. The problem comes in hand, is that SPICE doesn't have organic devices in their devices libraries and makes the developer of the model define circuits in which complex devices are used for simulation.

Due the complexity of the dynamic models found through the consulted bibliography [5], [6] and [15], new simulation technologies were also took in consideration for organic circuit simulation. Having the need of generating new models for DC analysis as a consequence of the need of having the dynamic model. The new simulation technology also taken in consideration in this work, is VHDL-AMS, which demonstrated a lot of potential for model construction and simulation [10], [9] and [16]. All the models part from the deduction at least of the DC model and, the expressions obtained are of several complexity for using in a simulation technology with poor behavioral extensions such as SPICE. For dealing with these issues, new simulation technologies were took in consideration for ease the process of dynamic simulation of the organic technology, since these technologies are more orientated to model definition. This work pretend to extend this field in the consideration of other technologies as a possibility to have better simulation quality for organic device simulation.

1.3 Previous work

As mentioned already in this chapter, this work continues a previous study done by other colleagues in this particular area. The authors are Samuel Pinto and Vitor Pelado. Further reference about the study of various transistor devices using organic technology and models for static simulation can be consulted in [11].

These two authors worked with one of the same simulation technologies used in this work. They develop static models in SPICE, to simulate this technology. The major achievement was the developing of a measure system, which could acquire experimental data points. The acquisition consisted basically in two GPIB controlled fonts, a test board (OTTB) and developed acquisition software – the PME. With PME, experimental acquisition could be made making DC sweeps, and then experimental data can be fitted using HSPICE and a fitting algorithm for model parameter estimation.

1.4 Objectives of the Work

The main objectives of this work, are to extend the techniques developed in the previous work and supply a good model able to simulate the measured organic technology dynamically. Both static and dynamic simulation support are intended to be added to the models for allowing DC, Transient and AC analysis. The final goal of this work, will be the attempt to develop an organic inverter with the help of simulation technology as the dynamic model is of extremely importance regarding the ability of complex circuity development using organic devices.

This work also, intends to result in additional tools and features to the previous developed software and incorporate hardware extensions to the previous solution for posterior development of dynamic models.

1.5 Structure of the Dissertation

After the bibliographical research done to gain knowledge of the organic technology's state of art in modulation, the following chapters will present the developed works needed to achieve the organic circuits' simulation having dynamic capabilities and with the selected new technology.

In chapter 2, the line of thought for developing an organic dynamic model is presented and possible implementations in the selected simulation technologies discussed. The advantages and disadvantages of each simulation technology for the capacity of representation of the models obtained in bibliography.

In chapter 3, the new solution architectures for generating static and organic devices are presented and discussed, meeting the need for using the new chosen simulation technologies. Additions to the previous developed test board are presented and explained. Example results for the application of the new solutions for parameter extraction are presented.

In chapter 4, various models obtained from bibliography are presented for decision on which is the best able to simulate the new technology tested in laboratory. This chapter ends with the simulation results obtained by using the best fitted model and the comparison against the experimental data.

In chapter 5, the dynamic models found in bibliography are presented both large and small signal variants. The simulation results are presented and taken in comparison with the experimental data.

In chapter 6, simple circuits using the models pruposed in chapter 4 and 5 are simulated and the results analyzed for analyze the efficiency of the proposed solutions in chapter 3.

Finally, in chapter 7, the general conclusions of the entire work are made. Aspects that should be improved are presented as also actions that have to be taken in consideration for the improvement of the organic developed models.

1.6 Chapter's Overview

In this section an overview of the organic technology was presented having special attention to the F8T2 semiconductor technology, which is used in this work. The main characteristics of the organic devices were introduced among with their applications nowadays were described. The objectives of this work, having in consideration the previous work done were also presented.

2. Organic Transistor Modeling and Simulation Technology

This chapter intends to expose various techniques found in bibliography for organic modeling. These techniques pass from the experimental data treatment through the model simulation and ending in the parameter extraction, according to the objectives of this work. During this chapter, the group of ideas and solutions found in bibliography are exposed and discussed. The main goal is to present the various techniques which are intended to be used for the developing of models able to simulate the measured organic technology both static and dynamically.

2.1 Organic Transistor Model Building

The approach for organic transistor model building based in acquired experimental data can be expressed in the architecture presented in figure 2.1. As figure 2.1 demonstrates, organic transistor model building starts with three components: mathematical model which was acquired from bibliography, experimental data consisting in data acquired from laboratory and the already known parameters which enter in the definition of the mathematical model.

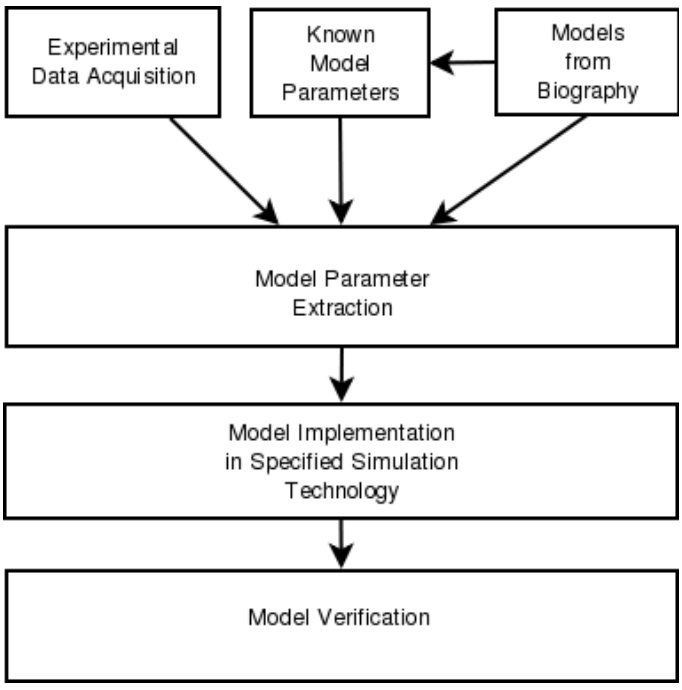

Fig. 2.1 - Process for building an OFET model

This process, as figure 2.1 describes, starts through the acquisition of experimental data and the consideration for the desired mathematical model. After these, the model equation parameters are extracted from already known parameters and from the experimental data acquired. The final process is to choose a simulation technology and built the desired model. In the next sub sections each task of this process is described.

2.1.2 Known model parameters

Organic transistors modeling process starts with two sets of parameters, the known parameters and the unknown parameters. The objective of the process described above, consists in the extraction of the unknown model parameters.

There are several that can be already parameters known in the target device, namely the charge mobility of the semiconductor and the geometrical parameters of the organic device. The number of parameters which belong to this section, depends on the model selected to simulate the desired organic device. The organic models found during research are relatively simple most of them, making the number of unknown parameters small and the curve fitting techniques for the unknown parameter extraction comfortable.

Due the amount of variables needed, the isolation of the known parameters is of most importance. The ideal panorama consists in having few parameters to extract, due the fitting algorithms could result in convergence problems if the panorama stands in having too many parameters to extract.

2.1.2 Experimental data acquisition

Experimental data acquisition for organic transistors results, usually, in automated acquisition systems. When acquiring experimental data, it's important to ensure the quality of the acquired data for organic model building. This happens because it's from here that comes the unknown parameters that must be deducted for a successful reproduction of the organic device. One of the major issues that has to be taken in consideration in this process is the signal noise, due the small amount of current which these devices operate (sometimes around the pA, or 10^{-12} A) that can create difficulty in the data acquisition process. Next, several techniques for transistor parameter extraction are presented.

General Method for Static Data Acquisition

In [11], the method used successfully for static data acquisition consists mainly in the acquisition of I-V experimental curves, usually source-drain current (I_{SD}) relation between source-gate voltage (V_{SG}) or source-drain voltage (V_{SD}). This data is acquired through the use of a measuring

system consisting in voltmeters and ammeters. Some automated systems were built for this porpose, and in this work the intention is to use the already built system of the previous work, the OTTB [11]. After the data is acquired, the static model parameter extraction process can be initiated if desired. In figure 2.2, the measuring circuit diagram for extraction of this data can be observed.

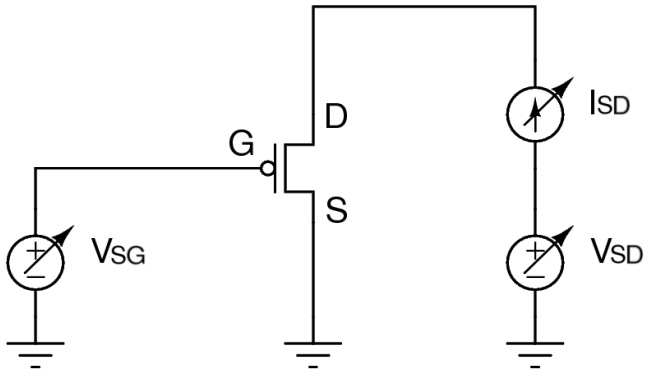

Fig. 2.2 - Measuring circuit diagram for static model parameter extraction

As can be seen in figure 2.2, the system consists in one ammeter and two voltage sources. The behavior of the system consists in the one of the voltage sources performing a DC sweep as the other one is at a fixed value, after this the I_{DS} current curve is acquired. First, V_{SG} DC source starts sweeping between the desired voltage interval. When the sweep finishes, V_{SD} DC source is increased and V_{SG} voltage source starts sweeping again. After V_{SD} DC source finishes at the last desired fixed value, the process begins again by changing the roles of the DC sources: V_{SG} DC source becomes the fixed source, and V_{SD} DC source becomes the voltage source which performs the DC sweep. When this process finishes, a set of $I_{SD}(V_{SD})$ and $I_{SD}(V_{SG})$ curves is obtained.

For dynamic model building, the previous solution is not sufficient. The time factor must be included for extraction of the capacitances of the device. To study the evolution of the device in time, a new circuit diagram has to be taken in account. In [17], there is a methodology which revealed satisfactory results to be used for capacitance extraction. This method consists in using a LCR meter for capacitance measure, and it's known as the low frequency quasi-static method. In figure 2.3, the measuring circuit diagram for extraction of the C-V curves is demonstrated.

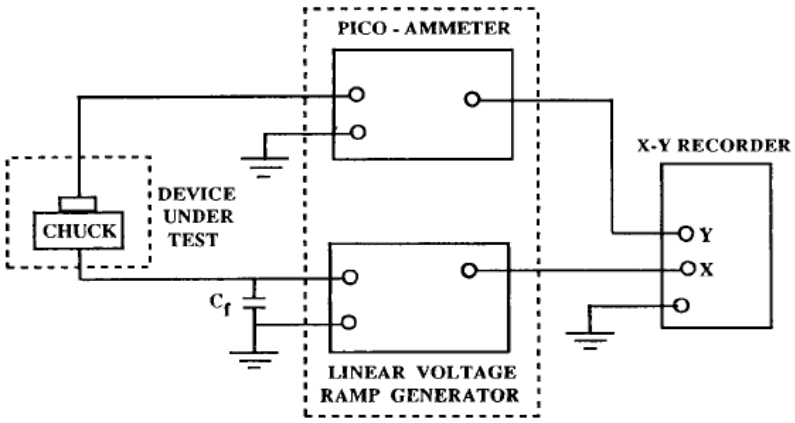

Fig. 2.3 - Circuit Diagram for capacitance measurement using quasi-static method

As the ramp generator sends a ramp signal with certain amplitude for the device, the pic-ammeter extracts the current, and calculates the capacitance from the periodic signal. The X-Y recorder, which can be and oscilloscope makes the registry of the I-V curve of the device through time. After performing the measuring, equations 2.1 and 2.2 give the capacitance desired. Equation 2.1 represents the ramp signal, and equation 2.2 the deduction of the capacitance from the current measured over the desired device.

$$V = V_0 + rt \tag{2.1}$$

$$i = \frac{dQ}{dt} = \frac{dQ}{dV}\frac{dV}{dt} = Cr \tag{2.2}$$

Where,

- r – is the slope of the ramp signal;
- Q – the charge in the desired channel;
- I – the current passing in the device;
- C – the capacitance desired to measure.

Due the capability of the LCR meter to supply the capacitance directly, the calculations become unnecessary and making this method of easy application.

In [18] references other way of acquiring the capacitances of a transistor device is by the use of an oscilloscope. This method is known as the transient analysis method. In figure 2.4 the circuit

diagram is exposed.

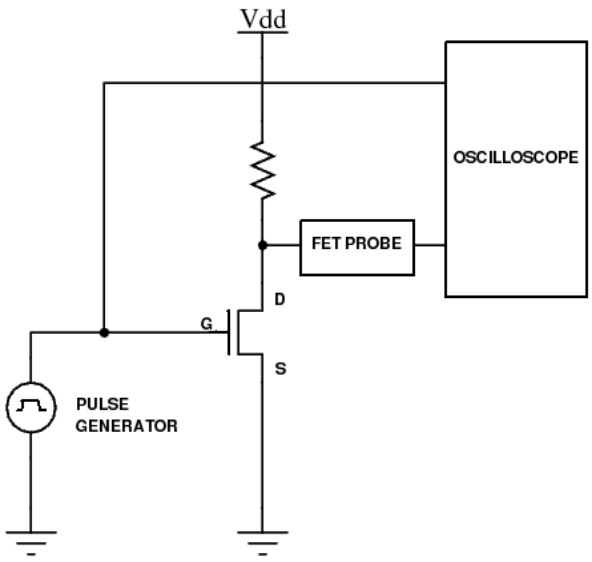

Fig. 2.4 - Circuit diagram for capacitance measurement using transient analisys method

The idea behind the measuring circuit diagram presented figure 2.4 is of establishing the relationship between a pulse of signal defining the V_{GS} signal and I_{DS} current, measured which a FET probe for being able to covert the passing current in to an equivalent voltage signal for translation of the current to the oscilloscope. After this, the evolution of the current through time is plotted as the V_{GS} ramp. After this procedure, the transistor device intrinsic capacitance can be extracted by using the desired model equations regarding the capacitance expression for the Gate-Source capacitance – C_{GS}. The relationship between the measured data and the respective capacitance follows equation 2.3.

$$C.[\Delta V]=[\Delta Q] \Leftarrow C.[\Delta V]=\frac{[\Delta I]}{[\Delta t]} \Leftrightarrow \frac{[\Delta I]}{[\Delta V]}=C.[\Delta t] \tag{2.3}$$

In conclusion, this method follows the same principle for capacitance extraction as the quasi-static method, the difference is between the devices used in the acquisition process and the way of measure them.

2.1.3 Models from bibliography

This process consist on choosing the most adequate mathematical model or models for reproduction of the experimental data curves obtained in the data acquisition. The model choice depends of the organic device, for certain organic technologies some models have better results than

other models. The designer must choose the best model for the desired organic technology through the comparison of the experimental curves and the generated curves, when observing the simulation results. In [20] it's proposed a quality standard for analog models. In this work, this standard was adopted as a qualification tool for the OFET models found in bibliography and analyzed for parameter fitting of the TFT devices measured in laboratory. The Model Quality Chart is used in this work to qualify:

- Accuracy - A candidate model should give reasonably accurate results for
  - I-V characteristics,
  - speed predictions for logic circuits,
  - propagation delays at the individual nodes within the circuit,
  - voltage levels and noise margin determinations,
  - a reasonable range of bias voltages and temperatures.
- Capacitance Modeling - The model should include proper modeling of the transistor capacitances like gate-source and gate-drain capacitances. The accurate simulation of time-dependent voltage levels and signal shapes depends on the correct modeling of these capacitances.
- Compactness - The model equations should depend on as few parameters as possible:
  - There should be a strong relationship between model parameters and parameters reflecting device structure and fabrication processing (channel thickness, number of trap states, etc.). Such a model would be especially useful in statistical circuit analysis where effects of variations in fabrication and parameter distribution are accounted for in order to be of service in statistical circuit analysis, empirical parameters without physical meaning should be avoided.
  - The model accuracy should not depend on the geometrical dimensions of each device, so one set of model parameters should be valid for all devices of the same type and fabrication process.
- Parameter Extraction — The process of parameter extraction must be easy and straight-forward:
  - The number of required test devices and measurement procedures for the parameter extraction should be kept as small as possible.

- Ideally, model parameters are directly resolved using analytical reasoning without much computational effort.
- Alternatively, if general-purpose optimization techniques are used, they must not fail due to numerical instabilities.

When performing model selection, the preference should concentrate in models with small equation complexity due the risk of increased difficulty when performing the parameter extraction, although it's possible to deal with this problem performing equation linearization. In chapter 4 and 5, the static and dynamic models found are presented and discussed among with the analysis of the parameters extracted using them.

2.1.4 Model parameter extraction

Model parameter extraction consists in the use of several techniques for parameter extraction. The chosen technique or techniques, depend on various factors regarding the type of model desired making the algorithms use the experimental data with the reproduced curves from the mathematical model and when the error between them is smaller enough, displays the result of the calculated parameter values. This process ends when the difference between the experimental data and the generated curves is acceptable.

One of the major disadvantages of model parameter extraction is the number of parameters desired to be extracted. This number must be small, as some parameters are inconclusive regarding the information presented in the acquired data. Fortunately, for an early stage of organic simulation and circuit simulation, the models taken in consideration contain a small amount of parameters to extract resulting in the possibility of having satisfactory results in a simulation environment.

As referenced in [17], there are two ways for extracting parameters from a MOSFET transistor device. As the OTFT model equations have similar behavior as the MOSFET equations, these result in the possibility of this methods being used also for parameter data extraction of OTFT data with the models took in consideration.

The first way for performing parameter extraction from a transistor device is by using linear regression (linear least-squares) method [17], which consists in using a linear approximation of the device equations and then applying the method for the zones were the desired model parameters are dominant. Although this method results in simplicity, demands also the choice of simple models for easy equation manipulation. In general, the use of this technique over a model results in parameters with physical meaning. For using this method over more complex models, the components which

dominate the model behavior must be isolated resulting in mathematical manipulation of the model equations. This approach is tedious and time consuming, although necessary for model parameter extraction.

Other way consists in using the optimization method, which consists in the parameter extraction using curve fitting over the experimental data. The main advantage is the capacity of appliance of this method over all the regions of operation of the OFTF experimental data through the use of nonlinear least square optimization [17]. This technique starts from a “educated guess” and after that numerical methods are used for minimize the error between the model and the measured data. The “educated guess” can be obtained using the linear regression method, for example. The drawback of this method is that any combination of values will provide a working fit to the measured characteristics due there being sufficient iteration between the parameters. Thus, is not always clear as to which are the correct values. Further, parameter redundancy can lead to unrealistic physical values. This problem is relieved using constrains on the parameter values and/or using sensitivity analysis. The practical process using this method consists in separating the parameters in several group levels. The first group is the obvious deducted parameters which can be easily extracted from the equation and after the extraction, the next step is to freeze these parameters and pass to the next group of parameters to be deducted and so on until all the parameters are extracted.

2.1.5 Model Implementation in the specified simulation technology

After reaching the necessary model parameters for model implementation, a simulation technology is chosen. This simulation technology has the capacity of being able to produce simulations environments for stand alone device study, or for organic circuitry built. For static model building the stand alone device simulation is usually used, although for dynamic model building a circuit reproducing the acquired response of the circuit measured is simulated.

Basically, this process consists in the implementation of the mathematical model, and the substitution of the parameters values found which resulted from the model's parameter extraction process described previously. Depending on the simulation technology used, the model implementation approach is different. When implementing a desired model in a simulation technology, the model type used must be taken in account due possible difficulties regarding the technology limitations.

SPICE is a simulation technology with circuit simulation porposes, this simulation technology is well known regarding simulation of electrical circuits. This technology is silicon oriented and has various transistor device models in libraries. There is no organic device library in SPICE due this matter, the circuit model definition has to be taken in account if implementation in this technology is desired. In

SPICE technology, models are expressed as sub circuits. Having a model represented in a sub circuit, means that the equivalent circuit model of the transistor has to be taken in account if implementation is desired.

SPICE technology is the most used for simulation of circuits, it's circuit oriented and with the propose of circuit simulation. SPICE falls in the category of circuit description environments.

VHDL-AMS is other technology generally used for mixed-signal simulations and falls in the description language environments. Description language environments, such as VHDL-AMS, offer a framework for the development and implementation of arbitrary components and/or system models over a wide range of abstraction spanning from traditional, SPICE-like, component models to higher-level behavioral models [19]. It consists, when referring to a circuit description environment, in the abstraction of the use of circuit representations for model definition.

Having the possibility of circuit abstraction in VHDL-AMS, models can be implemented directly from the mathematical definition.

2.1.5 Model Verification

The final process consists in the model verification, is in this final stage were the simulation results obtained are compared to the experimental data. In this process, the results from the simulation are exposed with the experimental data, starting the process of data comparison and finding if the model was successfully implemented and if it actually simulates the organic transistor in analysis.

2.2 Establishment of the procedure for Organic Model Development

The establishment of the procedure for organic model development, stands for the division and implementation of the techniques exposed in section 2.1. The process flow takes in account all the necessary procedures for the generation of an organic transistor model. In figure 2.5, the path for organic model building taking the necessary steps is presented.

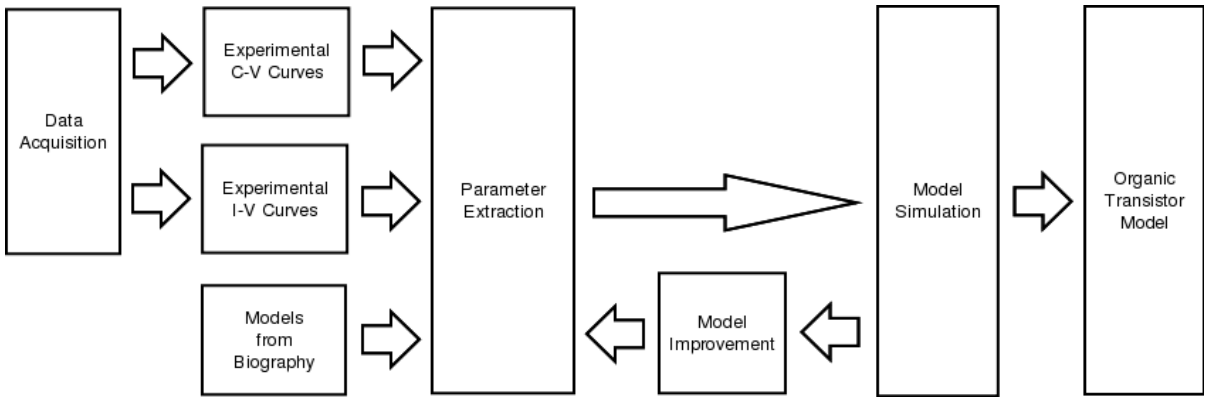

Fig. 2.5 - Path for organic model development

Starting with data acquisition, the experimental I-V and C-V curves of the device are obtained among with the collecting of the models desired to take in account to model the device using the static acquisition for the I-V curves and the desired technique for capacitance acquisition for the C-V curves presented in section 2.1.2.

After the conclusion of the experimental data, parameter extraction is performed using the fitting techniques exposed in section 2.1.4 of this chapter.

Following the end of the parameter extraction, these are supplied to the simulator and after the simulation finishes the results are analyzed conducting to the model improvement process. If the result are not satisfactory, parameter readjustment is made according to the detection of the parameters which are influencing the difference between the data fitted and the simulation response. If the result is satisfactory, the organic transistor model generation is concluded.

After having the path established for organic model development, the inclusion of the desired techniques and technologies is made. The advantages and disadvantages of each one, must be analyzed and after the choices being made the solution is defined.

2.3 Techniques' Comparison and Expected Results

As the most relevant techniques found in bibliography were presented in the previous section, this section intends to make the comparison and selection between them for the establishment of a possible solution for model development of organic transistors with both static and dynamic capabilities.

Starting from the previous work done, the OTTB solution managed to get good results regarding the static model building. In this solution, the support for dynamic parameter extraction implicated the building of circuitry, for example an inverter for turning the possibility of intrinsic

capacitance extraction from the desired device [11]. As mentioned in section 2.1.2, other techniques are available for capacitance extraction which could be of advantage regarding this issue. Although, the choice of having an LCR meter and an oscilloscope is very expensive. The method chosen must have in account which devices are available and/or which type of solution is most adequate in the general panorama of the solution system. As computation is generally free, the transient method is chosen.

As also regarding the parameter extraction, in the previous work, the simulator entered in the fitting process. Due the desire of including VHDL-AMS also as an alternative technology of model implementation, the solution passes by the isolation of the fitting process with algorithms capable of dealing directly with the modeling equations. Regarding the techniques for parameter extraction, the methods are not exclusive and makes possible the co-implementation of both. The linear regression is used first and the calculated parameters enter in the non linear optimization for best optimal parameter fit according with the desired model.

For dynamic model construction, the model complexity increases making harder to implement in SPICE technology some of the models found in bibliography. And having this issue in mind, VHDL-AMS is also used as a technology for simulation due the fact of being a description language and allowing to bypass this problem.

In conclusion, tables 2.1, 2.2 and 2.3 presents the advantages and disadvantages of the techniques presented in this chapter, having each table dealing with a relevant section of the organic model development process.

Tab. 2.1 - Comparison of the data acquisition techniques for capacitance extraction

Property	Quasi-static Method	Transient Method
Device(s) Involved	LCR meter, Oscilloscope	Oscilloscope
Computation Required for calculation of capacitance	None	Calculations of the acquired data for extraction of the C-V curves
Solution cost	High	Medium

Tab. 2.2 - Comparison of the parameter extraction techniques

Property	Linear Regression	Non-Linear Optimization
Quickness of algorithm	Slow	Fast
Analytical Model Equations Treatment	The expression must be linear, according to the model desired mathematical manipulation can be an issue	Almost none
Convergence Problems	Low	Medium
Requirement for separation of the device operating regions	Always, must be done for reaching linear situations for the operating process	Almost none – depends if the model equations used takes all the operating modes in account
Risk of non physical meaning of the extracted parameters	Low	Medium

Tab. 2.3 - Comparison of the simulation technologies available for organic devices

Property	SPICE	VHDL-AMS
Circuit Perception/Description	Node Based	Flux Based
Model Implementation	Weak Support	Strong Support
Analysis Tools	Good	Good
Language Syntax	Simple	Complex
Simulation Processing	Interpreted	Compiled
Line of thinking	Circuit description	Abstract/Behavioral description

2.3 Chapter Overview

In this chapter an introduction to the process of organic model development was presented, as the techniques which were taken in account for application to various areas of the described process. The solution for organic model generation must have in consideration static and dynamic capabilities was established. The chapter finished with the comparison of all the techniques presented demonstrating the advantages and disadvantages of each and mentioning the expected results.

3. Organic Model Building Solution – DC and Transient/AC model building

3.1 Introduction

In this chapter, the solution architectures for the static and dynamic approach for targeting the new simulation technology are presented. In this chapter, both architectures are also analyzed through every steps of both processes.

3.2 DC Solution Architecture – Static Model Generation

In this section, the solution architecture is presented in two different designs as consequence of the research found in [17], [18], [16] and the alterations deducted in section 2.2 and 2.3 of chapter 2. The final architecture for the DC organic DC model build is presented next in figure 3.1.

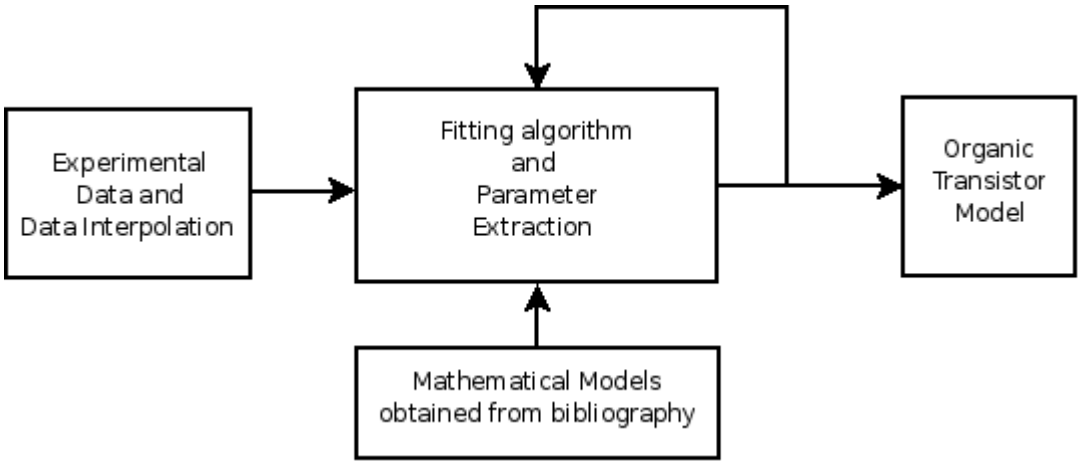

Fig. 3.1 - The architecture for DC OFET model building

The main difference between the previous solution architecture[11] and the new architecture, is due the use of another fitting algorithm for the parameter readjustment and as consequence of the use of VHDL-AMS technology. In the next subsections each of the sub-processes of this architecture are explained.

3.2.1 Experimental Data Acquisition

Consisting in various sets of experimental data took using the laboratory ampere-meters and voltmeters, characteristic curves of the OFET devices are took with the help of computer measurement software controlling these measure devices. Also was used the previous solution OTTB board[1] for extraction of the experimental data. The experimental data took for the new OFET devices can be consulted in appendix A.

The data took from the physical device consisting in the $I_{SD}(V_{SD})$ and $I_{SD}(V_{SG})$ curves, after acquired, is submitted to an interpolation process. Interpolation consists in a method for constructing new data points within the range of a discrete set of known data points. This method is used generally in experimental results, having the advantage of establishing a greater number of points for posterior fitting and parameter extraction. In MATLAB software, this is easily done with a simple command which receives a set of acquired data points. There are several types of interpolation in this process, the best results were given using Quadratic Spline interpolation in the MATLAB environment. After the data is submitted to the interpolation process, the process of fitting with the chosen model can begin.

3.2.2 Fitting algorithm and Parameter Extraction

The experimental data after being treated through the interpolation process, is ready for the fitting algorithm.

Non linear regression is a method which can be used for parameter extraction of a MOSFET model parameters against a measured experimental curve [17]. It is used for finding the optimal coefficients in a certain model (a function for example), and checks if the chosen model is able to define a certain domain of data points. The algorithm chosen was least squares approach.

This method basically verifies the following condition :

$$\min_{x} \frac{1}{2}\|F(coef, xydata) - zdata\| = \frac{1}{2}\sum_{1}^{m}(F(coef, xydata) - zdata)^2 \quad (3.1)$$

Where :

- coef is the actual group of coefficients
- xydata are the x,y data points which the given model must fit
- zdata are the z data points which the given model must fit also

Although this condition is specified for $\mathbb{R}^3$, it can be expanded for $\mathbb{R}^n$. The algorithm

begins with a group of chosen values (which are suspected) and makes iterations until it finds the best coefficients for the model that can define the given group of data points. This method allows running plastic transistors experimental data against some selected models and find which model best describes the experimental data. The main reason of choosing this particular fitting is the advantage of allowing the direct appliance of the mathematical equations which describe the desired model to be fitted. The major limitations of this algorithm is making sure that there are no discontinuities in the data points, and making sure that the algorithm doesn't get stuck in local minimum.

As a consequence of using non-linear regression, the mathematical equation coefficients of the OFET are extracted. These coefficients result in the physical parameters of the OFET model which were unknown. In section 3.2.3 the implementation of the solution architecture is described and examples of the developed tool are demonstrated.

3.2.3 Architecture implementation

After establishing the static solution architecture, the implementation is next step for establishing a solution for the generation of the static model which simulates the desired physical device. In the next subsections, the implementation of the whole process is described in detail and the results are displayed.

Matlab has a function that supply the method of non-linear regression which allows fast develop of a small application to run some known models against the current technology data. With this, is possible to find which is the best suitable model to describe the current developed technology and then build a DC model in a first phase and allows to extract the physical parameters of the measured device. The model fitting tool created is a simple Matlab command line application, the operation can be described in figure 3.2:

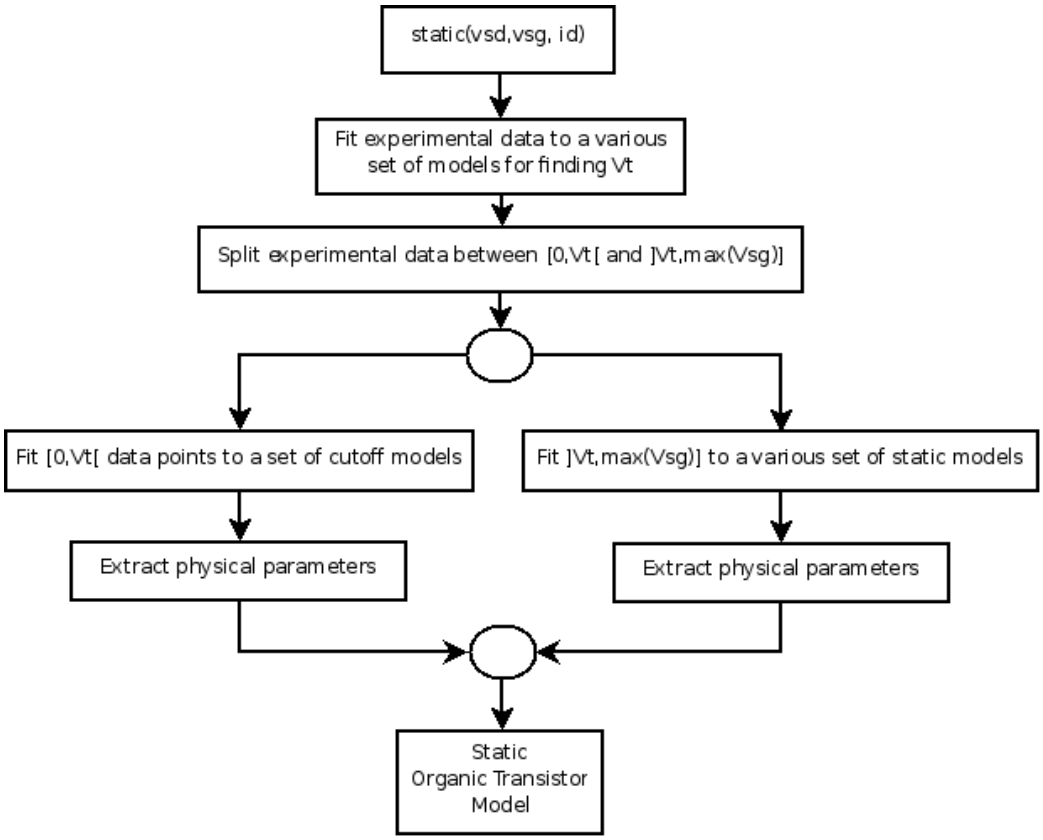

Fig. 3.2 - Algorithm Implementation Flowchart

Following figure 3.2, a flowchart is presented. As observed first all experimental data is took in consideration for discovering the Vt parameter. This is necessary because if $V_{SG} <$ Vt the OFET behavior can be compared to a simple resistor, for $V_{SG} \geq$ Vt OFET experimental data is fitted through a various set of static models. After the best model is chosen, physical parameters are extracted and can be supplied directly to a HSPICE or VHDL-AMS model. In the next section we use experimental data obtained from a F8T2-based device as an example of this process.

In chapter 4, the models found in the bibliography found in [8], [15] and [5] for describing plastic transistor's static behavior are described. The application described in the section above, will use these three models and show the curve fitting of each one. A user can chose which model best fits the experimental data, and obtain the physical parameters of the measured device. After this a HSPICE or VHDL-AMS model can be build. In this section the results of applying each model can be viewed. The device that is used for demonstration is a F8T2-based device measured in air after a curing of the film at 90 ºC for 15 minutes under vacuum. The data points extracted from the device can be viewed in figure 3.3. At first glance, we can observe that Vt is between 10 V and 20 V. After applying non linear

regression technique to the experimental data points, Vt gives approximately 15 V. So the split is made and data from V_{SG} between 0 to 10 V is separated from data between 20 V to 40 V. As the drain-to-source current depends of two node voltages, V_{SD} and V_{SG}, the experimental data is visualized through a surface.

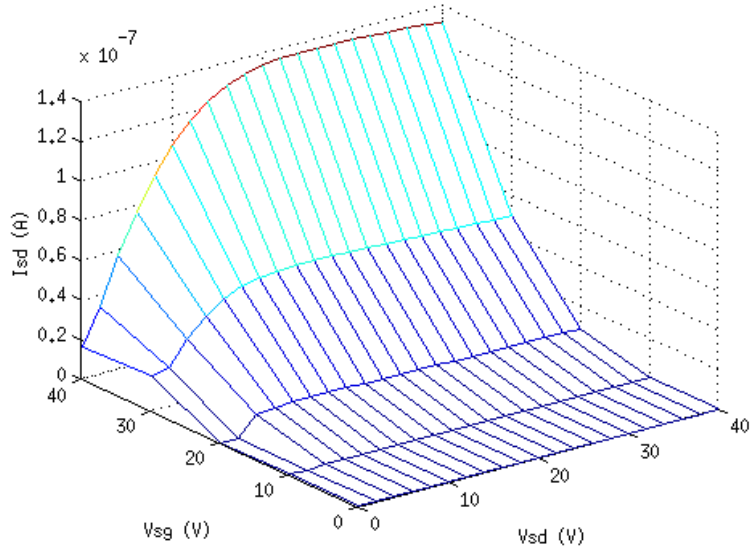

Fig. 3.3 - F8T2-based TFT device experimental data

After having the experimental data acquired and interpolated, the algorithm is going to run through the process described in this section. For example, the figure 3.4 shows a fitting result using Meijer's proposed Model[8]. For more information regarding the result obtained used the proposed solution, chapter 4 can be consulted.

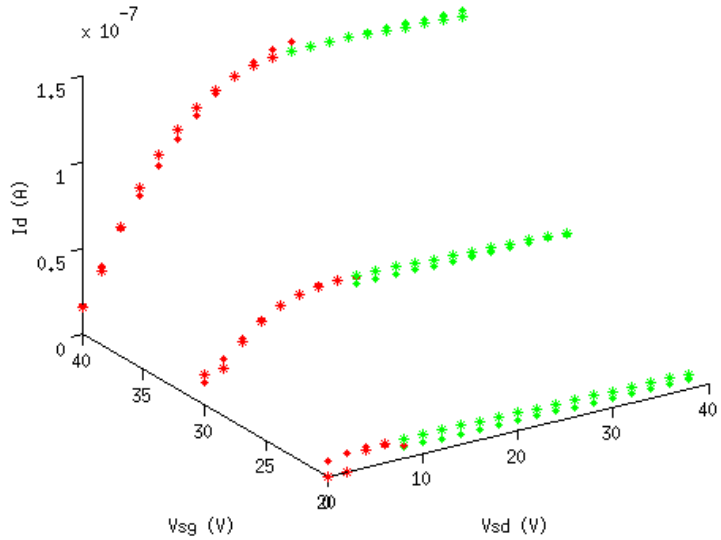

Fig. 3.4 - Experimental Data Vs. Meijer model in triode with losses drain-gate losses

3.3 Transient/AC Model Architecture – Dynamic Model Generation

In the bibliography found in [5] and [18], is possible to deduct a dynamic model from the static model equations and using the transient method, to perform a fitting process over the captured output capacitance. Regarding this approach, an architecture for the dynamic model was established for allowing dynamic model generation. This architecture is described next in figure 3.5.

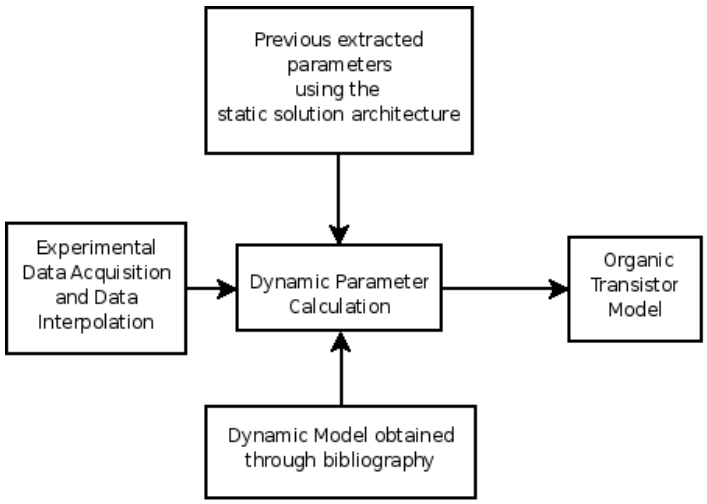

Fig. 3.5 - The architecture for Transient/AC Model building

The architecture established in figure 3.5, consists in the use of the architecture described in this chapter in section 3.2 and experimental data obtained using built circuits with the organic transistors for aquiring the C-V curves. In appendix A, the experimental data for C-V curves is obtained for better understoodment of the behaviour of the transistor capacitances between V_{SD} and V_{SG}.

3.3.1 Experimental Data Acquisition and Data Interpolation

The DC architecture solution, as described in section 3.2, needs to start from the experimental data and a set of models chosen from the bibliography. The Transient/AC solution, also needs the extracted static parameters previously taken by using the DC solution. Due this issue, first the DC solution must be run, and then the Transient/AC solution is run. For extracting the C_{IN} parameter, which stands for the intrinsic capacitance of the organic device.

The experimental data extraction for dynamic parameters is run through the building of two simple circuits. The circuits used are exposed next in figures 3.6 a) and 3.6 b).

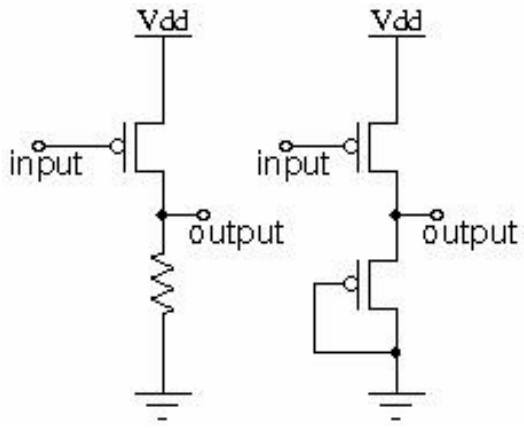

Fig. 3.6 a) and b) - circuits used in dynamic data acquisition

The circuits described in figures 3.6 a) and 3.6 b), consist in a simple p-type OFET with a load resistor and a p-type OFET inverter with enhancement load. The power supply for the circuit (V_{DD}) is -40V. The input is feed with a -40V pulse wave, which is supplied by the OTTB[11]. The input and output of the circuit are connected to a digital oscilloscope. In figure 3.7 the system for dynamic data extraction is described. This is the application of the transient method for capacitance extraction described in chapter 2. Due the resources available a ramp generator was available for being able to apply the quasi-static method. Which makes possible to measure the output capacitance of the transistor only, but applying the desired model equation, the transistor capacitances can be found.

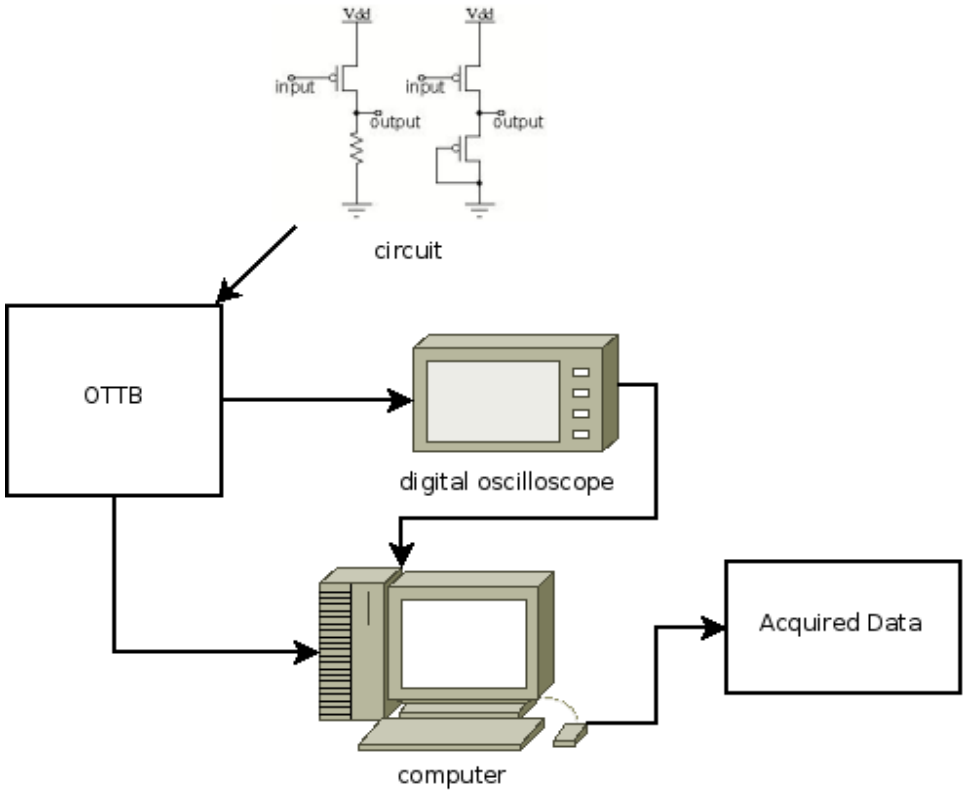

Fig. 3.7 - Dynamic data extraction system using the OTTB solution

As described in figure 3.7, a circuit is built in the OTTB solution board and the pulse generation is set, for more information the previous work can be consulted in [11]. A digital oscilloscope was added to the OTTB board for allowing the extraction of the circuit response and transfer of the extracted data to MATLAB, where the dynamic solution is built, for further interpolation and treatment.

The data interpolation method is the same used in the DC solution, this method is described in section 3.2.1. The circuit implements a surface of C-V curves, just like the I-V curves used in the static solution. Interpolation is run on C-V experimental curves for best parameter extraction performance and results.

3.3.2 Dynamic Parameter Calculation

Due research found in bibliography[5], the dynamic parameters of an OFET device can be calculated from the static extracted parameters of the device. Although, the unknown of several physical parameters, makes the need of working with C-V curves for founding which is C_{IN} value. The main problem is the need of knowing exact physical parameters of the organic device in question, such as the lattice temperature of the semi-conductor material and the effective temperature of this one,

which most of the times are unknown.

For the given solution in this work, a more simple approach was taken in consideration. First the DC architecture solution can be used, like described in the dynamic solution architecture in figures 3.1 and 3.2. After the static solution finished the DC model generation, the dynamic parameter calculation can be executed using the acquired response and perform curve fitting techniques for extracting the organic device output capacitance. In chapter 5 the equations which are used for fitting and the parameter extraction for the measured technology is given, in appendix A the fitting results can be consulted.

Non Linear Regression, just like the static solution, is performed using the desired model equations. The same procedure is used, having just in mind the fitting for one parameter only – C_{IN}. This makes the process easy for capacitance extraction and the algorithm itself, since it only has to concern with one variable.

After the dynamic parameters are extracted, a model is generated and a simulation is run. The simulation results are took in comparison with the experimental results and parameter readjustment can be made after the comparison.

3.3.3 Architecture implementation

Posterior to the establishment of the dynamic solution architecture, the implementation is the next step. In the next subsections, the architecture implementation for the dynamic solution's model generation is presented and described.

In figure 3.8, the flowchart describing the algorithm which the dynamic parameters are calculated is presented. This tool was created in MATLAB and allows the extraction of the output capacitance expression based in the experimental data. Curve fitting algorithms can be used depending on the known or not of the capacitance expression for the desired dynamic model.

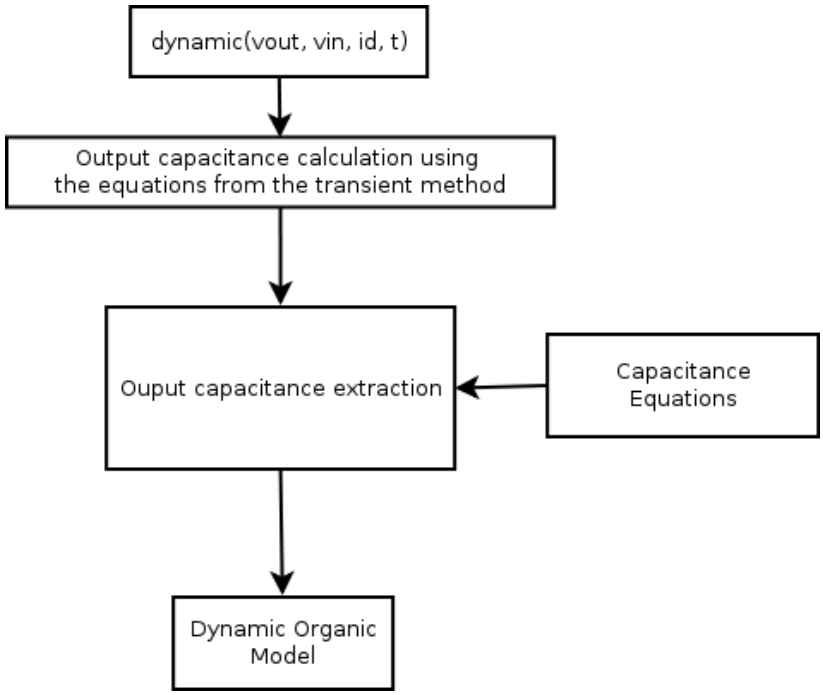

Fig. 3.8 - Algorithm Implementation for the proposed dynamic architecture

Basically, the intention here is to deal with the acquired data. The expressions for the capacitances, are extracted by performing curve fitting to the acquired data and then applying the model capacitance equations found in bibliography. After having the capacitance expressions, parameter fitting can be performed using the non-linear regression algorithm described.

After running the static solution proposed in section 3.3.1, the dynamic solution is executed against experimental data obtained using the circuit in figure 3.6 a). The figure 3.9, the demonstration of the capacitance extraction process result, after running the capacitance equations with the experimental capacitance measures.

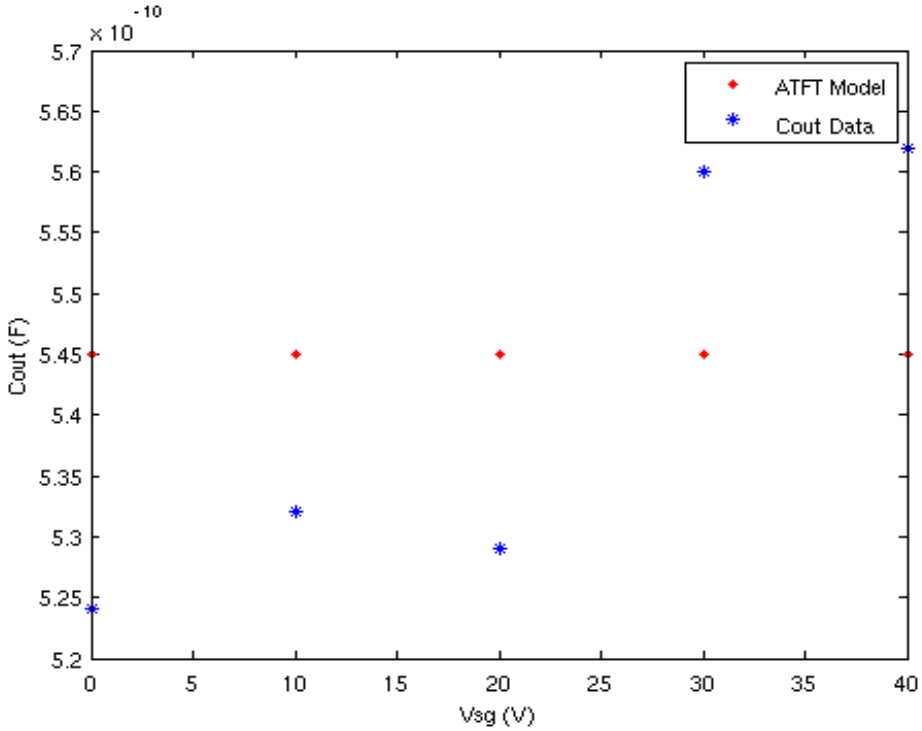

Fig. 3.9 - Output measured capacitance fitting using the ATFT model when Vsd = 40 V

Despite the fact that the capacity changes along with Vsg, and the fitting seems, awful. Although, the greatness of variation of Cout capacity is small and, as for ATFT model the capacities are constant. The this approximation, resulted in the C_{in} of 6.8×10^{-6} F/m^2 which is around the value deducted in [15] which is 7.1×10^{-6} F/m^2.

As we can see, we have a good approximation of the capacitances behavior of the F8T2 organic transistor as described in [5], making the goal for having a organic transistor model able of making transient simulations closer. In chapter 5, the fitting results are analyzed in detail for the models used with this solution architecture.

3.4 Chapter Overview

In this chapter a static and dynamic solution architectures were presented. After having the solution architectures established, the goal for generation of a large signal model and small signal model with static and dynamic capabilities becomes possible. In chapter 4 and 5, static and dynamic model generation are analyzed in detail and applied to a simulation and comparison with the experimental results with various set of models obtained from bibliography.

4. Organic Static Transistor Models

In this chapter, the solution architecture proposed in chapter 3 is run using experimental data obtained through laboratory and fitted to some models found in bibliography. In the next sections, these models are presented. The model fitting results and calculated parameters using the proposed static solution architecture for parameter extraction, as the code listings of the selected models for SPICE and VHDL-AMS can be consulted in appendix B.

4.1 Organic Static Model theory

There were found several organic device models in bibliography. These models having their advantaged and disadvantages regarding complexity and ease for model implementation, the mathematical definitions for them are presented in section among with a description of their behavior. The analysis and comparison between the models are taken in account with the requirements mentioned in chapter 2 for the qualification of usefulness of a transistor model in circuit simulation. It is important to take in account that organic model construction is based in experimental data, so, simple models must be used to satisfy this matter. Only DC models are took in consideration here, dynamic models are discussed in chapter 4.

4.1.1 Shichman-Hodges Model (Level-1 Model)

The first model to be presented, and the most used transistor model in SPICE simulations, is the Shichman-Hodges Model also known as the Level-1 Model [20]. Regarding the fact that the observed I-V characteristics of OFET devices present similarity to the MOSFET I-V characteristics, the first approach to be made should be the using the Level 1 model for entering in the solution proposed in chapter 3. By approaching the transistor simulation response to the experimental data, the differences of the OFET responses regarding the transistor experimental data can express the major differences between the behavior of each device.

In figure 4.1, the output characteristics of an OFET model which take in consideration a Level-1 model are presented. The behavior regions for this model are divided in three regions: cutoff region, linear and saturation. The equations are for a n-type transistor, but the resulting equations are also applicable for p-type transistors also.

As can be observed in figure 4.1-b, the device is in the cutoff region when the V_{GS} voltage is lower than threshold voltage V_T. In this operation mode, there is no current passing in the drain. As V_{GS}

voltage increases, the device enters in linear operation mode, the current passing in the drain assume a square-law dependence on V_{DS}. As V_{GS} voltage increases, the device enters in saturation mode. In this mode the current in the drain is proportional to the drain-source voltage.

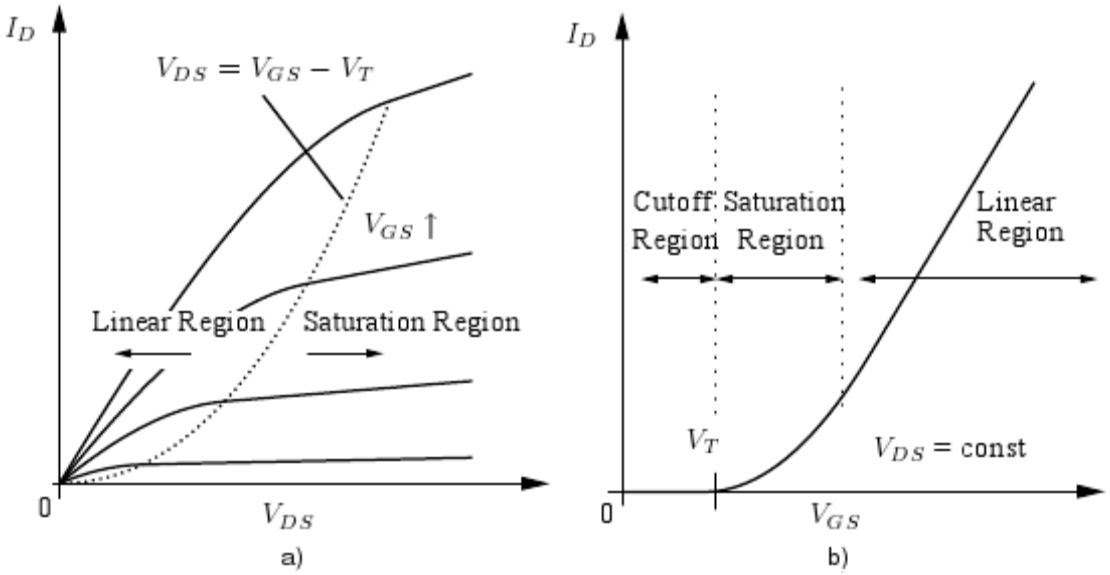

Fig. 4.1 - Output characteristics for an OFET Level-1 model

The equations 4.1, 4.2 and 4.3 describe the behavior of the transistor in the different operation modes for the Level-1 model.

1. Cutoff region:

$$I_D = 0, \quad V_{GS} < V_T \tag{4.1}$$

2. Linear region:

$$I_D = \mu C_{is} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} (1 + \lambda V_{DS}), \quad 0 < V_{DS} < V_{GS} - V_T \tag{4.2}$$

3. Saturation region:

$$I_D = \frac{1}{2} \mu C_{is} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}), \quad 0 < V_{GS} - V_T < V_{DS} \tag{4.3}$$

Where,

- μ – is the charge-carrier mobility;

- C_{is} – is the intrinsic capacitance of the transistor device;
- W – is the channel width;
- L – is the channel length;
- λ – is the channel length modulation parameter;
- V_T – the threshold voltage of the transistor device.

With easy equation manipulation the process conductance parameters is introduced, which will help in model parameter fitting. In equation 4.4 the process conductance in this model is displayed.

$$K_P = \mu C_{is} \tag{4.4}$$

The device conductance parameter β further extends K_P by taking into account the channel geometry of the transistor. In equation 4.5, this is defined.

$$\beta = K_P \frac{W}{L} = \mu C_{is} \frac{W}{L} \tag{4.5}$$

As the process conductance parameter K_P reflects the driving capabilities of the transistor device, the threshold voltage V_T on the other hand establishes how much gate-source voltage is needed to induce charge carriers in the transistor channel.

4.1.2 Amorphous TFT Model

In [15] a model is proposed for simulation of the F8T2 devices, this model is used for a-silicon TFT devices which demonstrated a similar behavior to the OFETs. The current in the drain is given by using the equation 4.6.

$$I_D = I_{leakage} + I_{ab} \tag{4.6}$$

Where,

- $I_{leakage}$ – is the intrinsic conductivity of the organic semiconductor current contribution;
- I_{ab} – is the accumulation of carriers current contribution.

As organic semiconductors work in accumulation of carriers mode, it was observed a leakage current due the intrinsic conductivity of the organic semiconductor. The model is based on the assumption that above threshold, most of the charge carriers induced in the channel are trapped and only a small fraction contributes to charge transport. A V_{SG} dependent mobility reflects this property.

In equation 4.7, the carrier equilibrium approach is given.

$$\mu = \mu_0 \left(\frac{V_{SG} - V_T}{V_{AA}} \right)^{\gamma} \tag{4.7}$$

Where,

- γ – the power law mobility parameter;
- V_{AA} – the characteristic voltage for field effect mobility [V];
- μ_0 – is the charge-carrier mobility of the organic semiconductor [cm^2/V].

It's important to notify that In this model γ, V_{AA} and μ_0 are fitting parameters which are obtained from experimental data and not physical values which are deducted from the TFT device.

4.1.3 Brescia VRH Model

A more complex DC model can be built for more precision in simulation of organic TFT devices, which are those studied in this work. In equations 4.8, 4.9 and 4.10, the model is described for a n-type device. This model was deducted and proposed in a scientific paper by E. Calvetti and others[5].

1. In the linear region:

$$i_D = \beta \frac{W}{L} \frac{T}{2T_0} \left[(V_{SG} - V_{FB})^{2\frac{T}{T_0}} - (V_{SG} - V_{SD} - V_{FB})^{2\frac{T}{T_0}} \right], \quad V_{SG} - V_{FB} > V_{SD} \tag{4.8}$$

2. In the saturation region:

$$I_D = \beta \frac{W}{L} \frac{T}{2T_0} (V_{SG} - V_{FB})^{2\frac{T}{T_0}}, \quad V_{SG} - V_{FB} \leq V_{SD} \tag{4.9}$$

3. And the expression of β is given by:

$$\beta = \frac{\sigma_0}{q} \frac{T}{2T_0 - T} \frac{C_{is}^{\frac{2T_0}{T-1}}}{(2K_B T_0 \epsilon_0 \epsilon_s)^{\frac{2T_0}{T-1}}} \left(\frac{(T_0/T)^4 \sin(\pi T_0/T)}{(2\alpha)^3 B_C} \right)^{\frac{T_0}{T}} \tag{4.10}$$

Where,

- T_0 – characteristic temperature of the semiconductor material [K];

- T – lattice temperature of the semiconductor material [K];
- C_{in} – insulator capacitance [F/μm^2];
- B_c – critical number for the percolation onset → approx. ≈ 2.8;
- K_B – Boltzmann constant [J/K] ≈ 1.3806504 x 10^{-24} J/K;
- ε0 – vacuum permittivity [F/m] ≈ 8.8541878176 x 10^{-12} F/m;
- ε_s – relative dielectric constant;
- σ_0 – electrical conductivity of the semiconductor material [S/m];
- α – effective wave functions overlap parameter [Aº - argon];
- q – electron charge [C] ≈ 1.6021892 x 10^{-19} C;
- W – the semiconductor channel width;
- L – the semiconductor channel length;
- V_{FB} – the flat-band voltage used for denoting the onset of accumulation [V].

This is simplified version of the complete model presented in [5], making it appliance useful in simulators like SPICE. It's important to have in account that β is obtained in curve fitting, and it was observed in typical operating conditions that T_0 parameter is negligible, making the fitting of this model possible.

4.1.4 Meijer Model

Meijer and other authors [8], proposed a model to describe ambipolar organic field effect transistor devices. In this work for easy reference, the analytic model presented in this section will be referred as the Meijer model. The model can be described next :

$$I_{SD} = k_p \frac{W}{L}\left(\llbracket V_{SG} - Vt \rrbracket^{\frac{2T_0}{T}} - \llbracket V_{SG} - V_T - V_{SD} \rrbracket^{\frac{2T_0}{T}}\right) \quad where \quad \llbracket x \rrbracket = \frac{1}{2}x + \frac{1}{2}|x| \tag{4.11}$$

Where:

- K_p – is the semiconductor process transconductance parameter [S];
- W – Channel width [m];
- L – Channel length [m];
- Vt – Threshold voltage [V];

- T – lattice temperature of the semiconductor material [K];
- T_0 – characteristic temperature of the semiconductor material [K];

This model was deducted to model ambipolar transistors, which allows construction of complementary logic (ambipolar are introduced in chapter 1). For modeling the analyzed p-type organic technology, this model showed the best results to describe the triode region. With ease, this model can manage to define the behavior in triode region in the model implementation.

4.2 Static Model Implementation and Simulation

After gathering the desired models in bibliography, the next step is to implement the desired model in a simulation technology and extract proceed to the equations treatment for parameter extraction. According to the equations and depending on which simulation technology is desired to be implemented, the separation and manipulation of the equations is to be made. In the next sections according to the simulation technology, the implementation of the devices is demonstrated.

4.2.1 Model Implementation of the Level-1 model

In this section the implementation of the model equations, as SPICE is a circuit description environment, is made by circuit and first we shall begin with the circuit description of Level-1 model. In figure 4.2, the circuit for model implementation in SPICE environments is demonstrated.

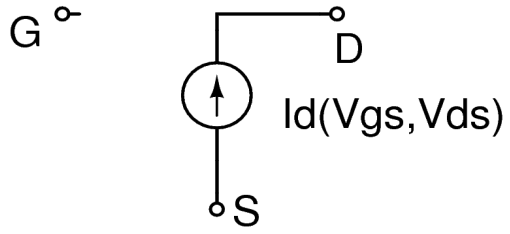

Fig. 4.2 - Level-1 Model equivalent circuit for SPICE

Although the implementation appears to be simple, the equations between linear and saturation operation modes make the model implementation hard in circuit description calling for the need of behavioral extensions. HSPICE simulator which is used in this work for the reproduction of the organic devices offers this kind of implementation, making the circuit description possible. The problem is that the circuit description results in a complex listing. In figure 4.3, the idea behind the model possibility in circuit representation is consisting in separating the operational modes with different sources.

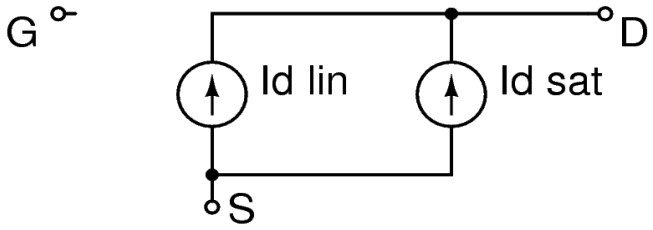

Fig. 4.3 - Division of the operation mode equations in circuit description

Where Id lin is the source activated under linear operation mode (in the others is 0) and Id sat is activated in saturation mode. At a determinate operation mode, only one source is active making the circuit being able to reproduce the model equations.

4.2.2 Model Implementation of the Amorphous TFT model

It was found that Level-1 model fits poorly with the organic devices, making the SPICE implementation of the Amorphous TFT model a need. In figure 4.4, the circuit implementation of the amorphous TFT model as referenced in [15] is presented.

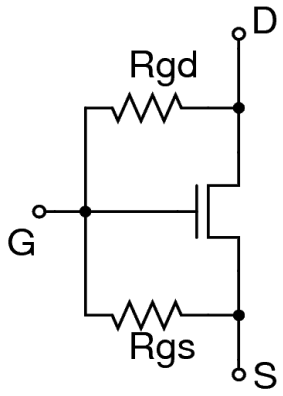

Fig. 4.4 - Amorphous TFT model circuit implementation in SPICE

The advantage of this model is the inclusion of the drain-gate and drain-source resistances, this has the advantage of reproduce the contact resistances influenced by the parasitic resistance R_I persisting in the device. The equation 4.12, gives the expression of R_{GS} and R_{GD}.

$$R_{GS}=R_{GD}=\frac{R_I}{W.(F+L)} \tag{4.12}$$

Where,

- RI – is the parasitic resistance of the device
- W – the channel width
- L – the channel length
- F – the finger width of the contacts

The model equations to be implemented in the circuit, are based in the equations 4.6 and 4.7, and the current in the drain is given by equations 4.13 to 4.19 as referenced in [15].

$$I_{ab}=g_{ch}V_{dse}(1+\lambda.V_{SD}) \tag{4.13}$$

$$I_{leakage}=SIGMA0.V_{SD} \tag{4.14}$$

$$g_{ch}=\frac{g_{chi}}{1+g_{chi}(R_S+R_D)} \tag{4.15}$$

$$g_{chi}=\mu C_i\frac{W}{L} \tag{4.16}$$

$$V_{gte}=\frac{V_{MIN}}{2}\left[1+\frac{V_{SG}-V_T}{V_{MIN}}+\sqrt{(DELTA^2+\left(\frac{V_{SG}-V_T}{V_{MIN}}-1\right)^2)}\right] \tag{4.17}$$

$$V_{dse}=\frac{V_{SD}}{\left[1+(V_{SD}/V_{SATE})^M\right]^{1/M}} \tag{4.18}$$

$$V_{SATE}=ALPHASAT.V_{gte} \tag{4.19}$$

Where,

- μ – semiconductor mobility [cm^2/Vs];
- ALPHASAT – saturation modulation parameter;
- λ – output conductance parameter [V^{-1}];
- M – knee shape parameter;
- C_i – device internal capacitance [F/m^2];
- W – channel width [m];

- L – channel length [m];
- SIGMA0 – Minimum leakage current parameter [A].

Fortunately, there is a SPICE library with amorphous TFT models. This makes the model implementation easy, and makes the concerning to go directly to the model parameter extraction. The model used for organic parameter fitting is the TFT-model AFET 15 which in [15] demonstrated good results in simulation for F8T2 devices.

4.2.3 Model Implementation for Brescia VRH Model

Due the number of parameters in the Brescia VHR Model, the SPICE simulation technology implementation philosophy makes it difficult to implement a circuit representation. Due this issue, a demand for an Description Behavior technology conduct the model implementation to VHDL-AMS. As VHDL-AMS implementation philosophy is through the use of description behavior, in figure 4.5 the flowchart of the VRH model implementation in VHDL-AMS is presented.

As observed in figure 4.5, the fitted values and the VSD and VSG voltage values pass through various conditions for calculating the simulated drain current in the device. This eases the implementation of the device, extending the range of possibilities and use of more complex models for simulation.

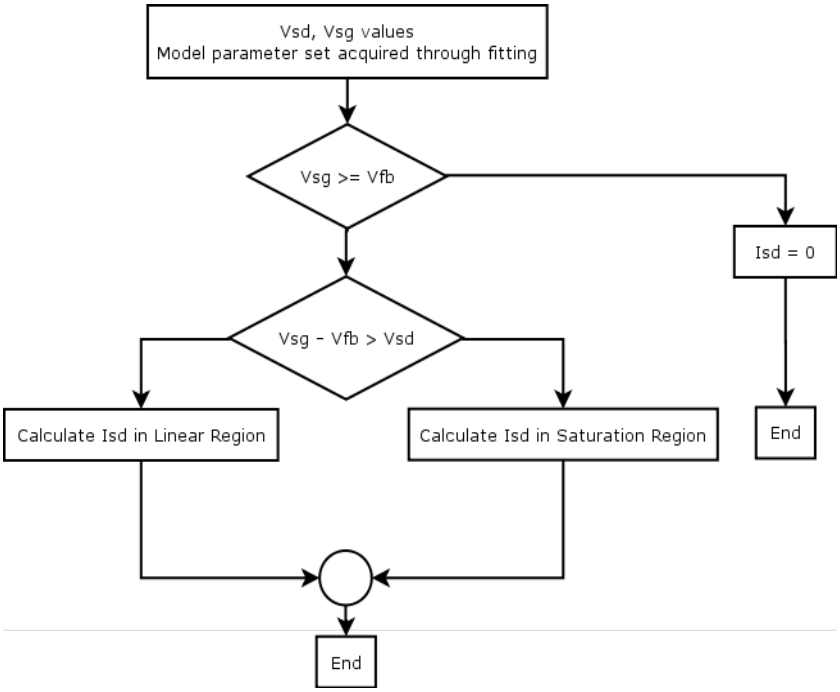

Fig. 4.5 - Brescia VRH Model implementation flowchart in VHDL-AMS

This concludes the implementation of the devices in the simulation technologies which were took in consideration in this work. After having the model implemented, the fitted parameter data and the simulation reproduction of the models presented in section 4.1 are compared and classified through the MQC standard.

4.2.4 Meijer model implementation

It was found in this work Meijer has the best results in describing the triode region. Due this issue, Meijer mode can be used among with the Amorphous TFT model for describing the behavior of the measured F8T2 organic TFTs. The circuit to be implemented consists in the same as figure 4.4. This can be accomplished with establishing the equation in the triode mode, using the boundary conditions already known for these devices.

4.3 Fitting the presented models with the experimental data

In chapter 2, three models for describing plastic transistors were described. The application described in the section above, will use these three models and show the curve fitting of each one. A user can chose which model best fits the experimental data, and obtain the physical parameters of the measured device. After this a SPICE or VHDL-AMS model can be build, this will be discussed in the next section. In this section the results of applying each model can be viewed. The device that is used for demonstration is a F8T2-based device measured in air after a curing of the film at 90 ºC for 15 minutes under vacuum.

The data points extracted from the device can be viewed in figure 4.6. At first glance, we can observe that Vt is between 10 V and 20 V. After applying non linear optimization technique to the experimental data points, V_T gives approximately 15 V. So the split is made and data from V_{SG} between 0 to 10 V is separated from data between 20 V to 40 V.

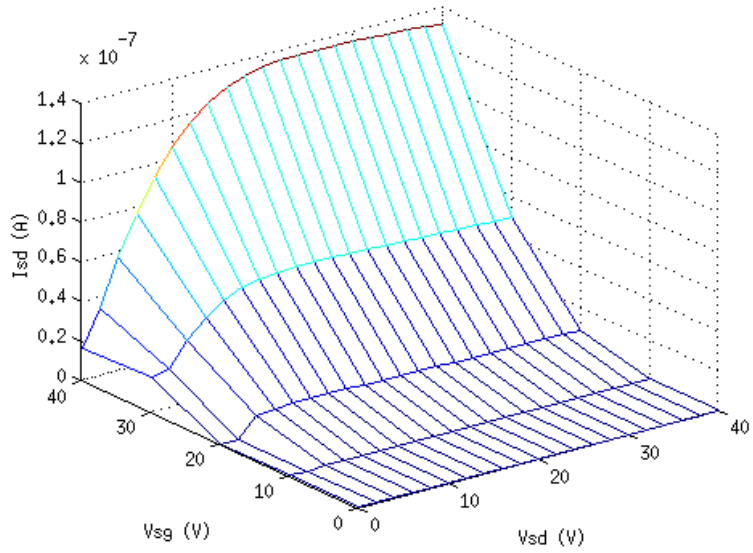

Fig. 4.6 - F8T2-based device experimental data

4.3.1 Level-1 model fitting

First, the Level-1 model which equations are indicated in section 4.1.1 is used. Curve fitting can be observed. Saturation is separated from linear region and the models are compared. The fitting can be observed in figure 4.7. The asterisk dots are the experimental data, the dot points are the data reproduced by the Level-1 Model with the best coefficients calculated after the procedure of non linear optimization is concluded. The linear region is showed in red, and the saturation region in green.

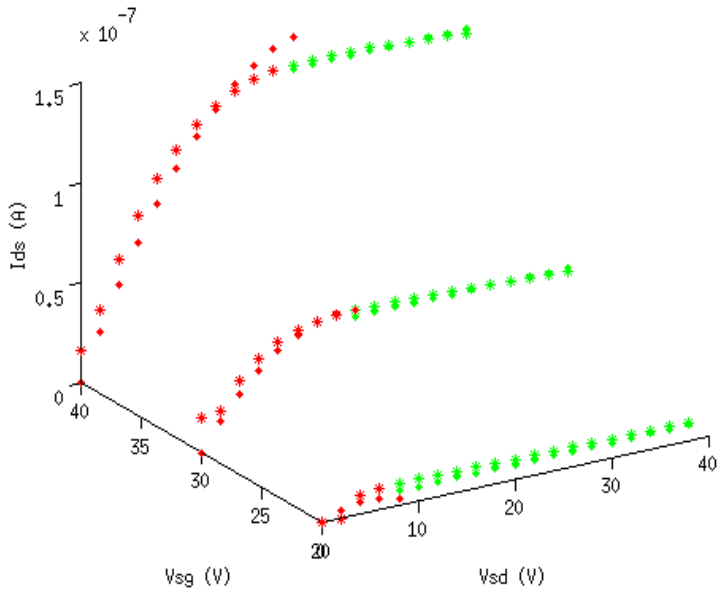

Fig. 4.7 - Experimental Data Vs. Level-1 Model

As observed in figure 3.4.1, saturation region is well defined by Level-1 model, but the linear region demonstrated a bad representation, specially when V_{SG} = 20 V. Although, when V_{SG} = 40 V, this model is not able to reproduces the $I_{SD}(V_{SG})$ curves in the linear region also.

In [11], the average parameters found using this model conducted to parameters with no physical meaning, concluding that this model cannot describe OFET behavior.

4.3.2 Amorphous TFT model fitting

As presented in section 4.1.2 the amorphous TFT model is defiantly a better approach to an organic device. Now, there's a leakage current and a induced current. The data confrontation is showed in the figure 4.8. Like in figure 4.7, asterisks describe experimental data and dots describe the approach of the model simulation using the best coefficients calculated after the non linear optimization process. But for this to happen, simplification of the model form presented in section 4.2.2 is used.

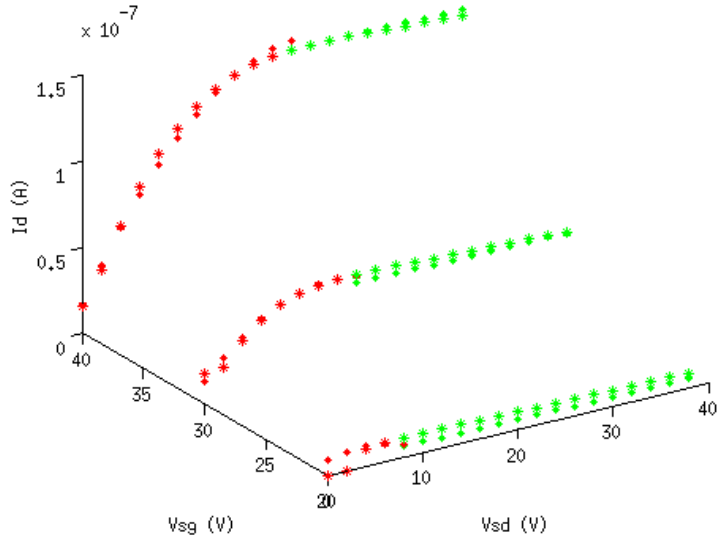

Fig. 4.8 - Experimental Data Vs. Amorphous TFT model

In figure 4.8, is observed a better approach in the linear region for V_{SG} = 40 V. This model presents better capabilities for describing the F8T2 organic devices measured. Using the equations of the model implementation of the amorphous TFT model, a good curve fitting note between the experimental data and the reproduced model.

The parameter values obtained with the application of the solution described in chapter 3, result in the following set described in table 4.1.

Tab. 4.1 - Fitted parameters for Amorphous TFT model

Parameter	Value	Description
μ	1.57 x 10^{-3} cm^2/V	Semiconductor Mobility
ALPHASAT	0.49	Saturation Modulation parameter
λ	- 0.0038 V^{-1}	Output conductance parameter
M	2.78	Knee shape parameter
V_T	12.4 V	Threshold voltage
SIGMA0	1.19 x 10^{-3} A	Minimum leakage current parameter

4.3.3 Brescia VRH model fitting

The best results were obtained using Brescia VHR model which was presented in section 4.1.3, in figure 4.9 the results can be observed.

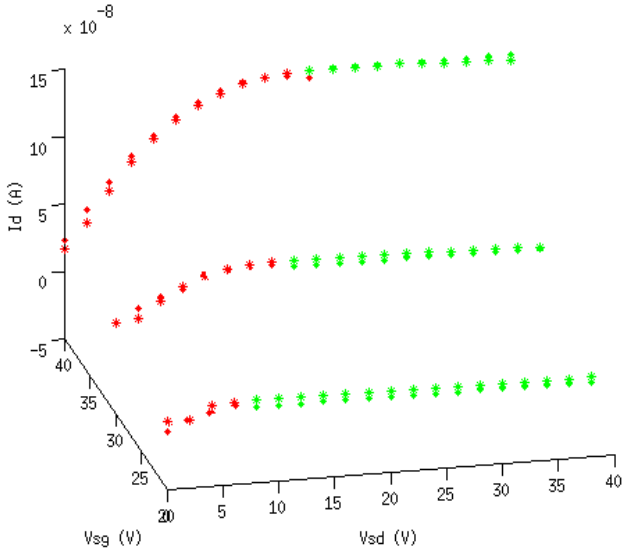

Fig. 4.9 - Experimental Data Vs. Brescia VRH model

This model demonstrates good accuracy in describing the experimental data. Although as discussed in section 4.2.3, the implementation in SPICE of this model is difficult and has to be made using VHDL-AMS as an alternative. Being the number of parameters in this model considerable, the capacity for the proposed solution to extract all the parameters is limited.

The parameter values obtained with the application of the solution described in chapter 3, result in the following set described in table 4.2.The other parameters cannot be deducted, or if the value is already known.

Tab. 4.2- Fitted model parameters for Brescia VRH Model

Parameter	Value	Description
C_{in}	8.2×10^{-6} F/m^2	Insulator capacitance
μ	1.53×10^{-3} cm^2/V	Semiconductor mobility
V_{FB}	2.3 V	Threshold voltage

4.4 Qualifying the Models presented

In this section the qualification of the models according to the MQC [20] which is described in chapter 2.

Due to the multitude of materials and processing routes, there is no uniform shape of the current/voltage characteristics of OFET devices. Therefore, the accuracy of the Level-1 approach has been rated from bad to medium. It can adequately reproduce OFET types where the mobility only weakly depends on the gate-source voltage. Other modeling approaches are better suited for devices with variable mobility for example. Modeling of capacitances is not part of the basic equations. It should be noted, however, that Level-1 implementations in SPICE simulators include nonlinear modeling of capacitances which are similar to OFET-related capacitance values expected from parameter extraction process.

As the Level-1 model is based on a physical background (gradual channel approximation) and only few parameters are necessary in the equations, compactness of the model has been rated as good. Numerous approaches can be used for deriving these parameters. Therefore, parameter extraction has also been rated as good. Stress effects are not included in the model. Level-1 model MQC is presented in table 4.3.

Tab. 4.3 - MQC for Level-1 model

Requirement	Rating
Accuracy	Bad to medium
Capacitance Modeling	Not included
Compactness	Good
Parameter Extraction	Good

Regarding the the accuracy of the model with respect to F8T2 transistors is good as demonstrated in section 4.3.2. Modeling of capacitances is not included in the model. The model needs only six technology parameters ($R_C = R_S = R_D$,η, V_T , μ_0 , γ, VAA), which increases its compactness (rating good). Contact effects influence the shape of current-voltage characteristics in a non-linear way. Therefore, parameter extraction schemes which rely on curve fiting are difficult to employ unless linearization procedures are taken in account for parameter extraction. This property complicates parameter extraction (rating bad). In table 4.4 the MQC for this model is presented.

Tab. 4.4 - MQC for Amorphous TFT model

Requirement	Rating
Accuracy	Good
Capacitance Modeling	Not included
Compactness	Good
Parameter Extraction	Bad

Finally, for Brescia VHR model accuracy has been rated as good according to the results observed in section 4.3.3. Modeling of capacitances is included and is discussed in chapter 5. The physical models work with a limited set of parameters, which improves their compactness and leads to a rating of good in this category. Parameter extraction has been rated as medium because it is more difficult than in the case of Level-1 modeling but easier, since the direct behavior of current does not depend on the extraction of all the parameters. Table 4.5 gives the MQC for Brescia VRH model.

Tab. 4.5 - MQC for Brescia VRH Model

Requirement	Rating
Accuracy	Good
Capacitance Modeling	Good
Compactness	Good
Parameter Extraction	Medium

As the work objectives demanded dynamic capabilities for OFET devices, but having in mind a model which could be able to represent the experimental acquired technology through parameter extraction techniques, the model which best simulates is the Brescia VHR model.

4.4 Chapter Overview

In this chapter, the solution architecture proposed in chapter 3 was run against some selected models in static mode which could be able to represent the select technology. The results are good when using the model proposed in section 4.1.3 against the experimental results in simulation. In the next chapter, the extension of this model for dynamic model creation is presented.

5. Organic Dynamic Transistor Models

In this chapter, organic dynamic models are presented. These models consist in the dynamic extensions of the models exposed in chapter 4. In the next sections, the theory for transient/AC model representation is presented and the consequent extensions for each model presented in the previous chapter as a result of the consulted bibliography. Also, the implementation and simulation of the models exposed are presented among with the results, making this chapter ends with the comparison of the simulation results of the presented models.

5.1 Organic Dynamic Model Theory

Transient/AC response regarding transistor simulation models, are influenced by the physical structure of the device (the architecture type), physical properties of the materials which compose the device and the voltage between source-drain (V_{SD}) and source-gate (V_{SG}). Having all these factors of influence in the transient/AC response of a transistor device, the resulting equations of the application of the deduction processes makes the equations difficult for appliance in extraction techniques and forcing the use linearization techniques.

The way in which the transient/AC response is influenced is generally modeled through the definition of capacitances. These capacitances are the isolated members of the mathematical expressions which define the behavior of the transistor through time. In the next subsections, each model's dynamic extensions and capacities calculation are presented according with the gathered bibliography from the static models presented in chapter 4.

5.1.1 Amorphous TFT model with dynamic capabilities

According to the model presented in section 4.2.2 and described also in [15], a good approximation for a transient model for amorphous TFT, had demonstrated acceptable results with the F8T2 devices measured. In figure 5.1, this model is presented through the circuit diagram describing it and the mathematical expressions which defines the model behavior.

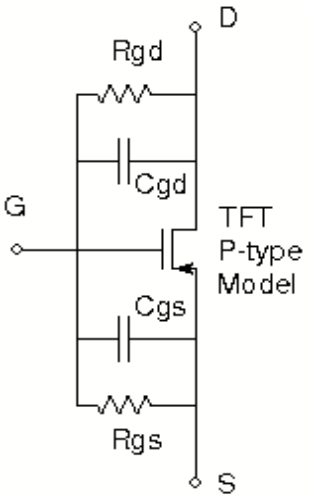

Fig. 5.1 - Equivalent Transient Amorphous TFT Circuit Model

As can be observed in figure 5.1, the model manages the modulation of the transient response of the Amorphous TFT Model through the use of equivalent capacitance-resistor pair. This manages to modulate the V_{SG} and V_{SD} influence in the transient response of the device. Having in consideration the non-organic insulator, this approach results in the capability that this model has in describing the parasitic resistances and capacitances observed in this devices as stated in [15]. Other great advantage of this model extension is the capacity of talking the leakage factor observed in the F8T2 OTFT devices.

The mathematical expressions which describes these models are given by equations 5.1, 5.2 and 5.3, which are given next.

$$C_{GS} = C_{GD} = C_1 . W . F \tag{5.1}$$

$$R_{GS} = R_{GD} = \frac{R_1}{W.(F+L)} \tag{5.2}$$

$$SIGMA0 = sigma_1 \frac{W}{L} \tag{5.3}$$

Where,

- CGS is the gate-source parasitic capacitance [F];
- CGD is the gate-drain parasitic capacitance [F];

- C1 is the intrinsic capacitance of the TFT [F/m2];
- W is the channel width [m];
- F is the channel length [m];
- L is the channel finger width [m];
- RGS is the gate-source parasitic resistance [Ω];
- RGD is the gate-drain parasitic resistance [Ω];
- R1 is the intrinsic resistance of the insulator material [Ω.m2];
- SIGMA0 is the leakage current of the device [A];
- sigma1 is the leakage current density of the device [A];

Analyzing the equations for the transient extensions of the Amorphous TFT model, implementation is possible using both SPICE and VHDL-AMS technology resulting in a good model to pick for a organic TFT modulation due model simplicity. SIGMA0 is for adding parameters correction to the static equations for this model presented in chapter 4.

5.1.2 Brescia VRH Model

For Brescia VRH Model, the dynamic model is derived from the static model equations using the charge oriented approach [5]. The charge orientated approach consists in having the static model equations, and through the charge conservation law, define the charge variation in the transistor device. In [5], after calculating the total charge contribution of each terminal of the organic device, equation 5.4 is used for establishing the relationship between the current passing on two terminals of the device and the voltage values established in the device.

$$\frac{dQ_i}{dt}=\sum_j \frac{\partial Q_i}{\partial V_j}\frac{dV_j}{dt}=\sum_j C_{ij}\frac{dV_j}{dt} \quad i,j=S,D,G \tag{5.4}$$

Using this approach, conducted the transient model to the circuit representation stated in figure 5.2. This circuit consists in the small signal model for the Brescia VRH model.

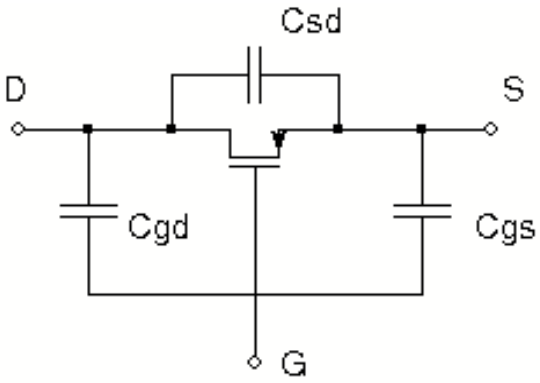

Fig. 5.2 - Brescia VRH Small-Signal Circuit Model

As can be seen in figure 5.2, the circuit besides the capacitances C_{GD} and C_{GS}, that are also taken in attention in the Amorphous TFT model, this model also includes C_{SD} capacitance. The equations deducted from the Brescia VRH static model are of extensive complexity as can be seen in this section. The expressions for C_{GS}, C_{GD} and C_{SD} capacitances are given next in equations 5.5 to 5.16.

$$C_{GS}=\begin{cases} WLC_{ins}\left(\dfrac{num_{GS1}}{den_{lin}^{2}}+\dfrac{num_{GS2}}{den_{lin}}\right), & if\ V_{GS}-V_{DS}\geq V_{FB} \\ WLC_{ins}\left(\dfrac{num_{GS2}}{den_{sat}}+\dfrac{num_{GS3}}{den_{sat}^{2}}\right), & if\ V_{GS}-V_{DS}<V_{FB} \end{cases} \tag{5.5}$$

$$C_{SD}=WLC_{ins}\left(-\frac{num_{SD1}}{den_{lin}^{2}}+\frac{num_{SD3}}{den_{lin}^{3}}\right) \tag{5.6}$$

$$C_{GD}=WLC_{ins}\left(-\frac{num_{GD1}}{den_{lin}^{2}}-\frac{num_{GD2}}{den_{lin}}\right) \tag{5.7}$$

$$\begin{aligned} num_{GS1}=&\left[-\frac{2\mathrm{K}_{B}T_{0}}{q}(V_{GS}-V_{FB})^{\frac{2\mathrm{T}_{0}}{T}-2}-(V_{GS}-V_{FB})^{\frac{2\mathrm{T}_{0}}{T}-1}\right] \\ &\cdot\left[\frac{K_{B}T}{q}((V_{GS}-V_{FB})^{\frac{2\mathrm{T}_{0}}{T}-2}-(V_{GD}-V_{FB})^{\frac{2\mathrm{T}_{0}}{T}-1}) \right. \\ &\left.+\frac{T}{T+2\mathrm{T}_{0}}((V_{GS}-V_{FB})^{\frac{2\mathrm{T}_{0}}{T}+1}-(V_{GD}-V_{FB})^{\frac{2\mathrm{T}_{0}}{T}+1})\right] \end{aligned} \tag{5.8}$$

$$num_{GS2}=(V_{GS}-V_{FB})^{\frac{2T_0}{T}}+\frac{2K_BT_0}{q}(V_{GS}-V_{FB})^{\frac{2T_0}{T}-1} \tag{5.9}$$

$$\begin{aligned} num_{GS3}=&\left[-\frac{2K_BT_0}{q}(V_{GS}-V_{FB})^{\frac{2T_0}{T}-2}-(V_{GS}-V_{FB})^{\frac{2T_0}{T}-1}\right] \\ &\cdot\left[\frac{K_BT}{q}(V_{GS}-V_{FB})^{\frac{2T_0}{T}}+\frac{T}{T+2T_0}(V_{GS}-V_{FB})^{\frac{2T_0}{T}+1}\right] \end{aligned} \tag{5.10}$$

$$\begin{aligned} num_{SD1}=&\frac{T}{(T+2T_0)}(V_{GD}-V\,FB)^{\frac{4T_0}{T}}+\frac{2TK_b^2T_0}{q_2}(V_{GD}-V_{FB})^{\frac{4T_0}{T}-2} \\ &+\frac{TK_B(T+4T_0)}{q^2(T+2T_0)}\times(V_{GD}-V_{FB})^{\frac{4T_0}{T}-1}+\left(\frac{2K_BT_0}{q}(V_{GD}-V_{FB})^{\frac{2T_0}{T}-2}+(V_{GD}-V_{FB})^{\frac{2T_0}{T}-1}\right) \\ &\cdot\left(\frac{TK_B}{q}(V_{GS}-V_{FB})^{\frac{2T_0}{T}}+\frac{T}{T+2T_0}(V_{GS}-V_{FB})^{\frac{2T_0}{T}+1}\right) \end{aligned} \tag{5.11}$$

$$\begin{aligned} num_{SD3}=&2\left[\frac{2K_BT_0}{q}(V_{GD}-V_{FB})^{\frac{2T_0}{T}-2}+(V_{GD}-V_{FB})^{\frac{2T_0}{T}-1}\right] \\ &\cdot\left\{\frac{T^2K_B(T+4T_0)}{4qT_0(T+2T_0)}\left[(V_{GS}-V_{FB})^{\frac{4T_0}{T}}-(V_{GD}-V_{FB})^{\frac{4T_0}{T}}\right]\right. \\ &+\frac{2T^2K_B^2T_0}{q^2.(4T_0-T)}\times\left[(V_{GS}-V_{FB})^{\frac{4T_0}{T}-1}-(V_{GD}-V_{FB})^{\frac{4T_0}{T}-1}\right] \\ &\left.+\frac{T^2}{(T+2T_0)(T+4T_0)}\left[(V_{GS}-V_{FB})^{\frac{4T_0}{T}+1}-(V_{GD}-V_{FB})^{\frac{4T_0}{T}+1}\right]\right\} \end{aligned} \tag{5.12}$$

$$\begin{aligned} num_{GD1}=&\left[\frac{2K_BT_0}{q}(V_{GD}-V_{FB})^{\frac{2T_0}{T}-2}+(V_{GD}-V_{FB})^{\frac{2T_0}{T}-1}\right] \\ &\cdot\left[\frac{K_BT}{q}\left((V_{GS}-V_{FB})^{\frac{2T_0}{T}}-(V_{GD}-V_{FB})^{\frac{2T_0}{T}}\right)\right. \\ &\left.+\frac{T}{T+2T_0}\left((V_{GS}-V_{FB})^{\frac{2T_0}{T}+1}-(V_{GD}-V_{FB})^{\frac{2T_0}{T}+1}\right)\right] \end{aligned} \tag{5.13}$$

$$num_{GD2}=(V_{GD}-V_{FB})^{\frac{2T_0}{T}}+\frac{2K_B T_0}{q}(V_{GD}-V_{FB})^{\frac{2T_0}{T}-1} \tag{5.14}$$

$$\begin{aligned} den_{lin}=&\frac{2TK_B T_0}{q(2T_0-T)}\left[(V_{GS}-V_{FB})^{\frac{2T_0}{T}-1}-(V_{GD}-V_{FB})^{\frac{2T_0}{T}-1}\right] \\ &+\frac{T}{2T_0}\left[(V_{GS}-V_{FB})^{\frac{2T_0}{T}}-(V_{GD}-V_{FB})^{\frac{2T_0}{T}}\right] \end{aligned} \tag{5.15}$$

$$den_{sat}=\frac{T}{2T_0}(V_{GS}-V_{FB})^{\frac{2T_0}{T}}+\frac{2TK_B T_0}{q(2T_0-T)}(V_{GS}-V_{FB})^{\frac{2T_0}{T}-1} \tag{5.16}$$

Where,

- T_0 – characteristic temperature of the semiconductor material [K];
- T – lattice temperature of the semiconductor material [K];
- C_{in} – insulator capacitance [F/μm^2];
- K_B – Boltzmann constant [J/K] ≈ 1.3806504 x 10^{-24} J/K;
- q – electron charge [C] ≈ 1.6021892 x 10^{-19} C;
- W – the semiconductor channel width;
- L – the semiconductor channel length;
- V_{FB} – the flat-band voltage used for denoting the onset of accumulation [V].

Brescia VRH dynamic extensions, have the capability of representing the capacitances in detail and also take in consideration the capacitance C_{DS} which is none in the ATFT model.

5.2 Dynamic Model Implementation and Simulation

In this section, the implementation of the dynamic models presented in section 5.1 is discussed. SPCIE and VHDL simulations are discussed. The main objective on these devices is using the parameter fitting system in the proposed architecture in chapter 3 for extracting the intrinsic capacitance C_{in} parameter.

5.2.1 Model Implementation in SPICE

For using Meijer or ATFT static equations, it's possible to implement the model using SPICE or

VHDL-AMS. In SPICE, the model follows the circuit presented in figure 5.2, the capacitances are modulated and approach by linear functions based on the experimental data.

For basic simulations, regarding logic circuits using the F8T2 technology, SPICE implementation works fine. The intention in these circuits is knowing the port delay time. The intention of using these dynamic extensions, is the fact that in saturation or in no-built in channel the capacitances assume the experimental results measured using the OTTB system with an oscilloscope. Although, the only model which is capable of being implemented in SPICE is the ATFT, Brescia VRH was found of several difficulty to implement using this technology.

5.2.2 Model Implementation in VHDL-AMS

In VHDL-AMS, the Brescia VRH dynamic extensions can be implemented. This implementation is described in figure 5.3.

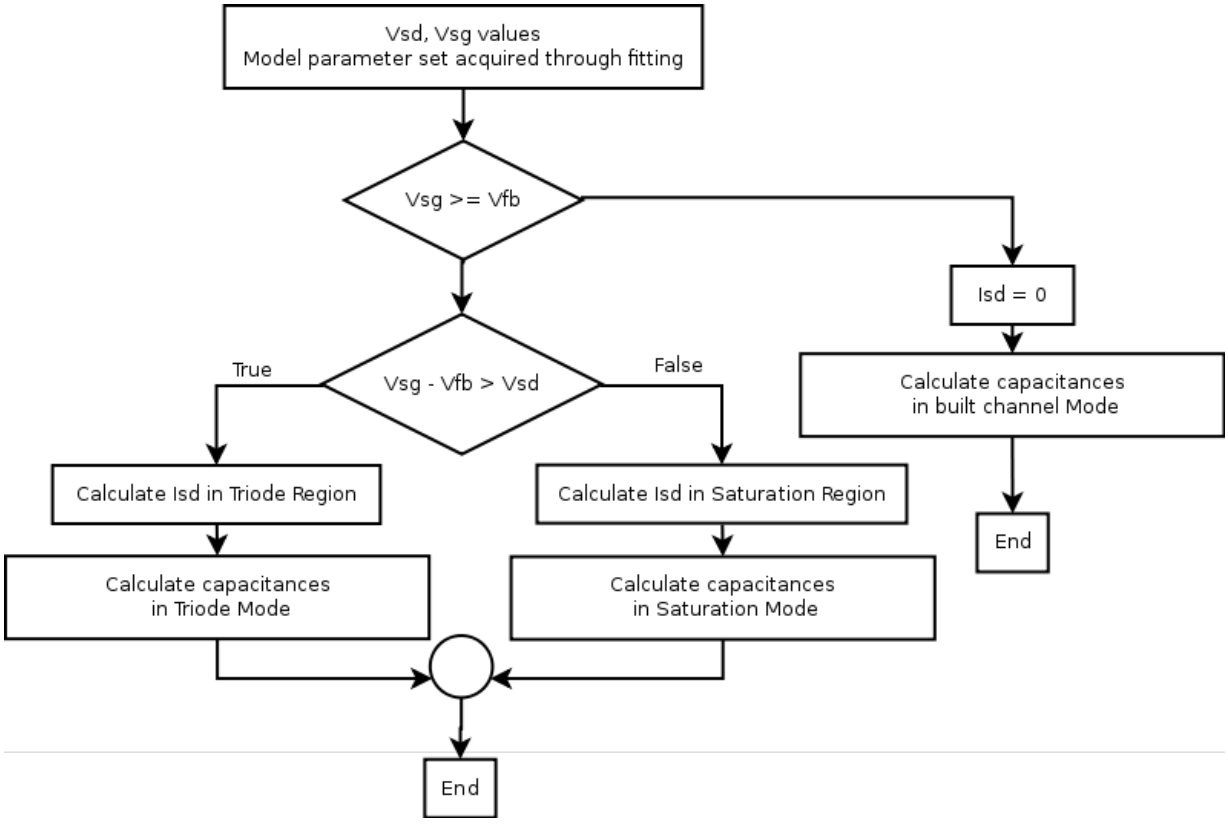

Fig. 5.3 - Implementation of the capacitances in VHDL-AMS using the Brescia VRH model

After implementing the desired model, the parameter fitting of the experimental measured capacitances must be performed for obtaining C_{in} and checking the results.

5.4 Fitting Results using the dynamic organic models

In this section, the fitting of the capacitance measuring using the OTTB system with an oscilloscope is fitted with the capacitance expressions of the given models. In figure 5.4 the capacitance of a F8T2 transistor is measured and surface fitting is performed using the ATFT model.

As can be seen in figure 5.4, the capacitances are big for an organic transistor, although it's importance to notice that the physical dimensions of this transistor are big also, making the calculations the Cin should be 7.1×10^{-6} F/m^2. And this model fitting gave 6.8×10^{-6} F/m^2 which is acceptable.

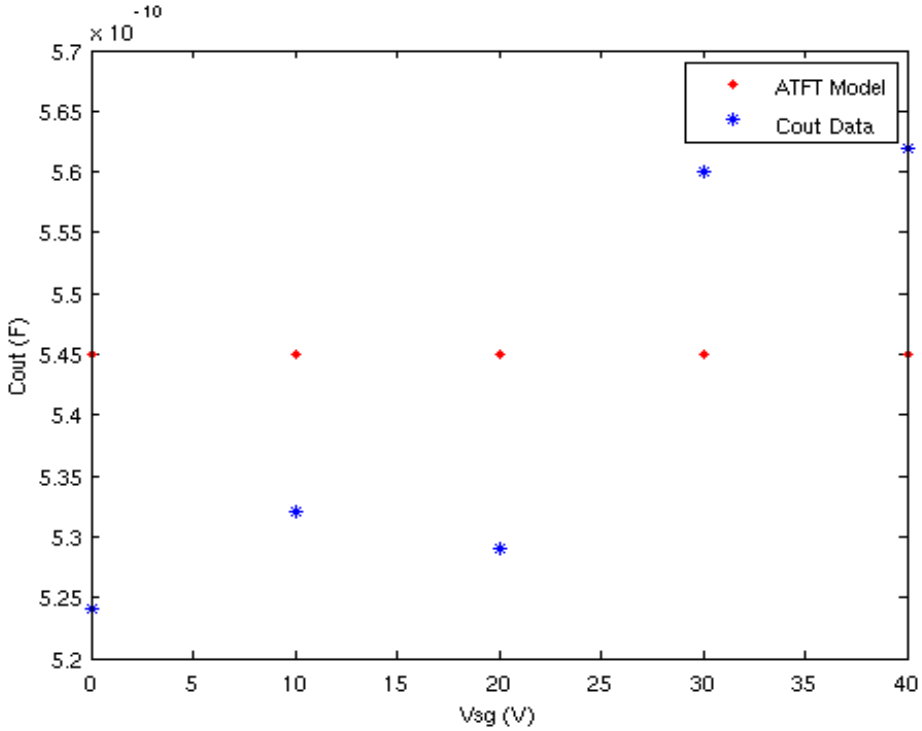

Fig. 5.4 - Output measured capacitance fitting using the ATFT model when Vsd = 40 V

For the Brescia VRH capacitances the fitting was found of several difficulty, making the approach of finding the capacities of several difficulty when C_{DS} exists. In [5], the capacitance can be ignored, having presented some significant value when in saturation. Regarding this, using the model equations of the ATFT model can be used for having a average approach of the capacitances values.

In table 5.1, the comparison between the models is made.

Tab. 5.1 - Comparison between ATFT and Brescia VRH Model

Property	ATFT Capacitance Model	Brescia VRH Model
Capacitance Expressions	Simple	Complex
Fitting Results	Medium	Couldn't reach using the transient method
Accuracy to the supposed results	Medium	Couldn't figure out
Capacity of describing real capacitance values	Poor	Good

5.3 Chapter Overview

In this chapter, it was possible to found models which were able to represent the devices capacitances. Having this established, a model which capable of represent the capacitances becomes a possibility and circuit implementation and comparison with experimental results is the next step. In chapter 6, the F8T2 inverter is constructed and analyzed. The experimental results are going to be compared with the simulation of the circuit using the models presented in this chapter.

6. Organic Transistor circuit simulation

In this chapter, simple circuits built with organic circuitry namely F8T2 technology are going to be presented and studied. Experimental implementations of these circuits are also applied for comparison of the models presented in chapter 4 and their dynamic extensions described in chapter 5. Experimental data acquisition and experimental-simulation comparison is performed using the solution architecture presented in chapter 3. The main propose in this chapter is to present the study realized around the organic inverter circuit using the built F8T2 devices.

6.1 Organic Circuits and Digital Electronics appliance

The attempt of making basic logic using organic technology is the main objective in this work, urging the need of establishing organic circuits for basic circuit cells. The circuits already originating average results in the F8T2 technology are the inverter circuit cell and the ring oscillator, which were already. Some organic inverters were demonstrated in [5], [8] and [15]. In [15], an inverter circuit using F8T2 printed electronics was established and measured experimentally among with good simulation results, which matches our analyzed technology. In this section, this circuit is analyzed for characteristics prediction and behavior study, using our built technology in laboratory and based in the models presented in chapter 4 and 5.

6.1.1 The F8T2 Organic Inverter

The most basic logic cell consists in the inverter circuit, which allows a signal to be inverted as the name intends to express. The inverter and has it's major appliance in digital electronics, for constructing inversion logic and when combined with other port types, to reproduce other logic ports. There's also the ability to create memory cells using inverters, although the current losses observed in the measured devices which can be consulted in the Annex I, demonstrate this porpose a though task. In this work, an inverter was managed to being built using F8T2 devices and following the information stated in [15].

The F8T2 organic inverter circuit is expressed in figure 6.1, as stated, it consists in the combination of two F8T2 p-type organic transistors. In equations 6.1 and 6.2, the circuit's characteristic equations are exposed. This type of equations refers to static analysis, discarding the time factor. In an early stage the first approach is to analyze the static properties of the circuit. The equations, are generic for both Amorphous TFT Model and Brescia VRH Model, since they only regard the common properties observed in the transistor organic devices.

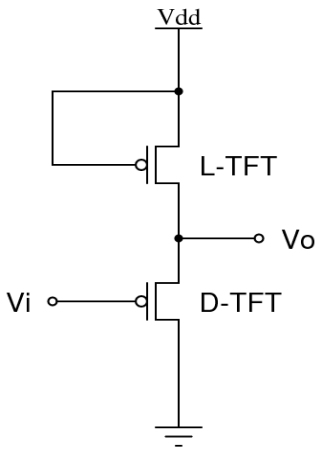

Fig. 6.1 - F8T2 Organic Inverter Cell

$$I_{SD-L} = I_{SD-D} \tag{6.1}$$

$$\begin{aligned} L-TFT &: V_{SG-L} - V_{T-L} \le V_{SD-L} \Rightarrow V_o - V_{dd} - V_{T-L} \le V_o - V_{dd} \quad SAT \\ D-TFT &: \begin{cases} V_{SG-D} - V_{T-D} > V_{SD-D} \Rightarrow -V_i - V_{T-D} > -V_o \quad TRIODE \\ V_{SG-D} - V_{T-D} \le V_{SD-D} \Rightarrow -V_i - V_{T-D} \le -V_{OUT} \quad SAT \end{cases} \end{aligned} \tag{6.2}$$

Where,

- I_{SD-L} – is the current passing in the L-TFT channel [A];
- I_{SD-D} – is the current passing in the D-TFT channel [A];
- V_{SG-L} – is the voltage between source and gate of the L-TFT device [V];
- V_{SD-L} – is the voltage between source and drain of the L-TFT device [V];
- V_{SG-D} – is the voltage between source and gate of the L-TFT device [V];
- V_{SD-D} – is the voltage between source and gate of the L-TFT device [V];
- V_{T-L} – is the threshold voltage of the L-TFT device [V];
- V_{T-D} – is the threshold voltage of the L-TFT device [V].

As the transistors used are p-type transistors, the current flow goes from GND node to Vdd node. This type of inverter is known as active load inverter, which after stated in equations 6.2, the L-TFT (which stands for Load TFT) is always operating in saturation mode, making the inverter circuit, be controlled exclusively by the D-TFT (which stands for Drive TFT). D-TFT can be, depending on the model used, cutted, in triode mode or in active mode. The conditions, for knowing which is the current operating mode in which D-TFT is in the moment, can be easily deducted using equations 6.2 and knowing which is the value of V_{IN} and V_{OUT} in that moment. It's important to state also, that p-type

transistors work with negative voltages values, which can mistake the reader for the equations behavior regarding the L-TFT and D-TFT. If the values are taken in their absolute value, the equations easily become the already known equations for state the behavior of these devices regarding the operating mode functioning.

6.1.2 Organic inverter equivalent circuit – transient analysis

For transient analysis, the organic equivalent circuit must be taken in consideration for determination of the time factor involved. The intention is to determinate the inverter circuit response time for a signal which immediately switches at the circuit input. For this study, the equivalent circuit for signal operation can be take in account. The equivalent circuits, regarding the models presented in chapter 5, can reproduce the time behavior of the organic inverter circuit. In figure 6.2 and 6.3, the equivalent circuits for the organic inverter, using the Amorphous TFT dynamic extensions model and the Brescia VRH dynamic extensions are presented.

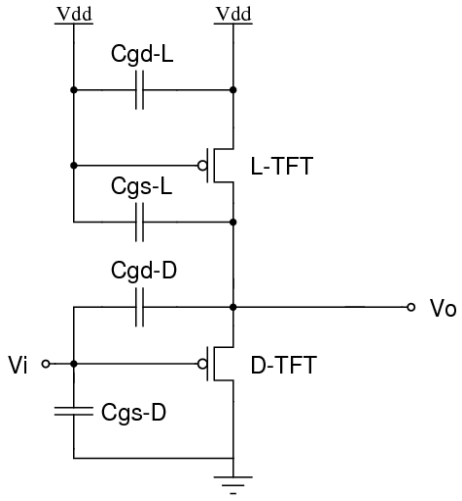

Fig. 6.2 - F8T2 Organic Inverter equivalent circuit for the Amorphous TFT dynamic extensions

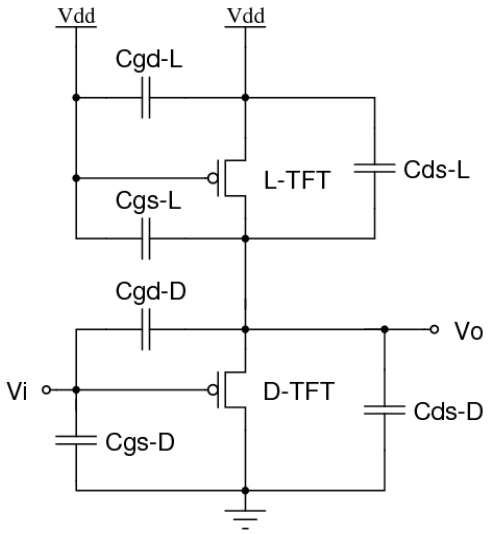

Fig. 6.3 - F8T2 Organic Inverter equivalent circuit
for the Brescia VRH dynamic extensions

As can be observed in figure 6.2, the dynamic internal capacitances of the amorphous TFT are stated, and in figure 6.3 the Brescia VRH additional capacitance between the drain and source of the organic transistor device are also stated.

In equations 6.3 and 6.4, the total capacitance viewed at the circuit's output is stated:

$$C_{OUT} = C_{GS-L} + C_{GD-D} + C_{GS-D} \tag{6.3}$$

$$C_{OUT} = C_{GS-L} + C_{GD-D} + C_{GS-D} + C_{DS-L} + C_{DS-D} \tag{6.4}$$

The equations for the capacitances were also presented and can be consulted in chapter 5. The transistors become in the models pure static devices, having their dynamic behavior controlled by the capacitances.

6.2 F8T2 inverter simulation using the organic models

In this section, the construction of the F8T2 inverter referenced in [15] and implemented in the OTTB system is described with the characteristics signals measured in time. In the next too sections, experimental data measured in laboratory among with the circuit descriptions are exposed among with the comparison of the simulation results.

6.2.1 Experimental measuring of the F8T2 inverter

For implementing an organic F8T2 inverter, the circuit in figure 6.1 is mounted in the OTTB system and the pulse generator is on among with the oscilloscope for voltage characteristics extraction. The huge current leakage and the capacities, make the device operate at really slow modes. The experimental data obtained from a F8T2 inverter can be viewed in figure 6.4.

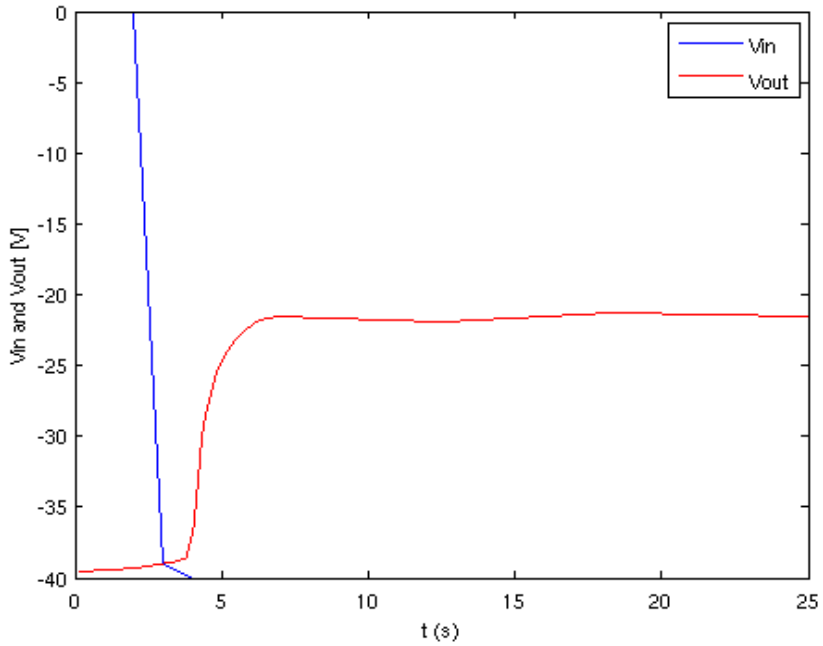

Fig. 6.4 - F8T2 Organic Inverter measured experimentally using the OTTB system

It was found that these transistors are pretty slow when functioning as an inverter gate. It makes sense, since the leakage current modeled resistors in chapter 4 using the ATFT model approach are in the MΩ and the capacitances are in the nF scale, which makes the circuit present a delay of 3.2 seconds in the gate output. Other problem is the voltage decrease when Vin is -40 V, resulting in Vout equaling -22.3214 V at his terminal.

6.2.2 Simulation of the F8T2 inverter

The simulation results are compared with the experimental results presented in figure 6.5. As we can observe the models, manage to reproduce the inverter with it's current leakages making the ATFT model and the Brescia VRH model able to model the F8T2 technology, when precise accuracy in the circuit values is not a problem, for logic circuits these models are able to work with good results.

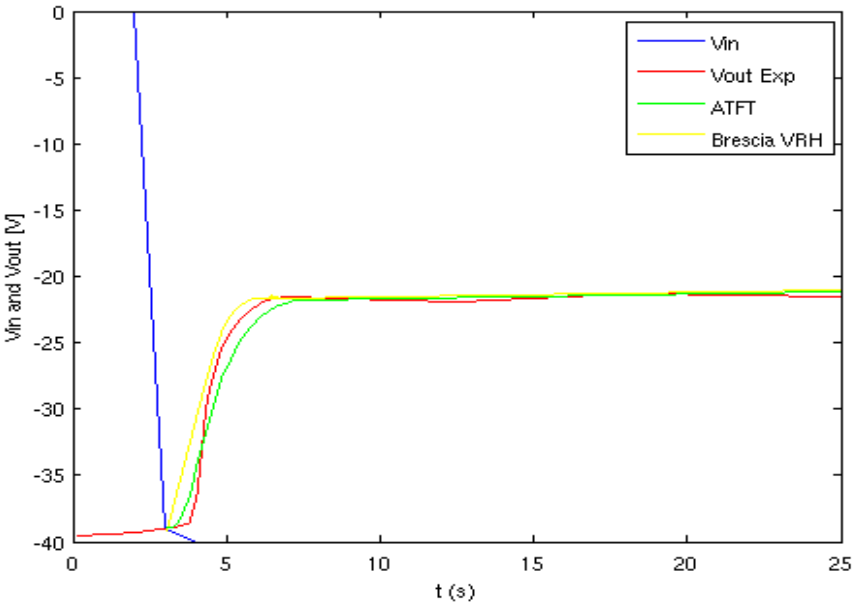

Fig. 6.5 - F8T2 Organic Inverter measured experimentally Vs. Simulation results using ATFT and Brescia VRH model

6.3 Chapter Overview

In this chapter, the Organic F8T2 inverter is analyzed and compared to the simulation of the circuit in VHDL-AMS. This comes forward to the establishment of a model able to simulate logic circuits using the models presented in chapter 4 and 5.

7. Conclusions and Future Work

The bibliography demonstrated that organic transistors circuits are becoming a reality despite the fact that organic technologies still present difficulties in several issues. The OTTB alterations for dynamic measuring and the use of other model to fit the measured data realized that this is actually possible to effectuate. The most recent research already manages to implement F8T2 technology in circuit printers for constructing cheap and flexible circuits with some level of performance.

Due these positive aspects, the future of organic technology is becoming a reality, although this work found improvements and models available for simulate the organic transistors dynamically, this is going to take more time for simulate organic technology successfully.

7.1 Issues yet to deal for Organic Circuits become a reality

Organic material research still is a primitive study and needs several improvement for managing the effectiveness of the behavior of transistors built with this technology. This is the first step for organic circuit projection to become real.

SPICE failed to have the robustness and capacity of implementation for some of the models found in the bibliography. Due this issue, VHDL-AMS was found as an alternative to manage the model implementation.

Besides the OTTB system extended to manage the acquisition of capacitances experimental data from a transistor, the robustness could be improved using capacitance measuring systems despite the use of an oscilloscope.

Matlab fitting tool manage to deal with the fitting in the experimental static data, making the process of data fitting quicker and not dependent of the simulation system, making it handles the models parameters to be fitted only. In dynamic data fitting, there were good results due the simplicity of the ATFT model regarding it's dynamic behavior description.

An inverter using F8T2 was built and showed average results according with the bibliography consulted, although urges the need of improving the technology for having better results due the response observed in chapter 6.

7.2 Organic Transistor Modeling

Models in found in bibliography managed to show good results for F8T2 technology both static and dynamically.

ATFT Model is a good choice for simple simulations, and for logic circuit implementations. The capacitance modeling is simple and the OTTB system for measuring the output capacitance of the transistor resulted in good results when performing the inverter circuit.

Brescia VRH Model, besides having difficulties in fitting the data due the model mathematical complexity, managed to fit the data statically and using the intrinsic capacitance calculated from the ATF Model capacitance fitting, managed to perform a good simulation of the transistor measured in laboratory.

7.3 Future Improvements

Besides the improvements in this technology, the main necessary improvement is still at the level of the technology's materials. The produced devices revealed themselves too much unstable for circuit and system level utilization. Besides the expected low mobility, the studied devices presented some abnormal electrical behaviours like:

- Transistors have shown a hysteresis phenomena in their I-V curves, as the upward sweeping values are different from the downward sweeping values. This is probably due to mobile charges in the used materials, namely mobile ions in the dielectric and/or impurities in the semiconductor.
- The studied transistors still reveal poor temporal stability, as a DC current measure varies in time, even if the biasing conditions are kept the same.
- The poor temporal stability is also observed when several time spaced measures are conducted, for instance, with an interval of several hours or days. In these cases it is observed that the device usually deteriorates, giving worst readings as time passes by.
- It is also a common aspect of organic technologies their fast device deterioration when exposed to the air.
- Considerable current leakages were observed in the measured transistors revealing the need of increasing the semiconductor mobility.

All these weak points of the presented technologies are aspects in which the chemical research team should increase its efforts. So, these are future improvements that must be done in the studied technologies.

In relation to the conducted work itself, several aspects should also be improved:

- The capacitance acquisition system can be improved for better capacitance measure precision and experimental capacitance study.
- The model fitting tools developed should be merged with PME developed in the last work for process automation.
- Current Leakage Modelling should be studied deep and improved.
- After these and eventually other issues have been considered, and having a stable available technology, intensive circuit design and simulation must be considered, so as to achieve the projects' initial goals.

Organic F8T2 technology is still in early stage, as a result, several development work must be done if the expected applications are desired to be achieved in the vicinity of a near future.

8. References

[1] E. Cantore, G.H. Gelink and D.M. De Leeuw, “Polymer Electronics: from Discrete Transistors to Integrated Circuits and Active Matrix Displays”, Philips Research, IEEE BCTM 9.3, pp. 167-172, 2002.

[2] Mekita F. Davis et al., “Integrated RF Architectures in Fully organic SOP technology”, IEEE Transactions on advanced packing, vol. 25, no. 2, May 2002.

[3] E. Cantore and E.J. Meijer , “Transistor Operation and Circuit Performance in Organic Electronics”, Philips Research , IEEE, pp. 29-36, 2003.

[4] Stephen R. Forrest, “The path to ubiquitous and low-cost organic electronic appliances on plastic”, PRISM, Nature, pp. 911-918, 29 April 2004.

[5] E. Calvetti, L. Colalongo and Zs.M. Kovács-Vajna, “Organic thin film transistors: a DC/dynamic analytical model”, DEA, University of Brescia, Solid-State Electonics 49 (2005) 567-577, ScienceDirect, 2005.

[6] Hideyuki Nishizawa and Yutaka Majima, “Analytical Model of Organic Field-Effect Transistor Based on Gradual Channel Approximation with Field-Dependent Mobility”, Japanese Journal of Applied Physics, vol. 45, no. 1, pp. L27-L29, 2006.

[7] L. Colalongo, F. Romano and Zs.M. Kovács-Vajna, “Organic Thin Film Transistors: a DC Model for Circuit Simulation”, DEA, University of Brescia, IEEE, 2004

[8] E.J. Meijer, D.M. De Leeuw, S. Setayesh, E. Van Veenendaal, B.-H. Huisman, P. W. M. Blom, J.C. Hummelen, U.Scherf and T.M. Klapwijk, “Solution-processed ambipolar organic field-effect transistors and inverters”, Nature Materials, vol. 2, October 2003

[9] T. Schneider, J. Mades and M. Glesner, “An Open VHDL-AMS Simulation Framework”, Institute of Microelectronic Systems, Darmstad University of Technology, IEEE, 2000

[10] S. Jemmali, A. Nehme and J.J. Charlot, “Behavioral Modeling of Multi-Technological Systems with VHDL-AMS and simulating with SPICE”, GET/ENST, dept COMELEC, IEEE, 2003

[11] N. Horta, J. Morgado, S. Pinto and V. Pelado, “PLASTIC – Project of Organic Integrated Circuits”, IT Lisbon, IST, July 2006

[12] Stephen R. Forrest, “The path to ubiquitous and low-cost organic electronic appliances on plastic”, PRISM, Nature, pp. 911-918, 29 April 2004.

[13] Dimitrakopoulos, C. D. and Mascaro, D. J. “Organic thin-film transistors: A review of recent advances”, IBM J. RES. & DEV. Vol. 45 No. 1 January 2001.

[14] H. Kawaguchi et al., “Cut-and-Paste Costumization of Organic FET Integrated Circuit and Its Application to Electronic Artificial Skin”, IEEE Journal of Solid-State Circuits, Vol. 40, No. 1, January 2005.

[15] M. Bartzsch, H. Kempa, M. Otto, A. Hübler and D. Zielke, “Device and circuit simulation of printed polymer electronics”, Elsevier B.V., Organic Electronics 8 (2007) 431-438, ScienceDirect, 2007

[16] “Two Dimensional ATLAS device simulation of pentacene organic thin film transistors”, Simulation Standart-journal for Process and Device Engineers, 2003, 12, (2), pp. 1-2

[17] Narain Arora, “MOSFET modeling for VLSI simulation: Theory and Practise”, Cadence Design Systems, World Scientific Publishing, 2007

[18] Soo Young-Ho, Donal E. Ward and Robert W. Dutton, “Trasient Analysis of MOS Transistors”, IEEE Journal of Solid-State Circuits, Vol. SC-15, No. 4

[19] Serag M. Gadelrab and James A. Barby, “Creative Methods of Leveraging VHDL-AMS-like Analog-HDL Environments. Case Study: Simulation of Circuit Reliability”, Analog Integrated Circuits and Signal Processing, 16, 152-172 (1998)

[20] Y. P. Tsividis and K. Suyama, “MOSFET modeling for analog circuit CAD: Problems and prospects,” IEEE J. Solid-State Circuits, vol. 29, no. 3, pp. 210–216, Mar. 1994.

A.1 F8T2 Organic Technology Overview

In appendix 1, the technology measured in laboratory and the analysis of the devices is effectuated. This appendix intends to expose the data in which this work based for defining the most adequate models in the consulted bibliography for simulation porposes. In the next sections, the device analysis based in the experimental data is presented, and for the porpose of picking the most adequate models for simulation of these devices. The simulation problems, in this technology are also exposed for stating the issues regarding non-linear behavior in these devices.

A1.1 Dictylfluorene-bithiophene based organic devices (F8T2 based)

F8T2 allows easy construction of organic devices, which is one of the major reasons that makes interesting the construction and study of devices based in this material.

F8T2, or Dictylfluorene-bithiophene, is a polymeric organic liquid crystal semiconductor. This material allows, when applied an electric field, build a channel and allow conduction of current. This behavior is similar to the silicon based TFT. With F8T2, it will be possible to construct organic integrated circuits using devices which work just like inkjet printers (it is already possible using other organic materials). The main advantages of this material are the capacity of solve in solvents and being stable in air. Although being a very promising technology, this material is still in a test phase and it's only possible to construct p-type transistor devices with it (n-type can't work in open air). This last matter makes construction of digital devices restricted to p-type devices only (this is exposed in more detail in chapter 6).

A1.2 F8T2 based devices hybrid architecture

The devices tested are an hybrid type of organic transistor, only the semiconductor material is organic. The construction of these devices follows an architecture known as Thin Film Transistor structure. The TFT architecture of F8T2 devices is showed next in figure A1.1:

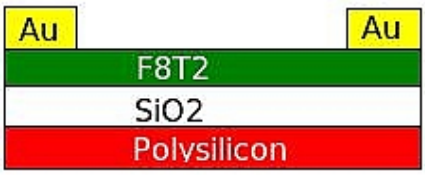

Fig. A1.1 - The F8T2 TFT architecture

As is seen in figure A1.1, the TFT gate is made of polysilicon a extremely doped silicon semiconductor, making this device having the same material as the silicon based transistors have in the gate. The dialectic is also the same material as MOSFET transistors, which is SiO_2 – Silicon Dioxide. The contacts, drain and source, are made of Au – Gold. Gold is known for being a great conductor. The only difference, despite the silicon TFT architecture, is the semiconductor which is made of the already presented material – F8T2. It's important to state that these devices are p-type devices, n-type devices only work under vacuum which makes the technology only implemented with p-type transistor circuits at this stage.

A1.3 Static characteristics of the F8T2 devices

In this section the static analysis of the experimental data is exposed and the particularities of the devices are exposed. It starts by a three dimensional view of the device's operation modes and how the annealing process under vacuum influences the F8T2 device behavior.

A1.3.1 F8T2 based hybrid device operation

This section describes the operation modes of the F8T2 devices described in the last section. As an analogy to the MOSFET, the F8T2 based TFT device has also triode and saturation mode when a conduction channel is built. The major difference appears when no channel is built, the TFT behaves like a almost linear resistor due the absence of hetero-junctions in the TFT structure. These devices, as mentioned in section A1.2, consist on p-type devices. For better understanding of the various operating modes of the F8T2 TFT, the three operation modes are exposed in the figure 2.2 through experimental data acquired from a F8T2-based device:

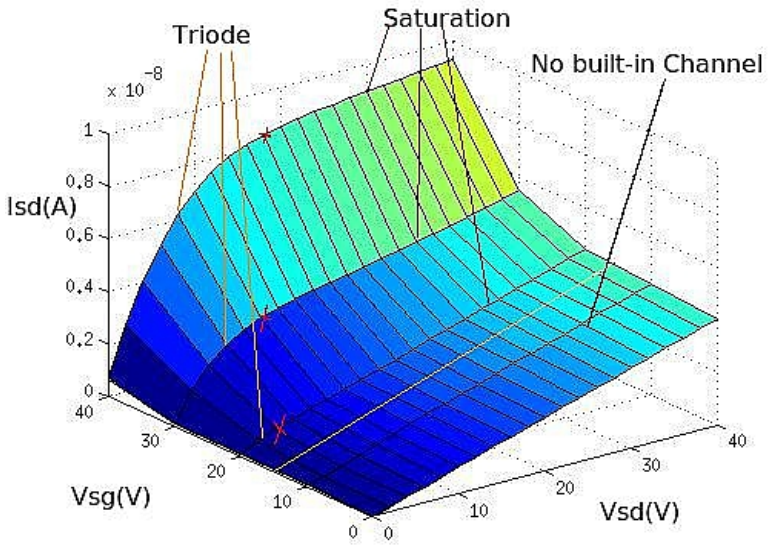

Fig. A1.2 - F8T2-based TFT operation modes seen through experimental data

In figure A1.2, the operating modes are exposed, it consists on a surface with 5 current curves. The red crosses mark the frontier between the triode and saturation mode, this operating modes exist when the the V_{SG} is equal or greater than the device threshold voltage (V_T).

The frontier between built-in and not built-in channel is marked with the yellow line for easier understanding. When V_{SG} is less than V_T, the channel is not built and the device has a linear current increase as V_{SD} increases too. In the next subsections, each operating mode is described in detail. Mathematical models for simulation these devices are described in detail in chapter 4.

A1.3.2 No built-in channel mode

Due the TFT architecture, if the Gate-Source voltage is less than V_T, the device still conducts and acts almost like linear resistor. This happens due the nonexistence of hetero-junctions, which in the silicon MOSFET case, allows the existence of a cutoff mode (like a diode that doesn't conduct when the current is forced to pass from the cathode to anode). The cutoff mode, just like the name suggests, makes the device's semiconductor act as a resistor with a very large value, this makes the current dispose very small values as is compared with the same device functioning in the other two operating modes.

With a TFT architecture, an organic device passes current between the drain and the source even with absence of electric field applied to the gate (in other words, making V_{SG} = 0V). This effect is observed when the analysis consisting in the isolation of the experimental data in this functioning mode

is made, the experimental data is demonstrated next in figures A1.3 and A1.4.

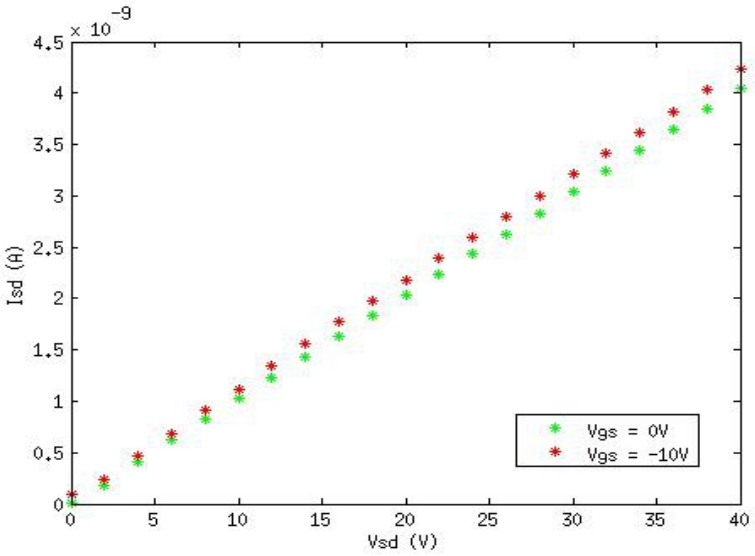

Fig. A1.3 - F8T2-based device functioning in no built-in channel operating mode measured in air after annealing of the film at 90 oC for 15 minutes under vacuum.

Analyzing figures A1.3 and A1.4, a major difference is observed. The first device demonstrates a linear current growth and show currents in the order of 10^{-9}A, making the device behaving as a linear resistance. The second one, exposes a more peculiar effect: when V_{SD} is small the current is non-linear. This last property conducted to two conclusions: the first conclusion is that these devices have current leakages, specially when V_{SD} is small; the second conclusion is that these devices have large capacitances, making the current discharge slow and interfering in the static measures. In both devices, the resistance between the drain and the source show decreasing as V_{SG} increases, specially in the device of figure A1.4.

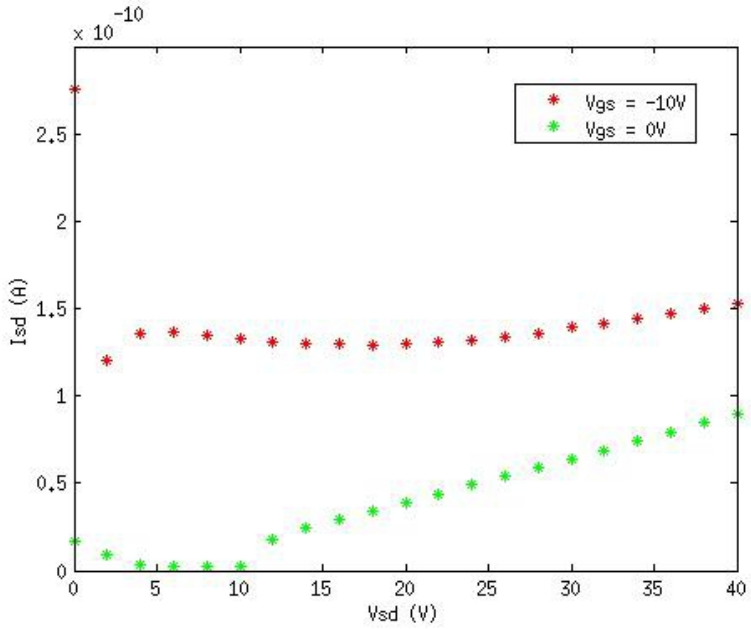

Fig. A1.4 - F8T2Ox-based device functioning in no built-in channel operating mode measured in air after annealing of the film at 110 oC for 15 minutes under vacuum.

Having this analysis in consideration, the construction of a model to simulate these devices must have the ability model this situation. The major problem is the modulation of the non-linearity that can be observed in these devices, in chapter 4 the models to simulate F8T2-based devices are presented with the exposition of the obtained results.

A1.3.3 Triode mode

When a built-in channel is created, the device begins to increase the current between the drain and the source in an exponential form (as can be seen in figure A1.2). In this operating mode, the channel is beginning to be constructed. This exponential current growth maintains until the saturation point is reached, which makes the device to change to saturation operating mode. The operating mode frontier points are the ones marked in figure 2.1 with the red crosses.

Saturation points depend on the voltage applied to gate-source and the threshold voltage of the device. These points are also called VSD_{SAT}, which is the point for a given V_{SG} and V_{SD} voltage, were the device with a built-in channel changes from triode to saturation mode.

This operation mode, as analyzed in figure A1.2, show no peculiar effects as compared against the previous introduced non-built channel operating mode. This happens due the current difference passing between the drain and the source make the effects observed in the no built-in channel mode

dispensable. This is explained by the current leakage being much smaller than the current passing in the built-in channel.

A1.3.4 Saturation mode

When these devices reach saturation mode (V_{SD} reaches the VD_{SAT} – the red crosses in figure A1.2, ideally, the current should be constant or have a linear increase (like it happens in the MOSFETs). Physically speaking, the built-in channel stops increasing as the gate-source voltage increases. The observed effects in organic technology current when operating in saturation mode, is that the channel can have an almost linear growth; can have a almost constant current; or it can have a almost linear current decrease. Some organic devices have demonstrated a constant current growth, but with the analyzed technology in this work – the F8T2-based, this last effect is not observed. The F8T2-based devices have an almost linear growth in their current as Vsd increases, or they expose a linear current decrease under the same situation.

The two described effects are observed in experimental data disposed in figures A1.5 and A1.6:

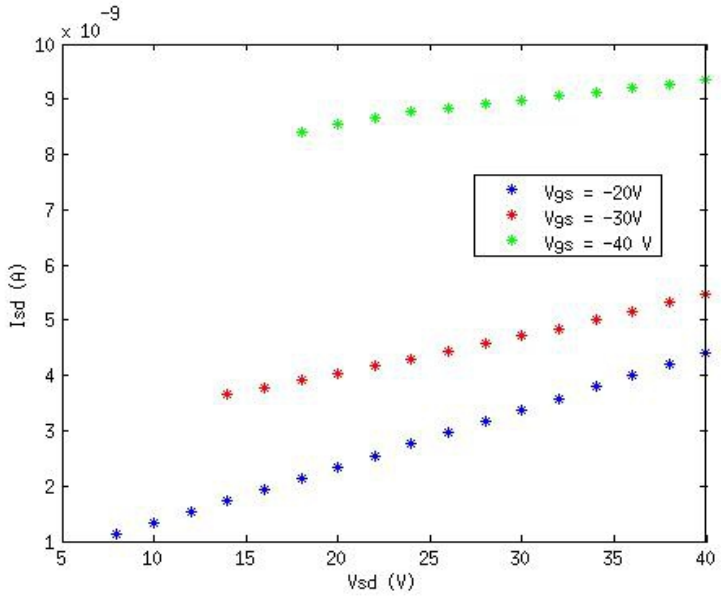

Fig. A1.5 - F8T2-based device functioning in saturation operating mode measured in air after annealing of the film at 90 oC for 15 minutes under vacuum.

As can be observed in figure A1.5, the device has a linear current growth as it has when no built-in channel exists in the device semiconductor. This current growth happens due the built-in channel conductivity being of the same greatness than the semiconductor with no channel built. For better understand, is just like two resistors in parallel – if the part with no channel expose a small resistance, the current contribution between the drain and the source is significant.

On the other case, in figure A1.6 the current decreases as V_{SD} increases. This effect is observed in many organic devices making look like the channel was submitted to a stress of some kind, this “stress effect” happens due current leakages observed through the gate. This stress effect can be significant in some cases, making current leakage, again, a very important factor to model.

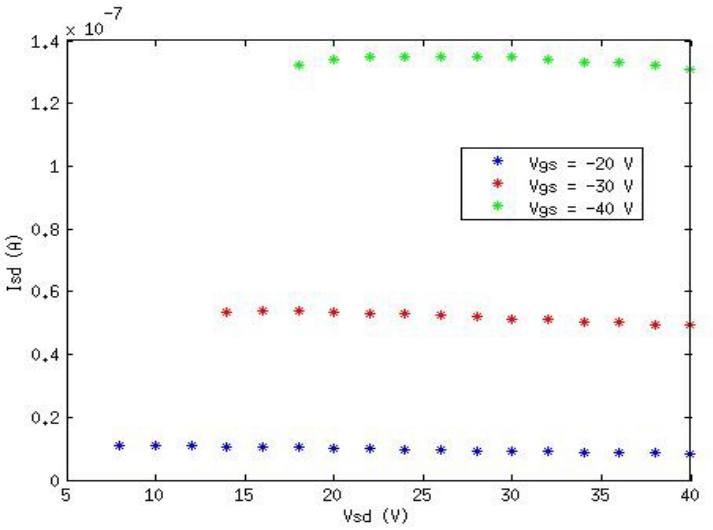

Fig. A1.6 - F8T2-based device functioning in saturation operating mode measured in air after annealing of the film at 110 oC for 15 minutes under vacuum.

A1.4 Dynamic characteristics of the F8T2 devices

Using the oscilloscope and the pulse signal generator from the OTTB system, it was possible to measure the capacitances experimentally, although it was only possible to measure them for V_{SD} = -40V. This happened due circuit limitations in the OTTB system, which in the measuring capacitance process couldn't change regarding the instability found in the F8T2 devices. In figure A1.7, the capacitances measured using the OTTB system with the oscilloscope are displayed for V_{SG} equaling 40 V.

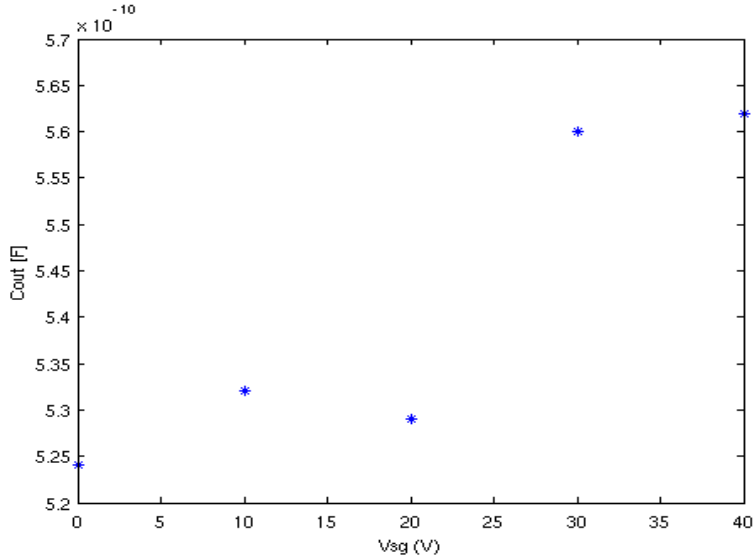

Fig. A1.7 - F8T2-based capacitance measuring in air after annealing of the film at 110 oC for 15 minutes under vacuum.

The capacity increases along with V_{SG}, notice that this device is operating in saturation mode. In saturation the output capacity increases when the gate-source voltage is high.

Having all the experimental results exposed, this concludes the experimental results annex obtained using the OTTB system.

A.2 Using the Parameter Extraction Tool and Fitting results

In appendix 2, the tools used and a brief introduction to them are going to be described among with the procedures to be taken to perform the capacitance extraction, parameter fitting and model simulation.

A2.1 Performing capacitance extraction using the OTTB system

For performing capacitance extraction, a circuit was built using in the OTTB system. The circuit is showed in figure A2.1.

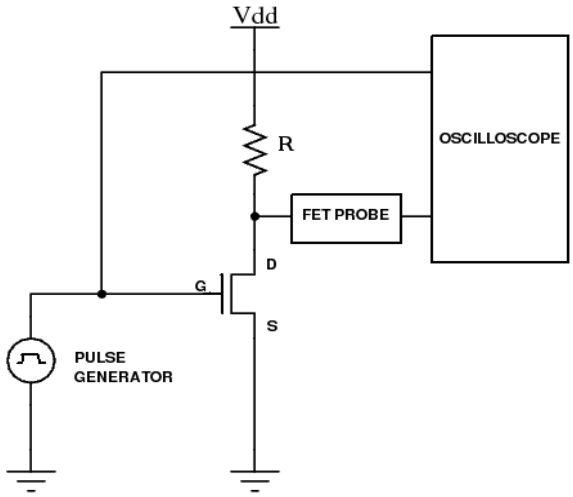

Fig. A2.1 - Circuit for intrinsic capacitance parameter extraction

The circuit in figure A2.1 is the used with a resistor of 1GΩ. After this, the tool is run to change the pulse amplitude by performing variation of the V_{SG} voltage source the V_{SD} voltage source is fixed. For this case, it's fixed at V_{SG} = 40V. The oscilloscope is configured by the Matlab application which is called *Capextract*. This application communicates with the OTTB board voltage sources and oscilloscope by GPIB interface. Due the Resistance-Capacity combinations that these F8T2 devices have, no periodic signals could be performed and the oscilloscope has to be set to one-shot mode. The one-shot mode runs 5 seconds (default time) per V_{SG} pulse amplitude value and the increase by default is of 10 V in module. This can be configured if the parameter is given. Capextract Matlab command receives the following parameters:

- VSGMax – Maximum amplitude that finishes the measuring of the output capacitance;
- VINT (optional, default is 10V) – voltage interval between values;

- period (optional, default is 5s) – acquiring duration period per pulse signal activation.

The output is a vector of experimental capacitance values - Cout vector, which are calculated after performing the transient method described in chapter 2 and 3 in the solution architecture.

A2.2 Static Fitting using non-linear regression

Static, is a simple Matlab command tool that using the experimental data is able to perform parameter fitting using a desired model. This tool starts from experimental data which is supplied by the OTTB system or can be obtained by other experimental measures after performing data importation such as Microsoft Excel files. This tool receives the following parameters:

- Isd – The experimental measured source-drain curves, this is represented by a matrix;
- Vsg – The voltage between source and gate which were applied to the device for performing the measuring of Isd;
- Vsd – The voltage between source and drain which were applied to the device for performing the measuring of Isd;
- a0 – The parameter values initial guess (calculated by performing calculations in the experimental data and supplying known parameter values);
- @model – The model which is desired for performing the parameter fitting. This parameter comes as a Matalb Function file. For example, the pure Meijer model can be defined as:

```
function F = Meijer(a,data)

 %MEIJER Summary of this function goes here
 %   Detailed explanation goes here
  function F = xMod(x)
    F = 0.5*x + 0.5*abs(x);
  end

 x = data(1,:);
 y = data(2,:);

 F = a(1)*(xMod(y-a(2)).^2-xMod(y-a(2)-x).^2);

end
```

Which applies for the pure definition of the Meijer mathematical model.

After this, the parameter fitting is performed and the results are demonstrated on the screen for the user to avail if the model fitting using the supplied mathematical model is adequate for representing

those organic transistors. The output is a vector of parameters a, which are related to the user's definition. For the Meijer example a(1) is the trans-conductance of the organic semiconductor and a(2) is the threshold voltage of the organic device.

A2.3 Dynamic Fitting using non-linear regression

Dynamic is the Matlab command tool which performs the fitting and extraction of the C_{IN} parameter measured experimentally and, which stands for the device intrinsic capacitance. This Matlab Command receives the following parameters:

- Cout – The output capacitance measured using the OTTB system with the oscilloscope and the Capextract tool already described in section A2.1;
- @Model – The model that describes the calculation of the device's ouput capacitance in agreement with the transistor model desired.
- Vsg – The pulse amplitude values vector applied to the transistor device;

The output is the C_{IN} parameter calculated through parameter fitting. For example, in ATFT model this is simple, although in Brescia VRH model this can be a complex process - since the equation resulting of the parameter calculation is sustain in the equations presented in chapter 5 and are of several complexity.

A2.4 Fitting Results using the Models Porposed

In this section, the fitting results using the static models porposed in chapter 4 and the dynamic extensions of the ATFT model in chapter 5. The fitting results are:

- ATFT Model (using Meijer as the current source and modeling the current leakages with resistances)

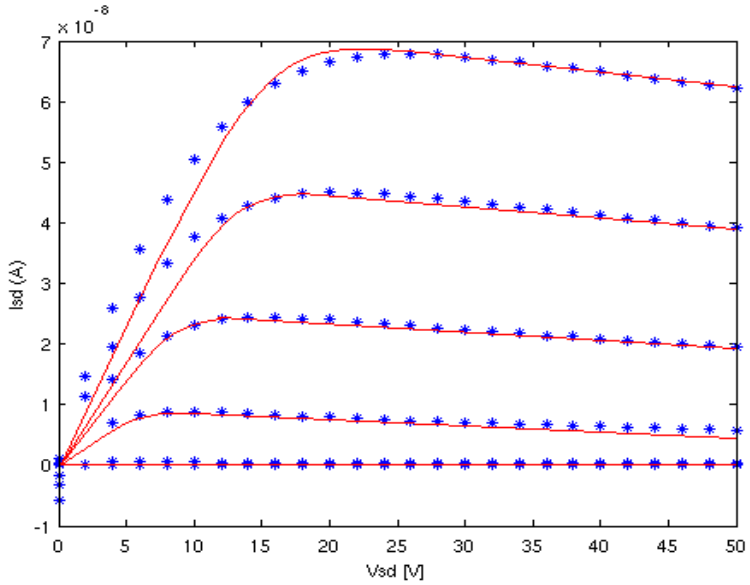

Fig. A2.2 - Fitting and F8T2 TFT with ATFT Model

- Brescia VRH Model

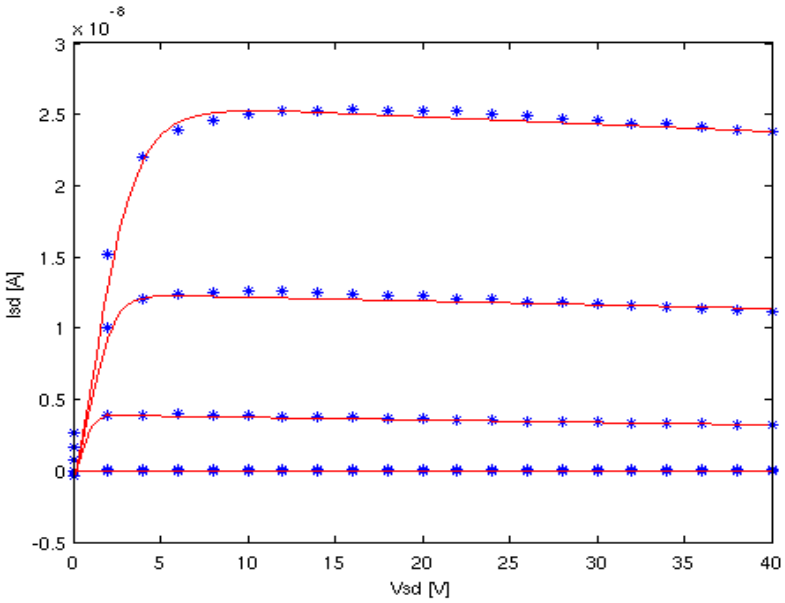

Fig. A2.3 - Fitting and F8T2 TFT with Brescia Model

A2.4 Simulation Software used

For performing the simulation of the devices standalone and the simulation of the inverter circuit, the technologies used for SPICE (only for standalone device simulation) was Linux version of HSPICE.

For performing VHDL-AMS simulation (standalone and inverter) the Linux version of Dolphin SMASH was used.